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# **$\Delta\Sigma$ Digital-RF Modulation for Adaptive Wideband Wireless Transmitters**

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# Current Trends in Wireless Systems

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- **Next generation wireless systems aim to provide data rates pushing towards Gb/s**
  - Wider channel bandwidths
  - 802.11n, UWB, 60 GHz
- **Systems are employing OFDM and more bits/symbol (64-QAM, 256-QAM)**
  - High PAPR leads to low PA efficiency
- **System on Chip (SOC) design approach**
  - Integration of analog/RF with digital
  - Use more digital circuits to take advantage of process scaling

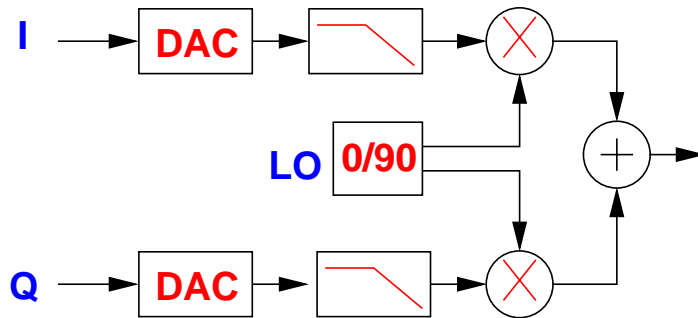
# Motivation

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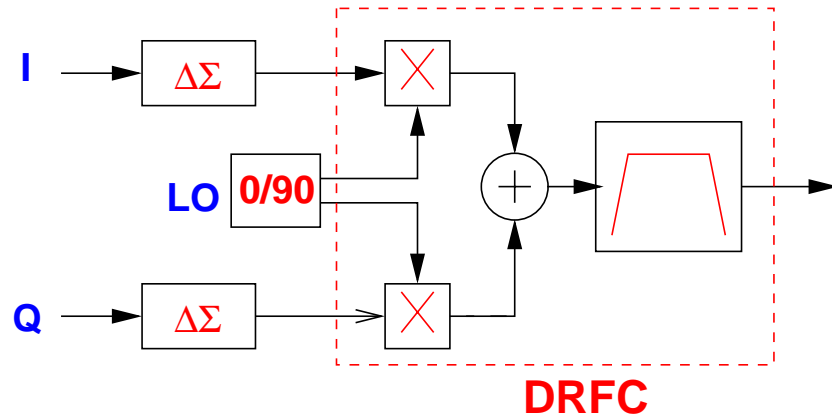
- **Design a power and area efficient, wideband, programmable digital-RF modulator with high dynamic range and Gb/s data rates**
  - PA linearization techniques often result in significant increase in signal bandwidth
    - Digital Pre-Distortion, Polar Modulation, Outphasing
  - Wide bandwidths do not allow use of closed-loop PLL modulation
  - Multitude of wireless standards requires distinct radios for each set of specifications

# $\Delta\Sigma$ Digital-RF Modulator

IQ Modulator

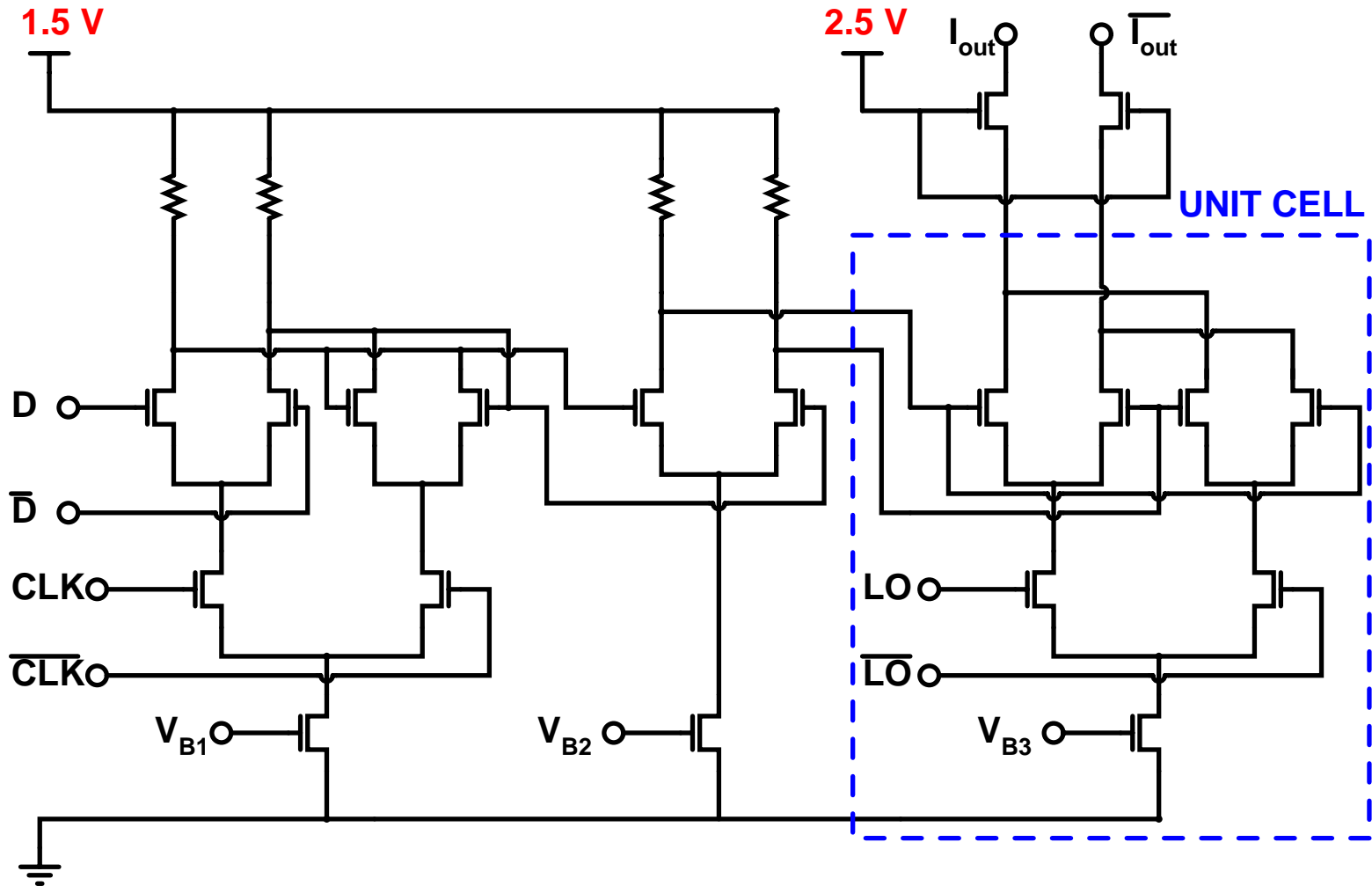


$\Delta\Sigma$  Digital-RF Modulator



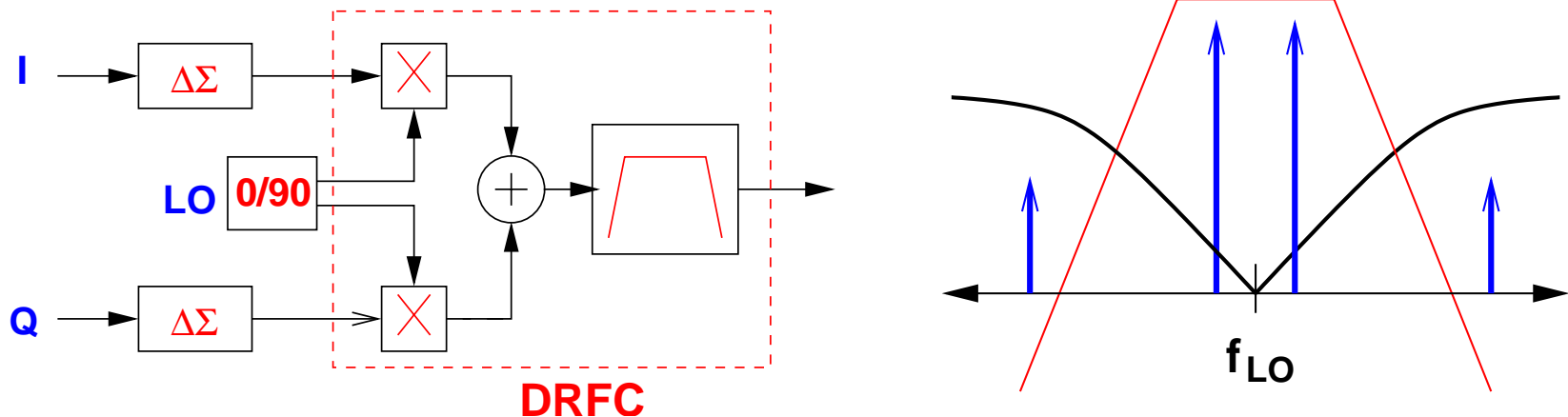
- Replace high dynamic range analog circuits with high speed digital circuits, active LPF with passive BPF
- No analog impairments in baseband path
- Performance improves with digital CMOS scaling
- Digital Inputs -> RF Output

# DRFC Unit Cell Schematic



# DRFC Requires RF Filtering

## $\Delta\Sigma$ Digital-RF Modulator



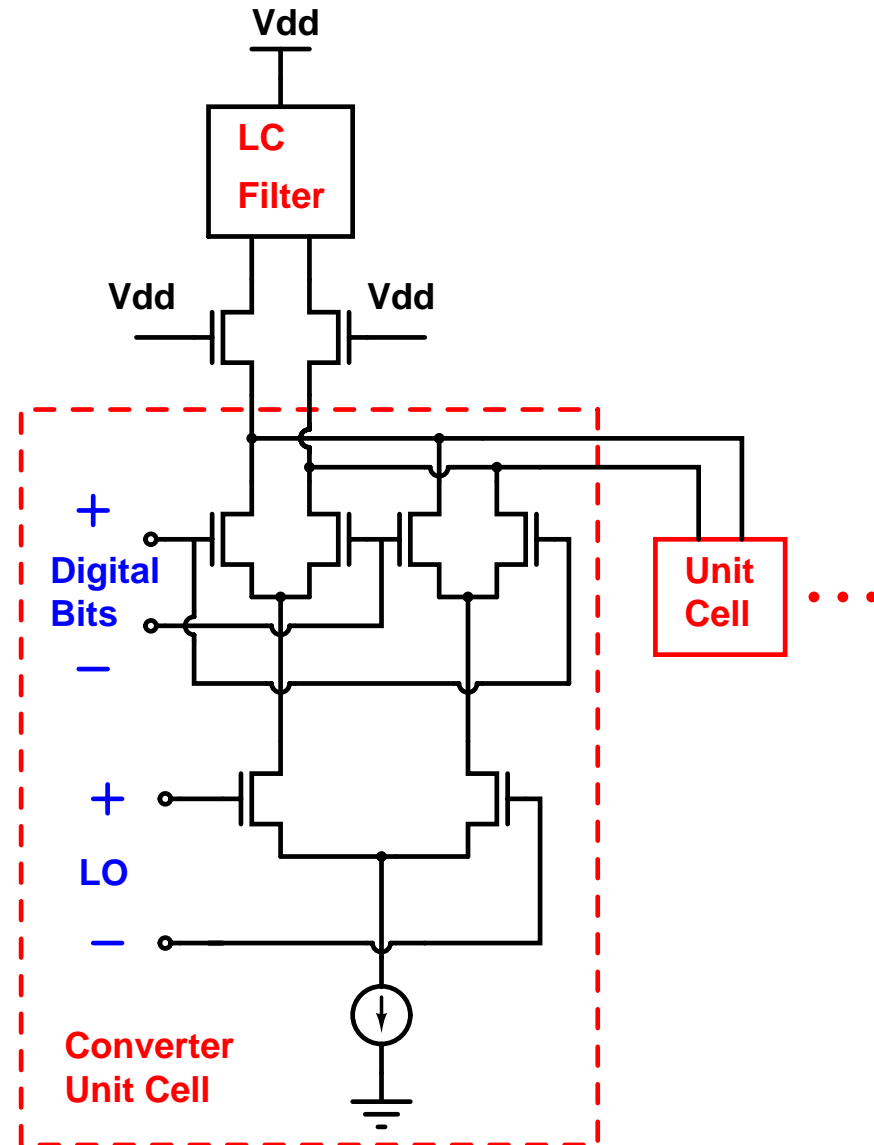
- Clock images and quantization noise of digital signal are up-converted without filtering.
- Previous works (Luschas [1], Eloranta [2]) require off-chip filtering to suppress spurious signals

[1] S. Luschas, R. Schreier, H.S. Lee, "Radio Frequency D/A Converter," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1462-1467, Sept 2004.

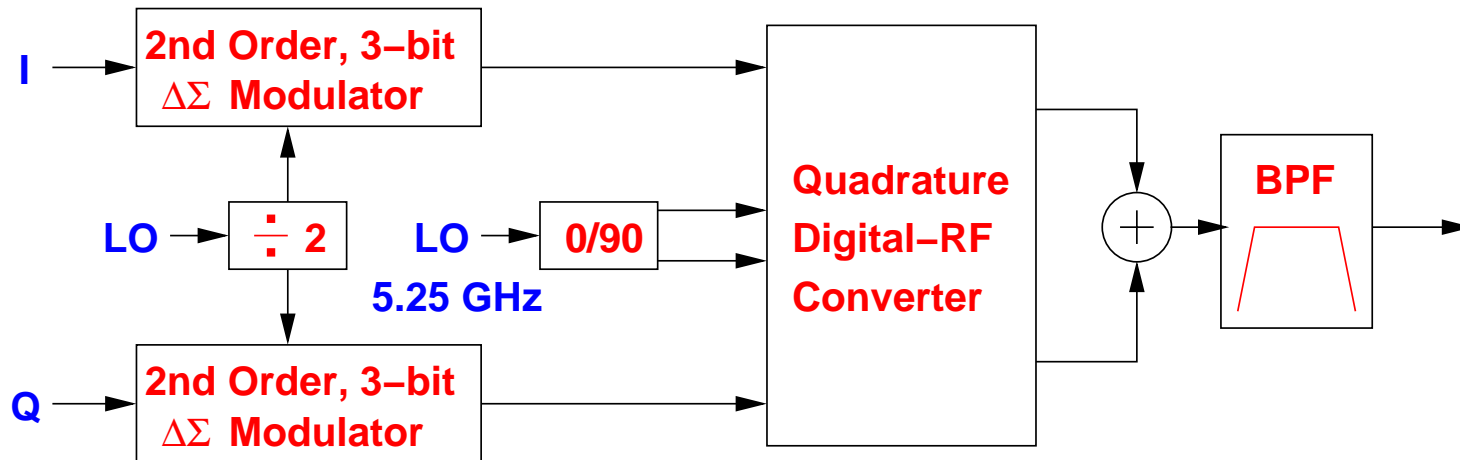
[2] P. Eloranta, and P. Seppinen, "Direct Digital-RF Modulator IC in 0.13  $\mu\text{m}$  CMOS for Wide-Band Multi-Radio Applications," *ISSCC 2005*, pp. 532-533.

# RF Reconstruction Filter

- Integrate passive LC BPF with DRFC cells
- Low noise and distortion
- Challenges : High Q, and tunability
- Favorable Trend
  - As bandwidth increases, LC filter becomes easier while analog filter becomes harder



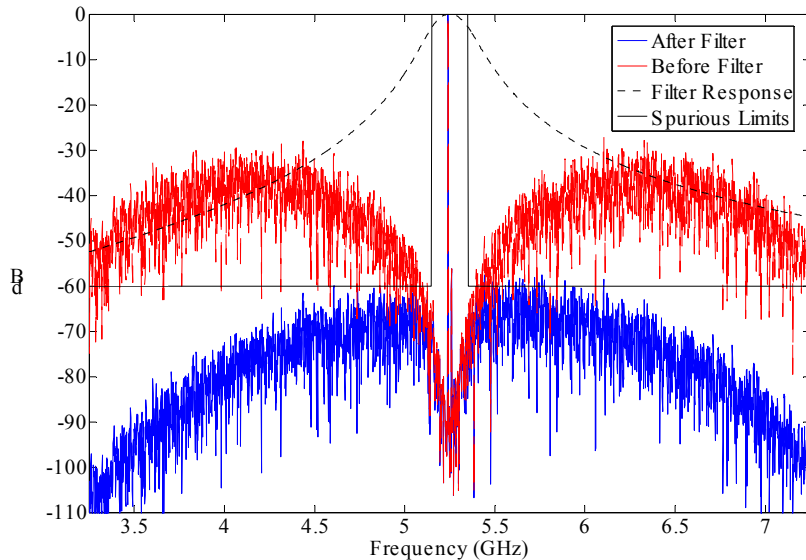
# System Design



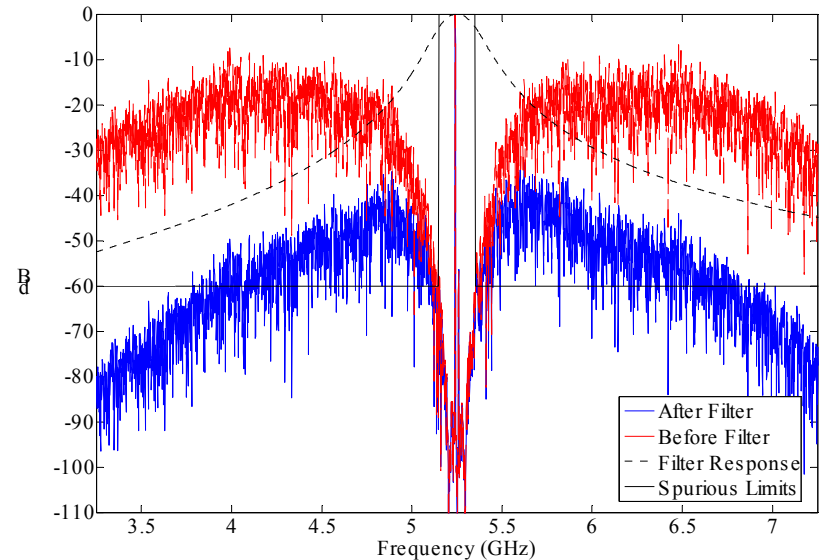
- **5.15-5.35 GHz UN-II band**
  - OFDM : 1 MHz sub-carrier spacing, 200 sub-carriers
  - 256-QAM -> Maximum data rate of 1.6 Gb/s
  - $f_{\text{clk}} = 2.625 \text{ GS/s}$
- **SNR > 45 dB, assuming**
  - SNR (256-QAM) > 30 dB
  - PAPR ~ 15 dB

# Co-Design of $\Delta\Sigma$ Modulator and RF BPF

4<sup>th</sup> Order BPF, 2<sup>nd</sup> Order 3-bit  $\Delta\Sigma$

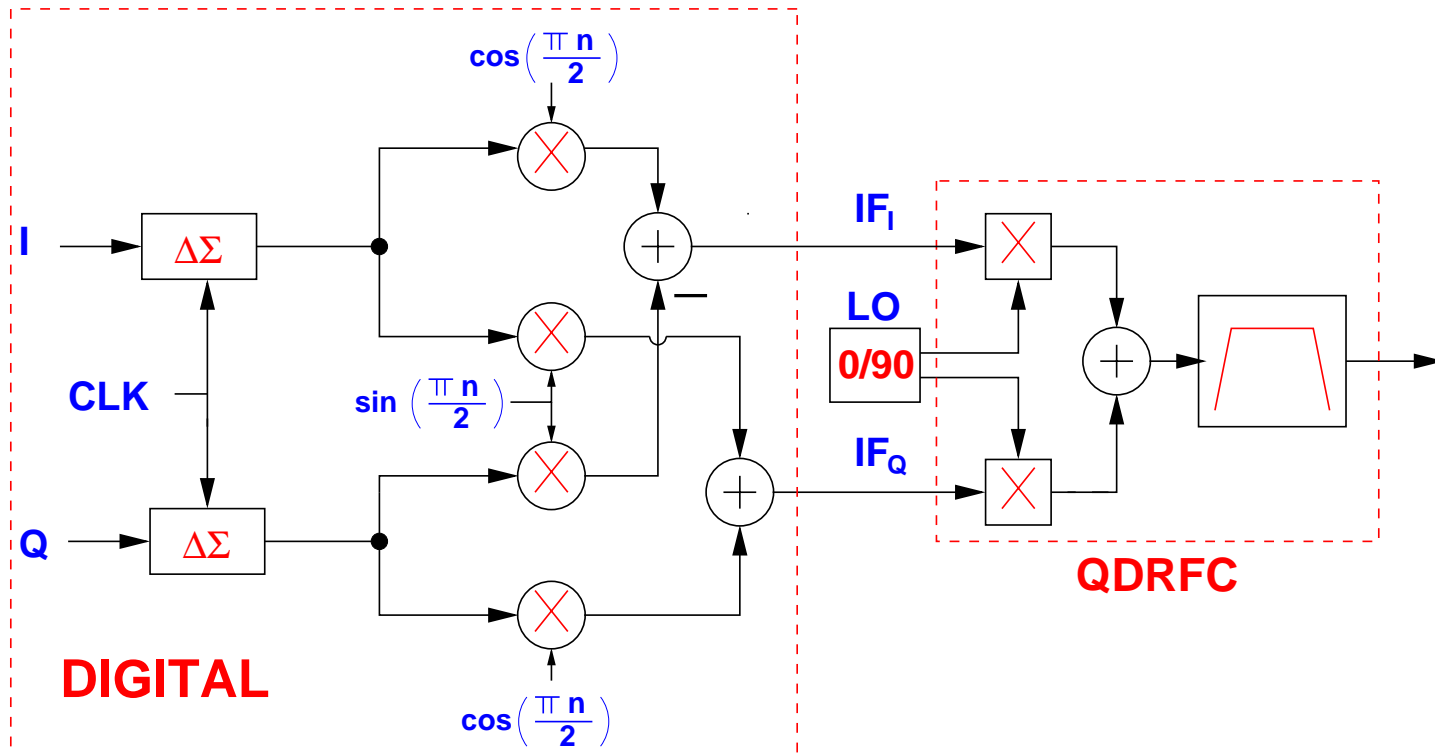


4<sup>th</sup> Order BPF, 3<sup>rd</sup> Order 1-bit  $\Delta\Sigma$



- Lower Order, Multi-Bit  $\Delta\Sigma$  Modulator allows RF BPF to be realizable on silicon

# Digital-IF



- Eliminate in-band LO and image spurs
- Quadrature digital mixers can implement ideal IF up-converter
  - Use  $f_{IF} = f_{CLK}/4$  to avoid multipliers and save power

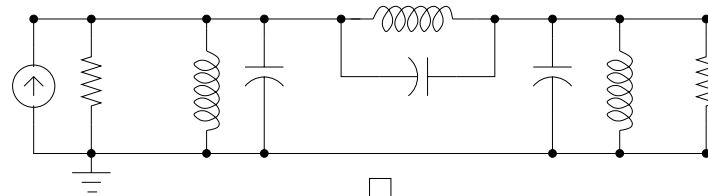
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**Circuit Blocks :**

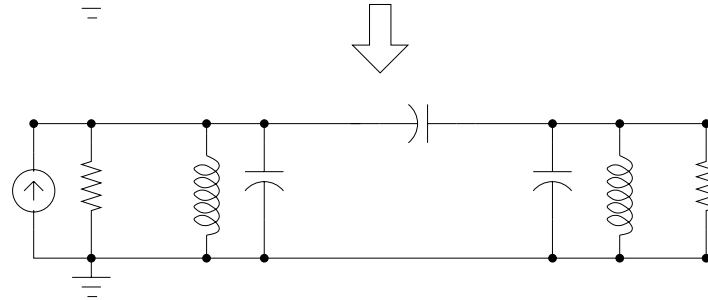
**RF BPF**  
**and**  
**Digital  $\Delta\Sigma$  Modulator**

# Passive RF BPF Design

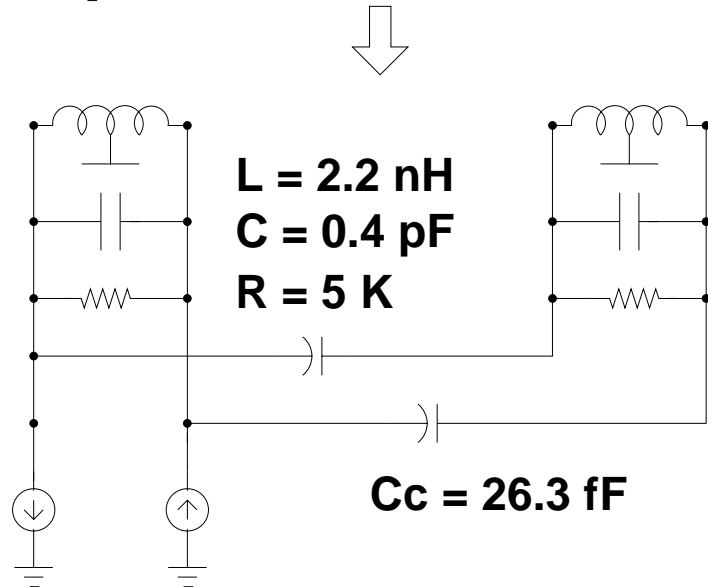
- Minimize Area
- Maximize Q



Bandpass  
LC Ladder  
Filter



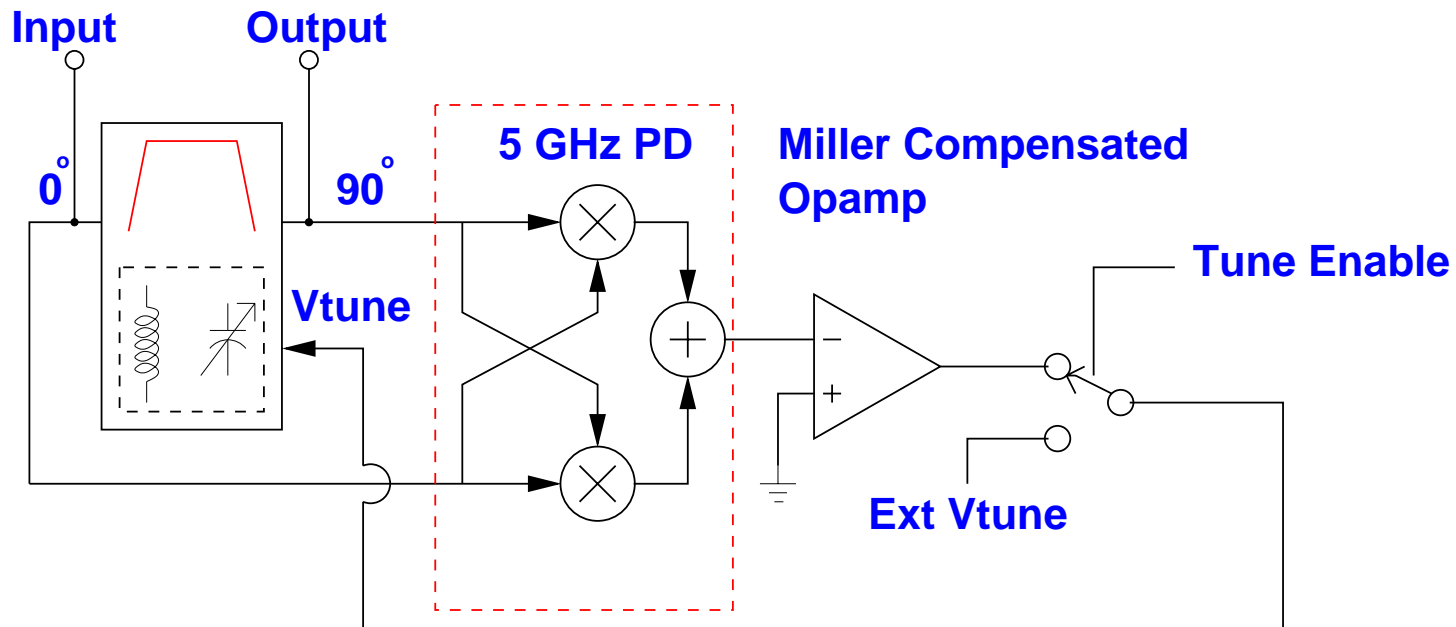
Coupled  
Resonator  
Filter



Differential  
Coupled  
Resonators

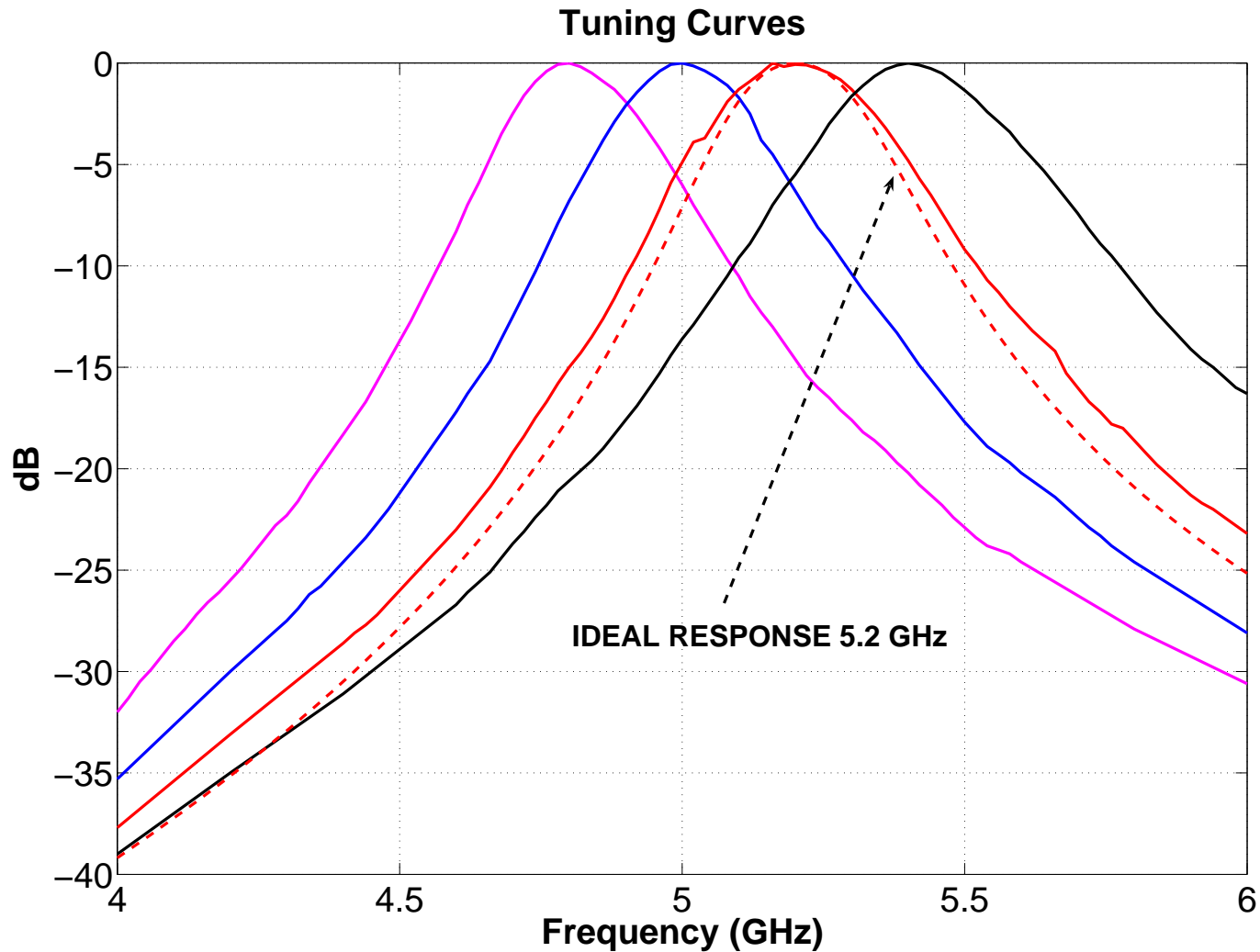
- $Q_{\text{ind}} = 25$
- PN varactor used for C

# Automatic Self-Tuning Loop

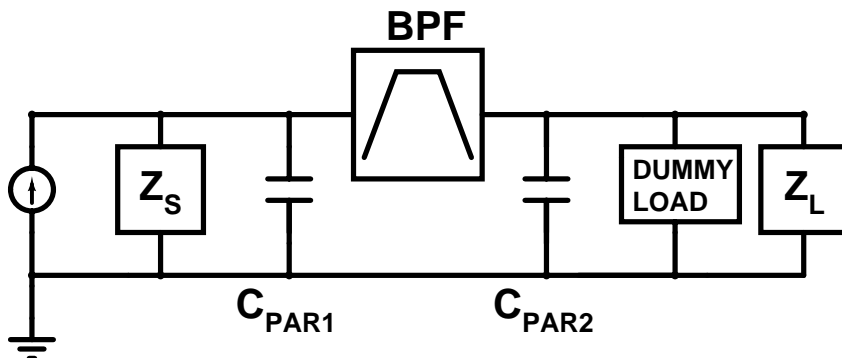
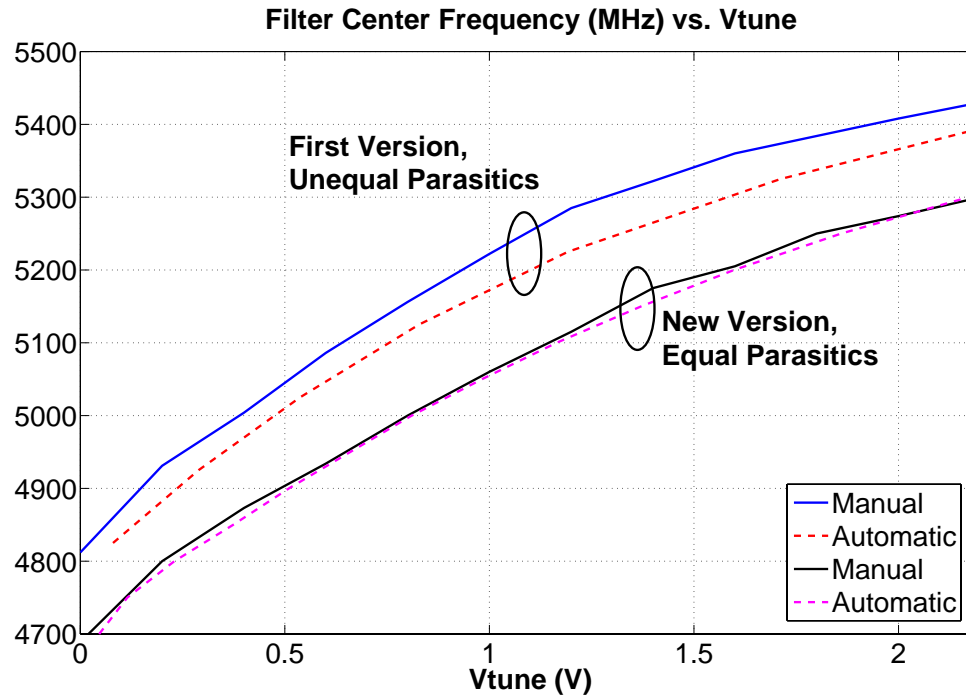


- **Filter tuning typically requires replica resonator, reference frequency, PLL**
- **Self-Tuning Loop avoids matching issues**
- **Calibrate using system LO signal**

# Measured Filter Response



# Auto Tuning Measurements



- If source and load impedances are equal, filter has  $90^\circ$  phase shift at  $f_o$

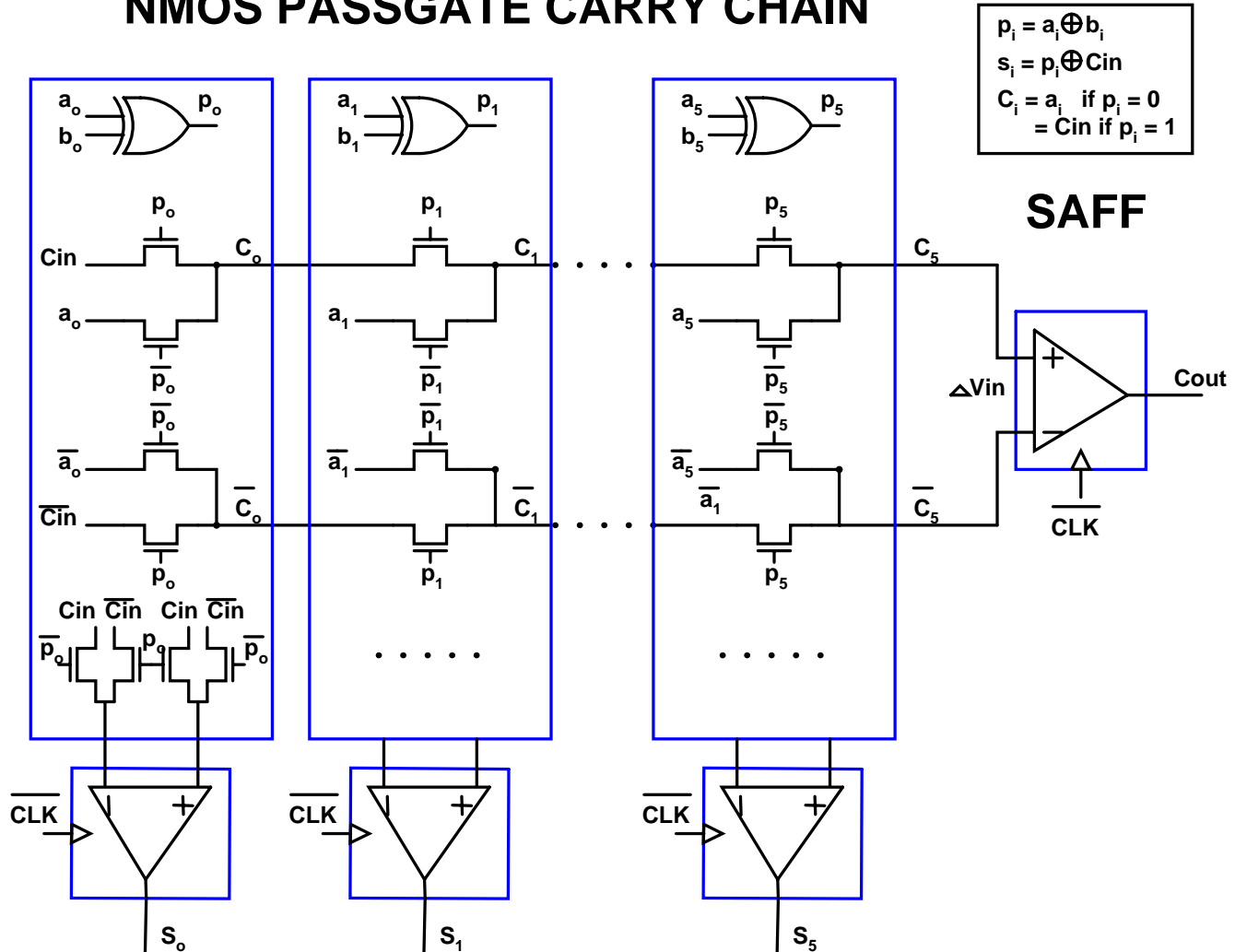
# **High Speed Digital $\Delta\Sigma$ Modulator**

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- **For use in radio transceivers, digital processing must be optimized for low power and medium resolution (~ 12 bits)**
  
- **Digital circuits operating at high sample rates**
  - Heavily pipelined (2-3 logic functions per pipeline stage)
  - Flip-flop power is substantial portion of total power
  - Clock power is high
  - Avoid multipliers for lower power implementation

# Passgate/SAFF Adder Design

## NMOS PASSGATE CARRY CHAIN

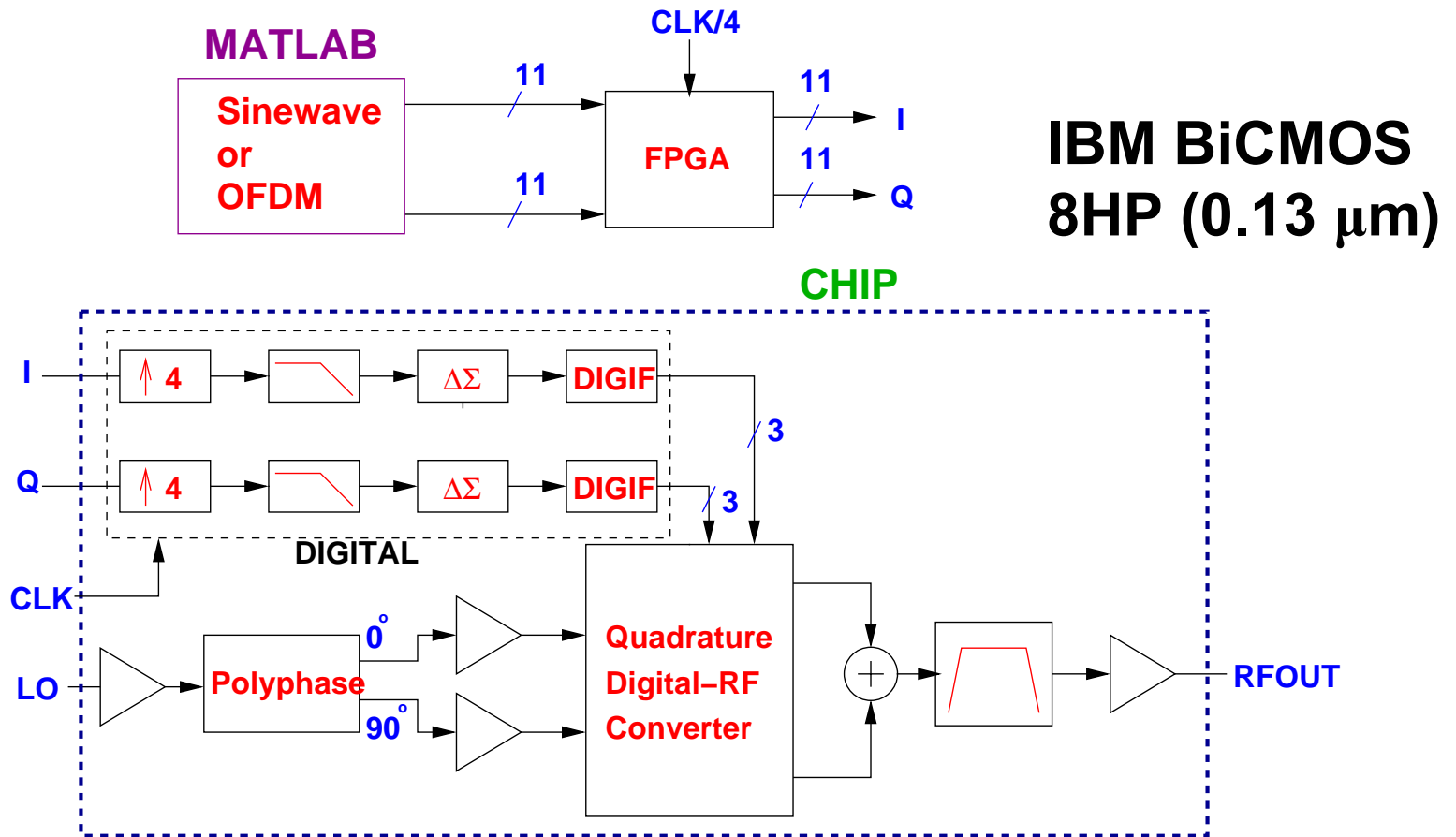


# Adder Design Comparison

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$f_{\text{clk}} = 2.5 \text{ GS/s}$	Pass-Gate SAFF	Static Mirror	Dynamic CLA
Pipelining Factor	2	6	1
Adder Cell Power	1.8 mW	3 mW	19.9 mW
Flip-Flop Power	8 mW	15.3 mW	-
Clock Driver Power	2.5 mW	7.7 mW	13.4 mW
Total Power	12.3 mW	26 mW	33.3 mW

# Test Chip



**IBM BiCMOS  
8HP (0.13  $\mu\text{m}$ )**

**LO = 5.25 GHz**  
**CLK = 2.625 GHz**

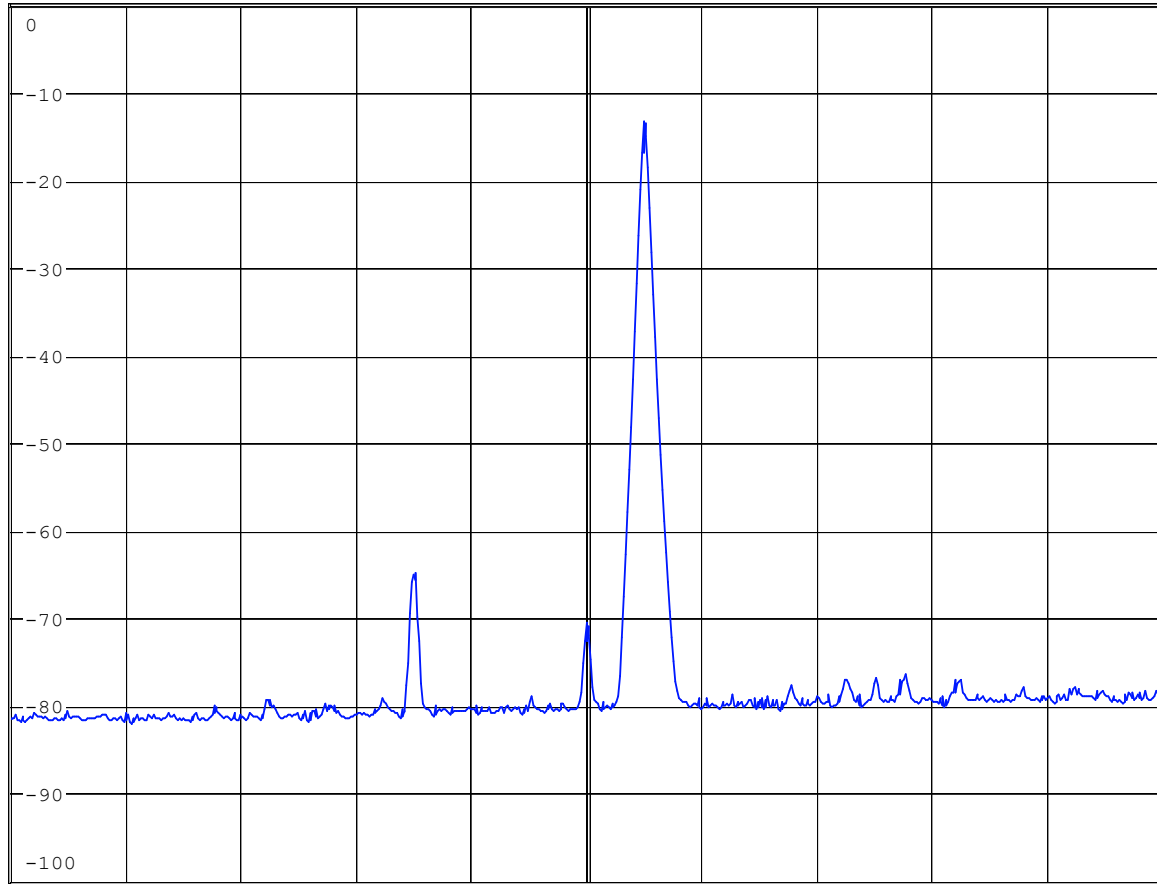
# Single-Tone 12 MHz Input



\* RBW 1 MHz  
\* VBW 10 kHz  
SWT 50 ms

Ref 0 dBm \* Att 5 dB

1 AP  
CLRWR

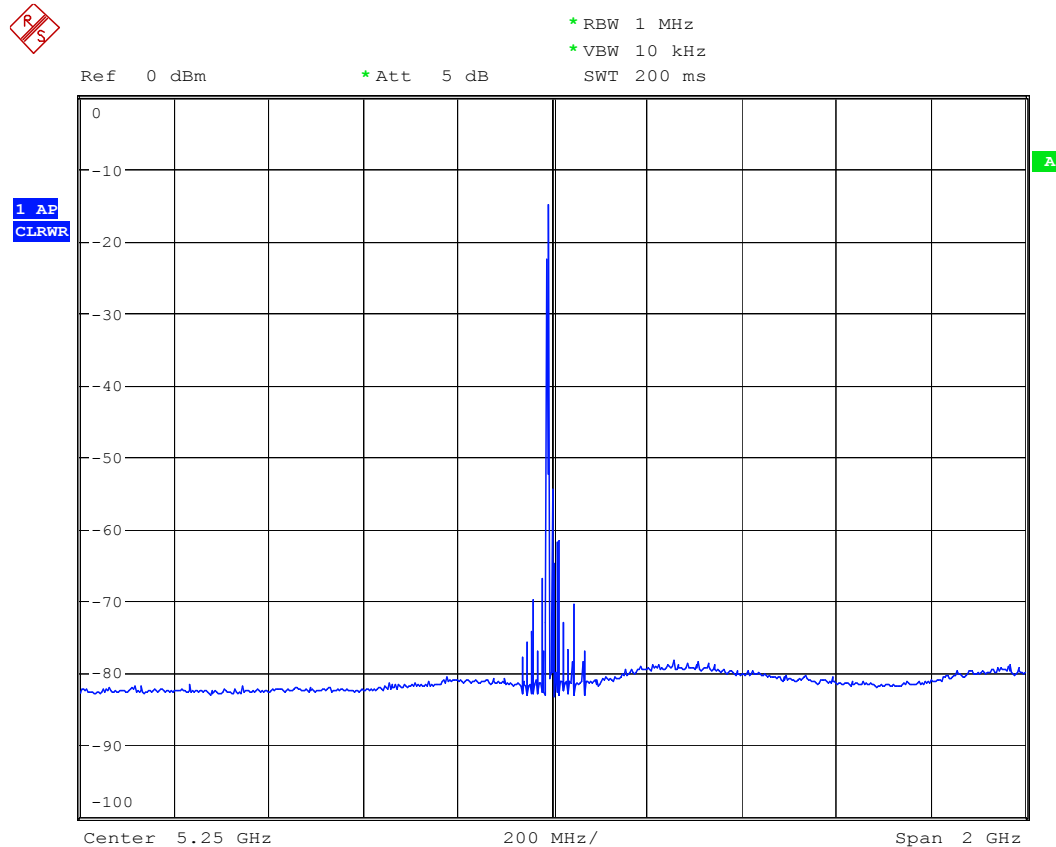


Center 5.25 GHz

20 MHz/

Span 200 MHz

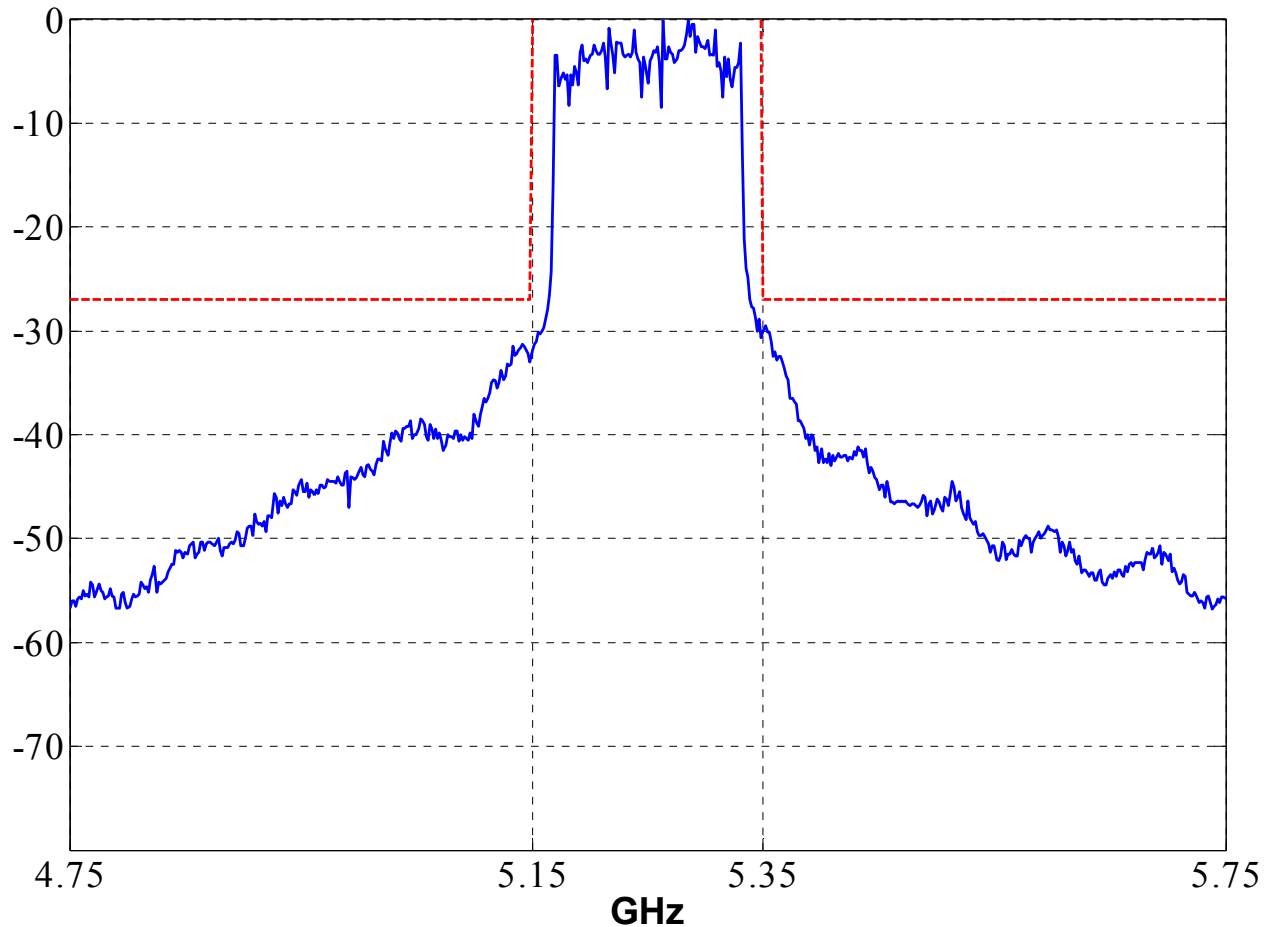
# Wideband Plot



- **Wideband Plot reveals no spurious signals or quantization noise outside the signal band, showing effectiveness of filter.**

# 160 Channel 256-QAM OFDM Signal

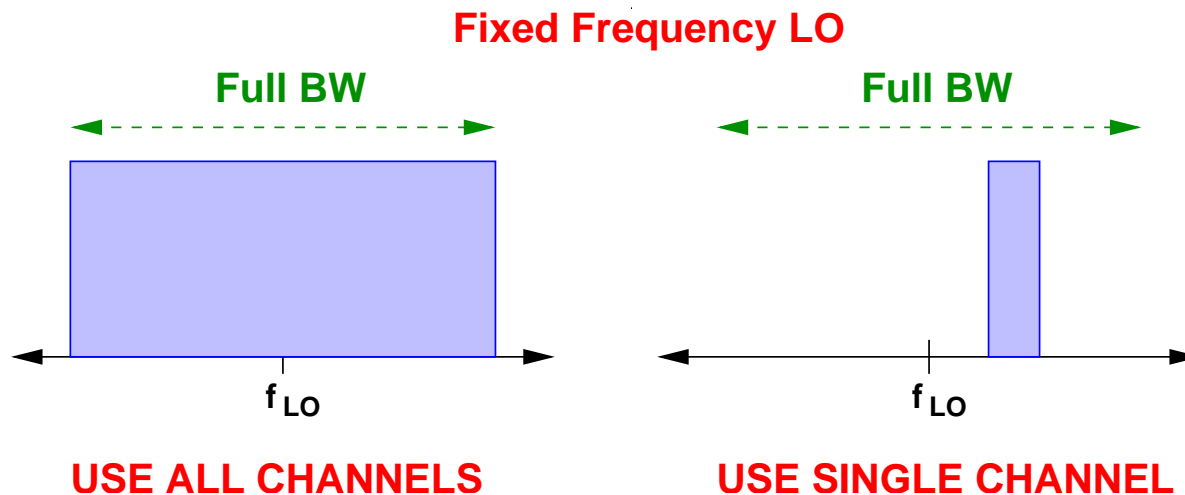
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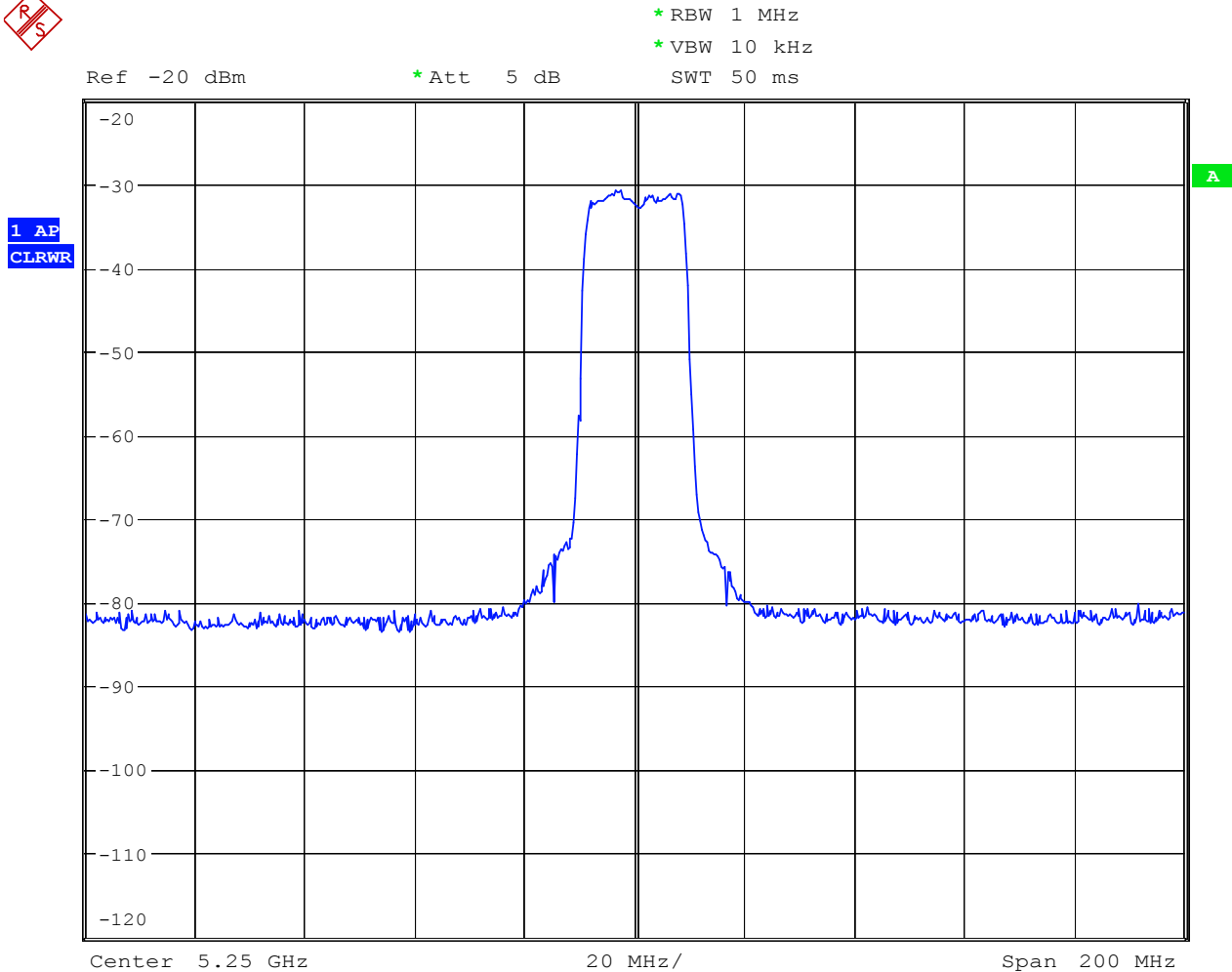
- **Maximum Data Rate = 1.28 Gb/s**
- **EVM ~ 30 dB**

# Wideband Digital Transmitter

- **Wideband Software-Defined Digital Modulation**
  - Flexible channel bandwidth, channel usage, and modulation scheme depending on channel conditions
  - Can perform channel selection in digital baseband instead of PLL



# 802.11a Compliant Transmitter



# Performance Summary

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<b>Performance Metric</b>	
<b>RF Output Frequency</b>	<b>5.25 GHz</b>
<b>RF Bandwidth</b>	<b>200 MHz</b>
<b>LO Feedthrough</b>	<b>-58 dBc</b>
<b>Image Rejection</b>	<b>No in-band image</b>
<b>HD3</b>	<b>-52 dBc</b>
<b>SNDR</b>	<b>49 dB</b>
<b>Maximum Data Rate</b>	<b>1.28 Gb/s</b>

# Modulator Power/Area

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	<b>Power (mW)</b>	<b>Area (mm<sup>2</sup>)</b>
<b>Quadrature DRFC Core</b>	<b>10</b>	<b>0.03</b>
<b>QDRFC Data/CLK Buffers</b>	<b>33</b>	<b>included in DRFC core</b>
<b>4<sup>th</sup> Order BPF</b>	<b>0</b>	<b>0.2</b>
<b>BFF Auto-Tuning Circuitry</b>	<b>4</b>	<b>0.12</b>
<b>LO Polyphase/Buffers</b>	<b>20</b>	<b>0.21</b>
<b>Digital Block (I and Q)</b>	<b>120</b>	<b>0.16</b>
<b>TOTAL :</b>	<b>187</b>	<b>0.72</b>

# FOM Comparison

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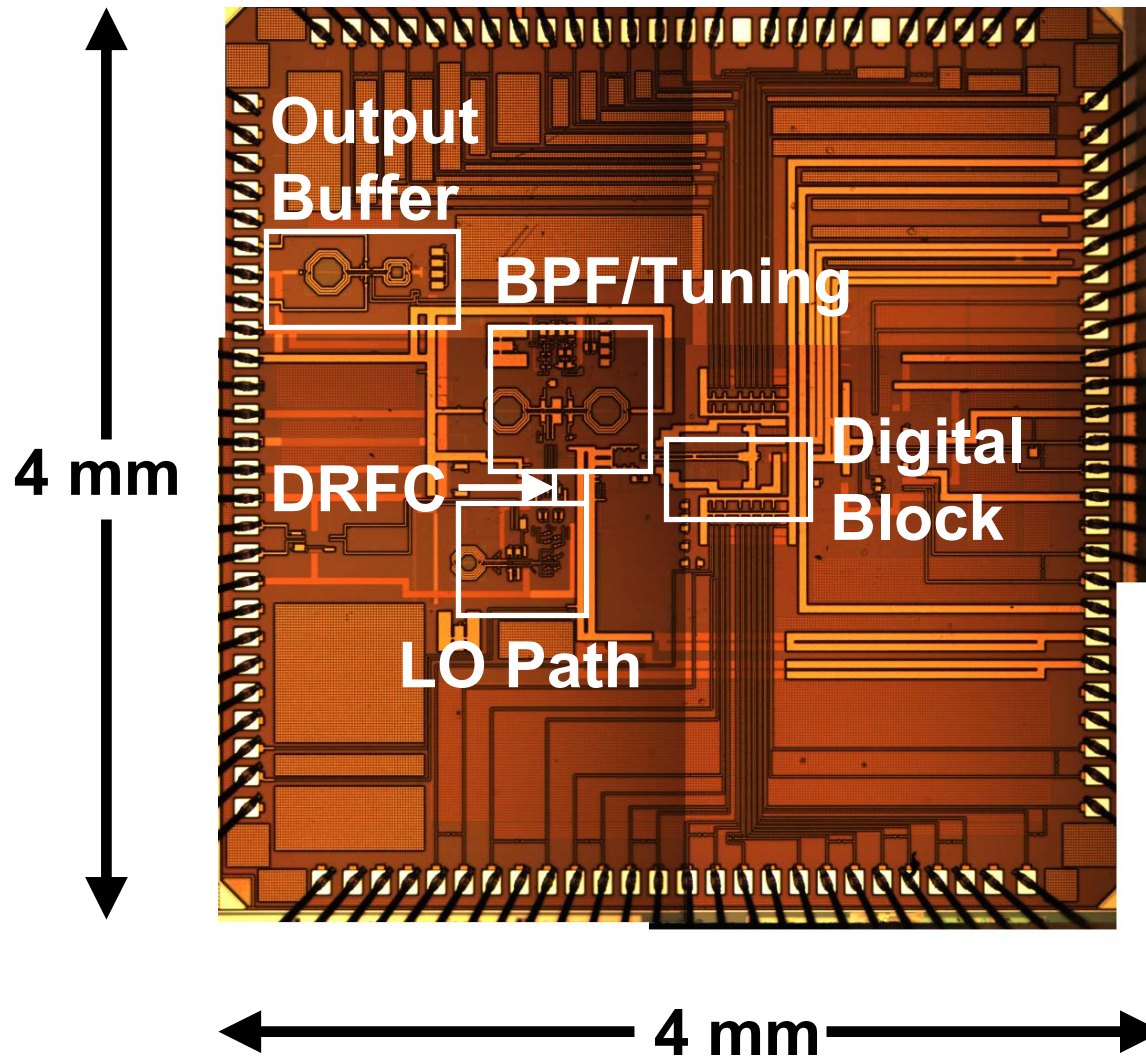
- A metric that defines the energy/bit efficiency of an RF modulator is defined as

$$FOM = \frac{Power}{ENOB * BW} = \frac{187e-3}{7 * 200e6} = 0.13 \frac{nJ}{bit}$$

<b>Digital-RF Modulator</b>	<b>ENOB</b>	<b>BW</b>	<b>Power</b>	<b>FOM (nJ/bit)</b>
<b>Eloranta [2]</b>	<b>8</b>	<b>20 MHz</b>	<b>60 mW</b>	<b>0.375</b>
<b>Taleie [3]</b>	<b>11</b>	<b>15 MHz</b>	<b>122 mW</b>	<b>0.74</b>
<b>This Work</b>	<b>7</b>	<b>200 MHz</b>	<b>187 mW</b>	<b>0.13</b>

# Die Photo

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# Conclusion

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- **Demonstrated a power and area efficient, wideband  $\Delta\Sigma$  digital-RF modulator with 1.28 Gb/s data rate**
- **Eliminated spurs associated with direct digital-RF conversion through design of a high-Q, self-tuned, passive LC BPF**
- **$\Delta\Sigma$  Digital-RF modulator is amenable to digital CMOS scaling, and is software programmable**

# **Acknowledgements**

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**I'd like to thank my colleague Ken Tan for help  
with measuring EVM**

**IBM Microelectronics for chip fabrication**

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Integrated Circuits and Systems**

# References

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- [1] S. Luschas, R. Schreier, H.S. Lee, “Radio Frequency D/A Converter,” *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1462-1467, September 2004.
- [2] P. Eloranta, and P. Seppinen, “Direct Digital-RF Modulator IC in 0.13  $\mu\text{m}$  CMOS for Wide-Band Multi-Radio Applications,” in *ISSCC Dig. Tech. Papers*, pp. 532-533, Feb. 2005.
- [3] S. Taleie, T. Copani, B. Bakkaloglu, S. Kiaei, “A Bandpass  $\Delta\Sigma$  RF-DAC with Embedded FIR Reconstruction Filter ,” *ISSCC Dig. Tech. Papers*, pp. 578-579, Feb. 2006.