

Embedded Super Computing Technology for Low-power Multimedia Application

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Outline

- Background**
- Proposed Processor Architecture**
- Software Interface and Benchmarks**
- Applications**
- Summary**

Background

- ❑ Digital multimedia systems are being built on SoCs.
 - Digital consumer electronics
 - ❑ (Image / Audio processing for DSC, Cellular phone, etc)
 - ITS (Intelligent Transport Systems)
 - ❑ High-level Image Recognition

Digital Consumer



Multimedia Processing

ITS

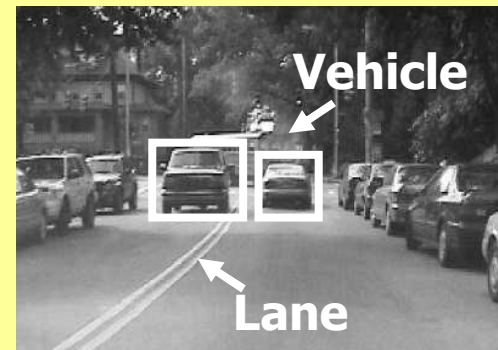


Image Recognition

Technical Issues (I)

These applications require

- High performance
- Low power consumption
- Small silicon area

to satisfy severe Performance / Cost demands.

Therefore,

Dedicated hardwired IPs have been employed to meet these requirements.

Technical Issues (II)

However, algorithms advance much faster than SoC's manufacturing cycle.

Ex.) Image Recognition Application

- Face Detection
- Vehicle / Lane Detection
- Object Tracking

Therefore, software solutions are indispensable.

Problem:

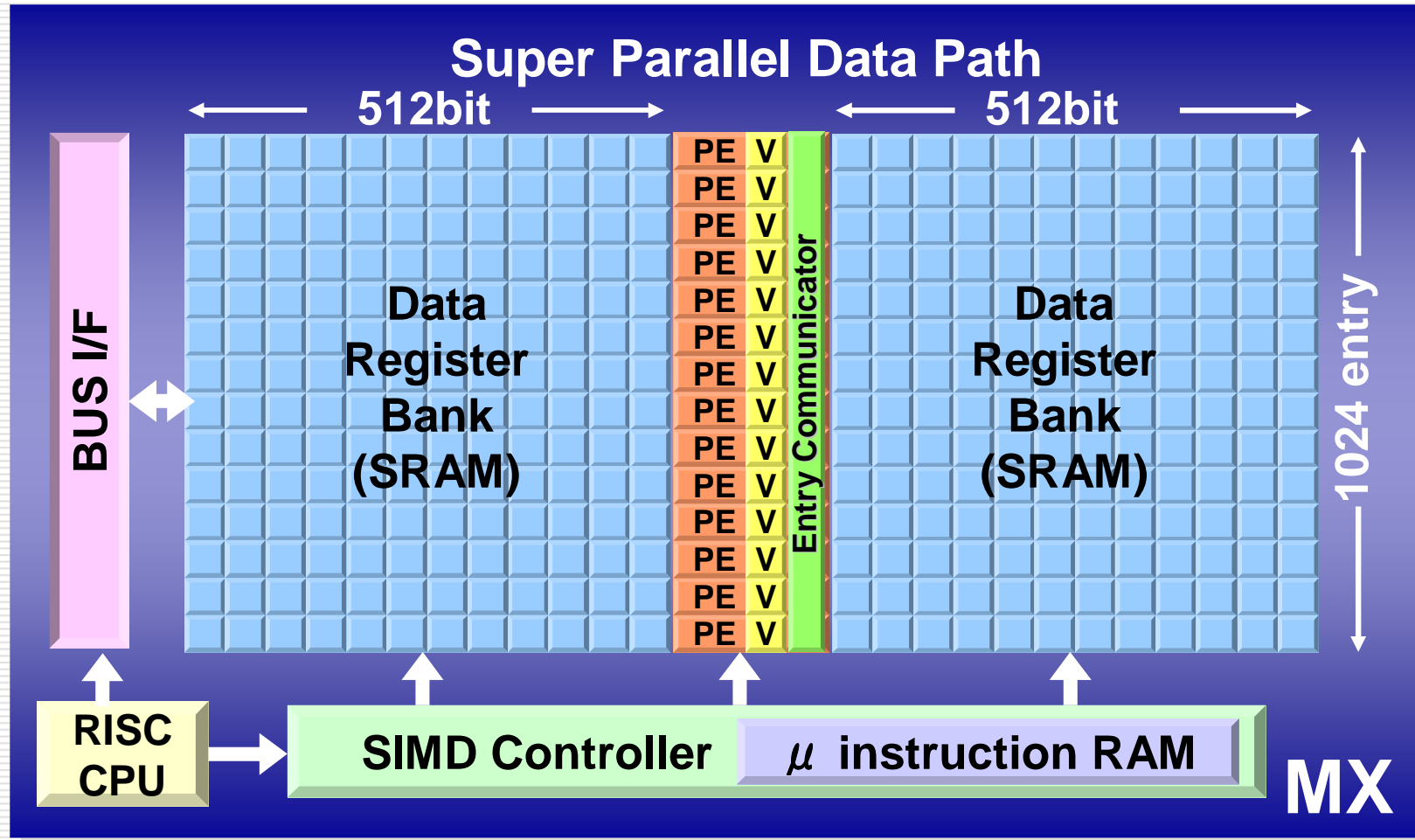
How can we enhance the performance of SoC while maintaining the programming flexibility?

Our Approaches

- **Super parallel and fine-grained SIMD data path structure**
 - **To enhance the performance in maximum.**

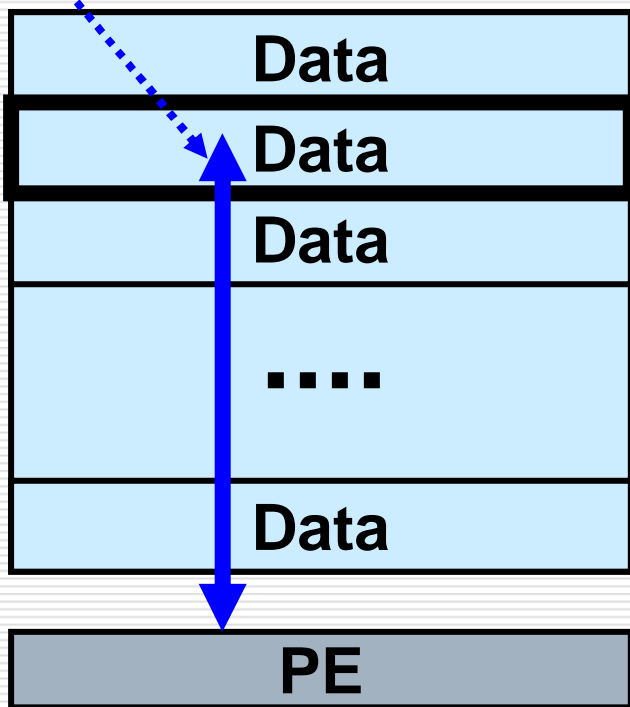
- **RISC CPU + dedicated SIMD controller**
 - **To realize the flexible programmability**

Hardware Architecture of MX processor



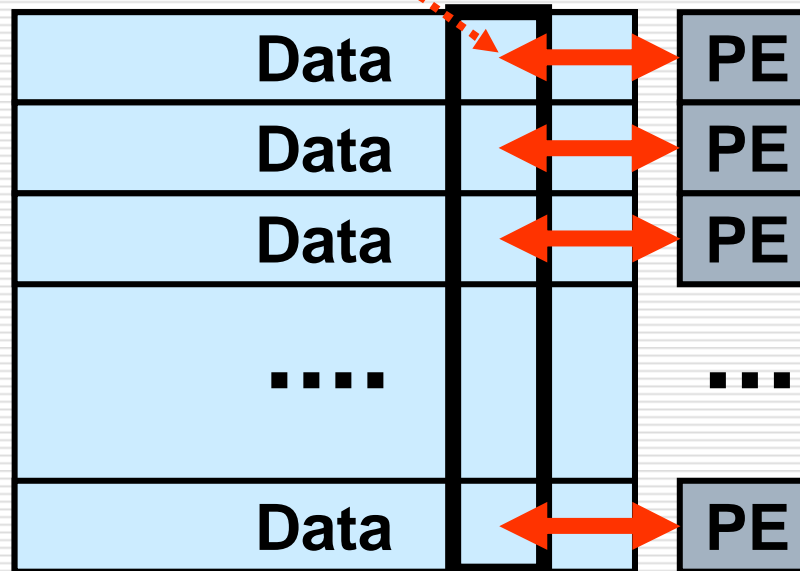
Concept of Data Processing in MX

Coarse-grained
data access



Conv. CPU/DSP

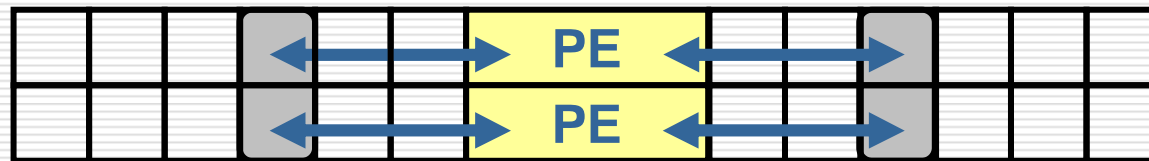
Fine-grained
data access



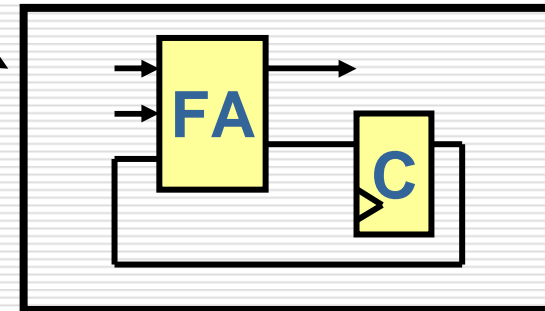
MX Processor
(this work)

Data path circuit design (I)

- “Logic in memory” design methodology
 - To enhance the area and the power efficiency



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(example) 1bit-grained PE

Problem:
What is the optimum structure for processor elements?

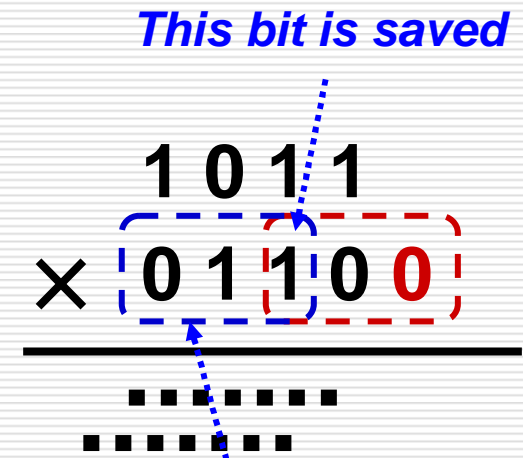
- ◆ 1bit-grained structure
 - Smallest, but slow in MAC (Multiply-Accumulate) operation.
- ◆ Coarse-grained structure
 - Fast MAC operation, but too large to be implemented.

Data path circuit design (II)

□ Applying the Booth's Algorithm

Radix-4 Booth's Table

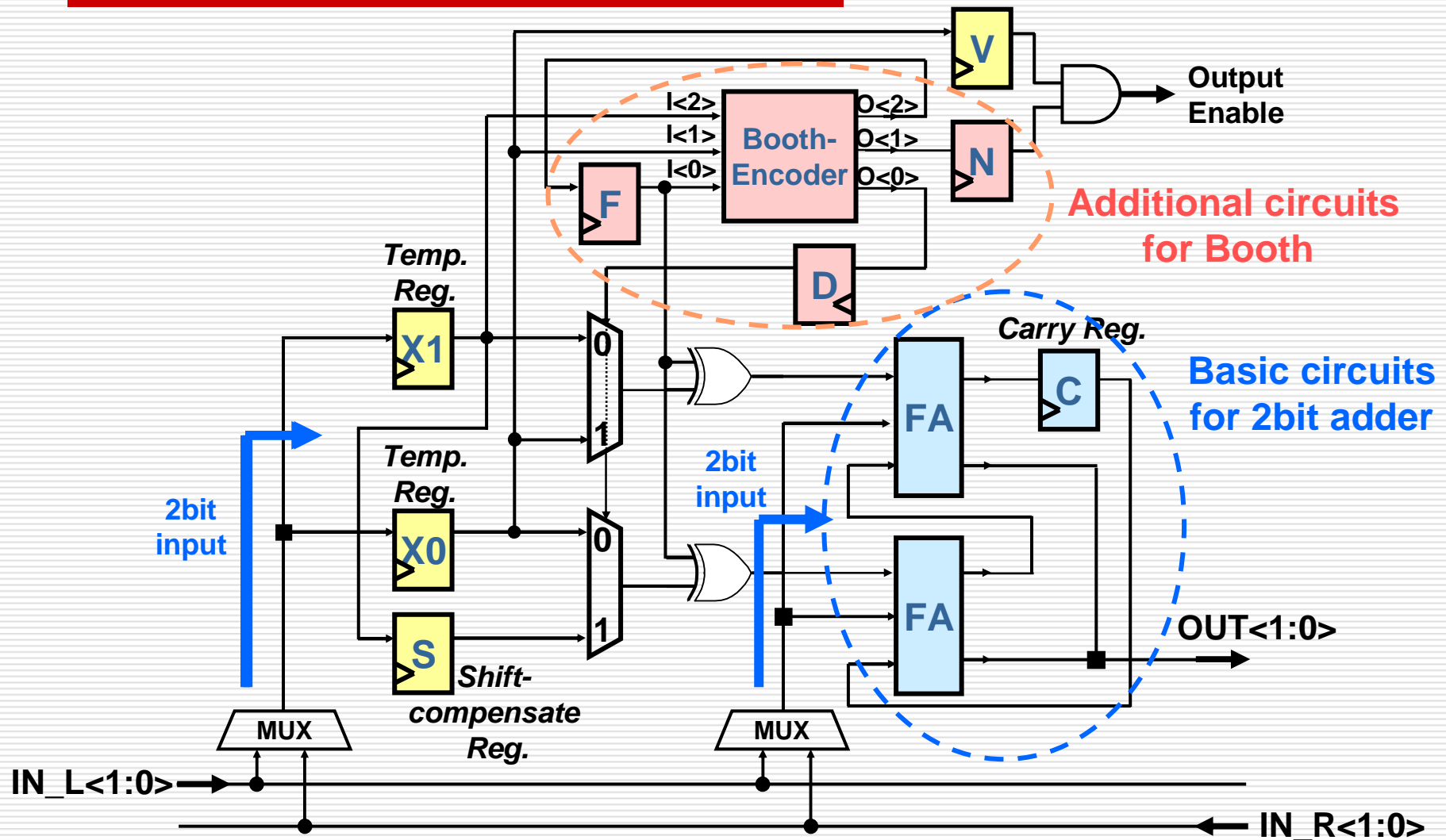
B [2i+1]	B [2i]	B [2i-1]	OP.	1-bit Shift	Invert	NOP
0	0	0	0			⊙
0	0	1	+A			
0	1	0	+A			
0	1	1	+2A	⊙		
1	0	0	-2A	⊙	⊙	
1	0	1	-A		⊙	
1	1	0	-A		⊙	
1	1	1	0		⊙	⊙



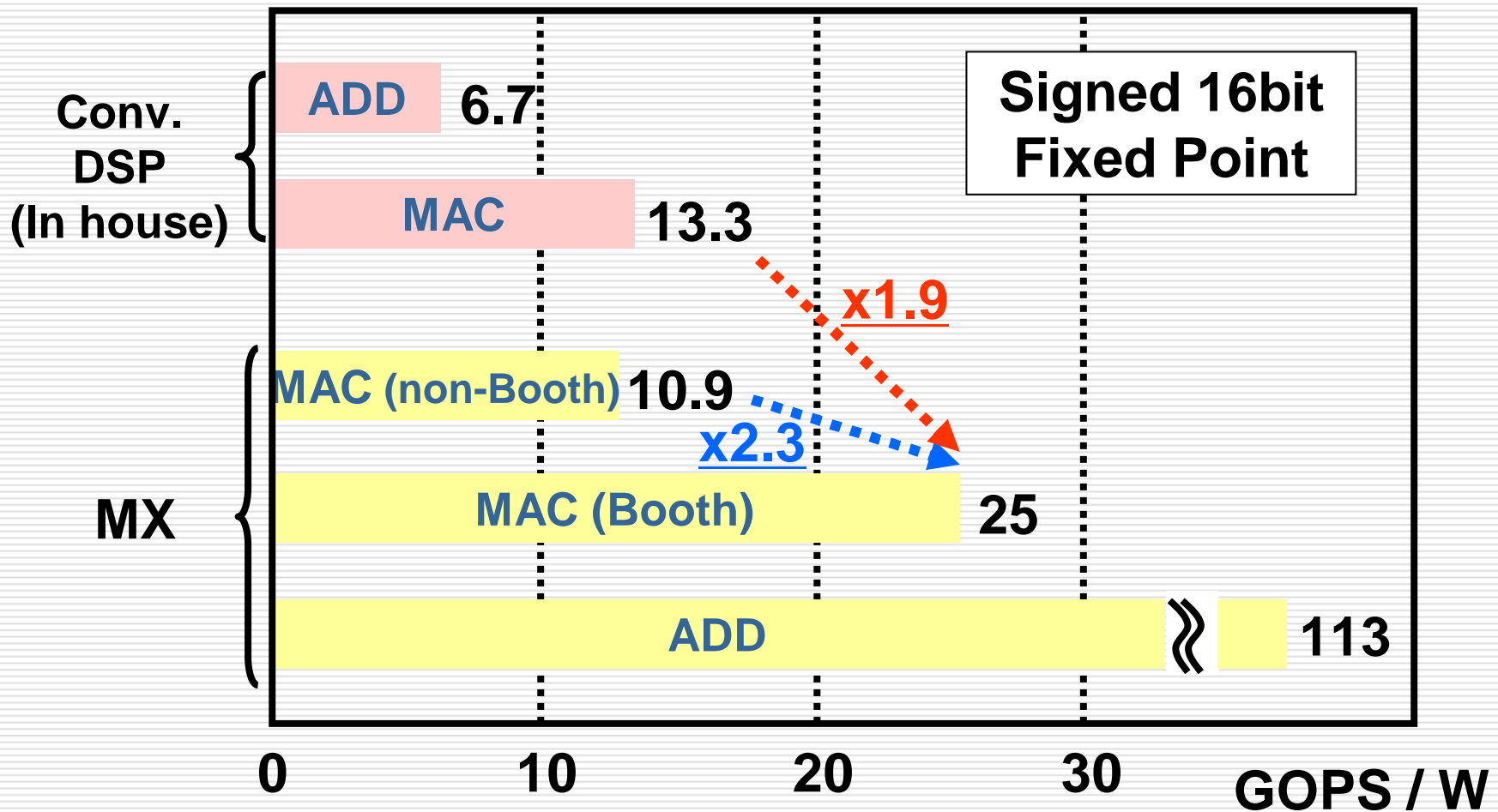
2bits are newly inputted

2bits-grained structure realizes both *small area* and *fast MAC operation*.

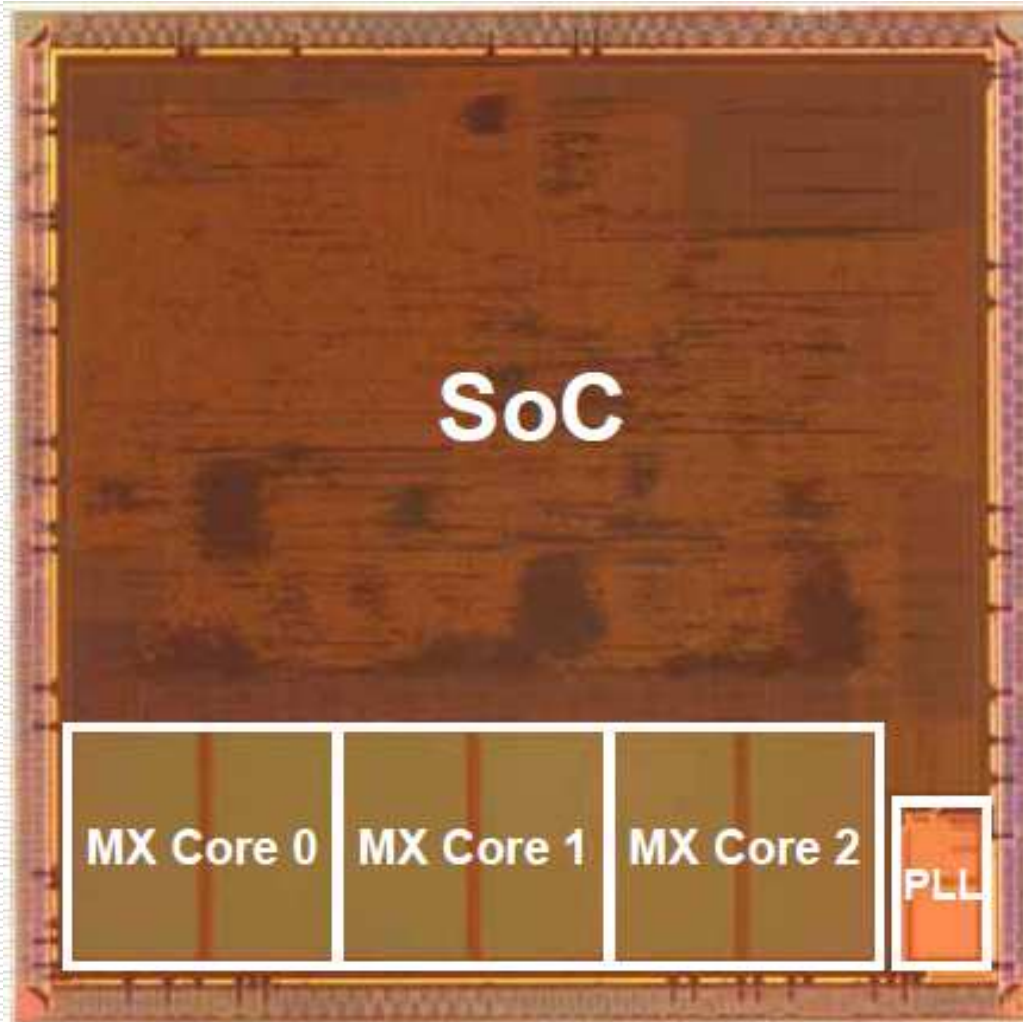
Data path circuit design (III)



Performance Comparison



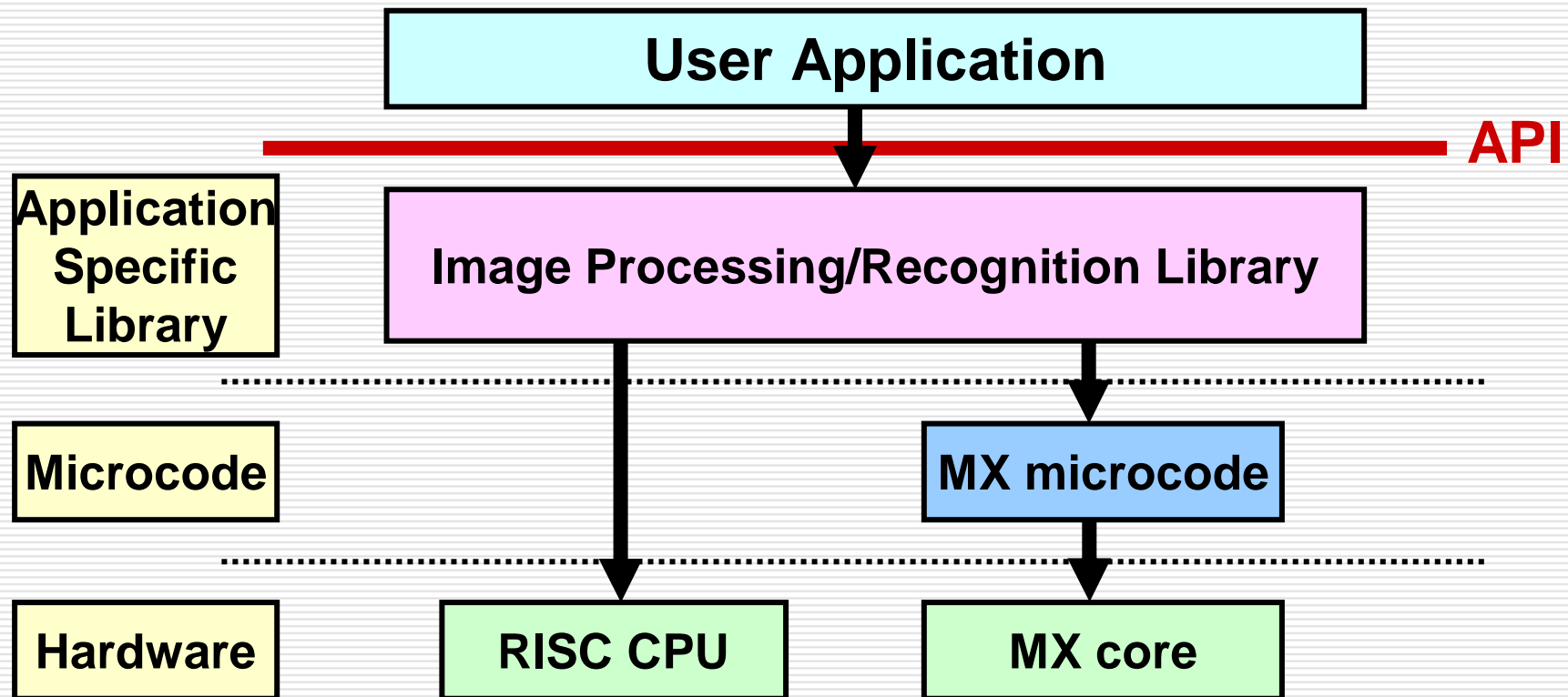
Chip Micrograph



Process	90nm 7Cu CMOS Low Standby
Chip Size	6.20mm*6.20mm
MX-Core Size	2.26mm²/core
Frequency	166MHz
MX-Core Power	150mW
Module	32bit RISC CPU, Camera I/F, Display cont. , etc

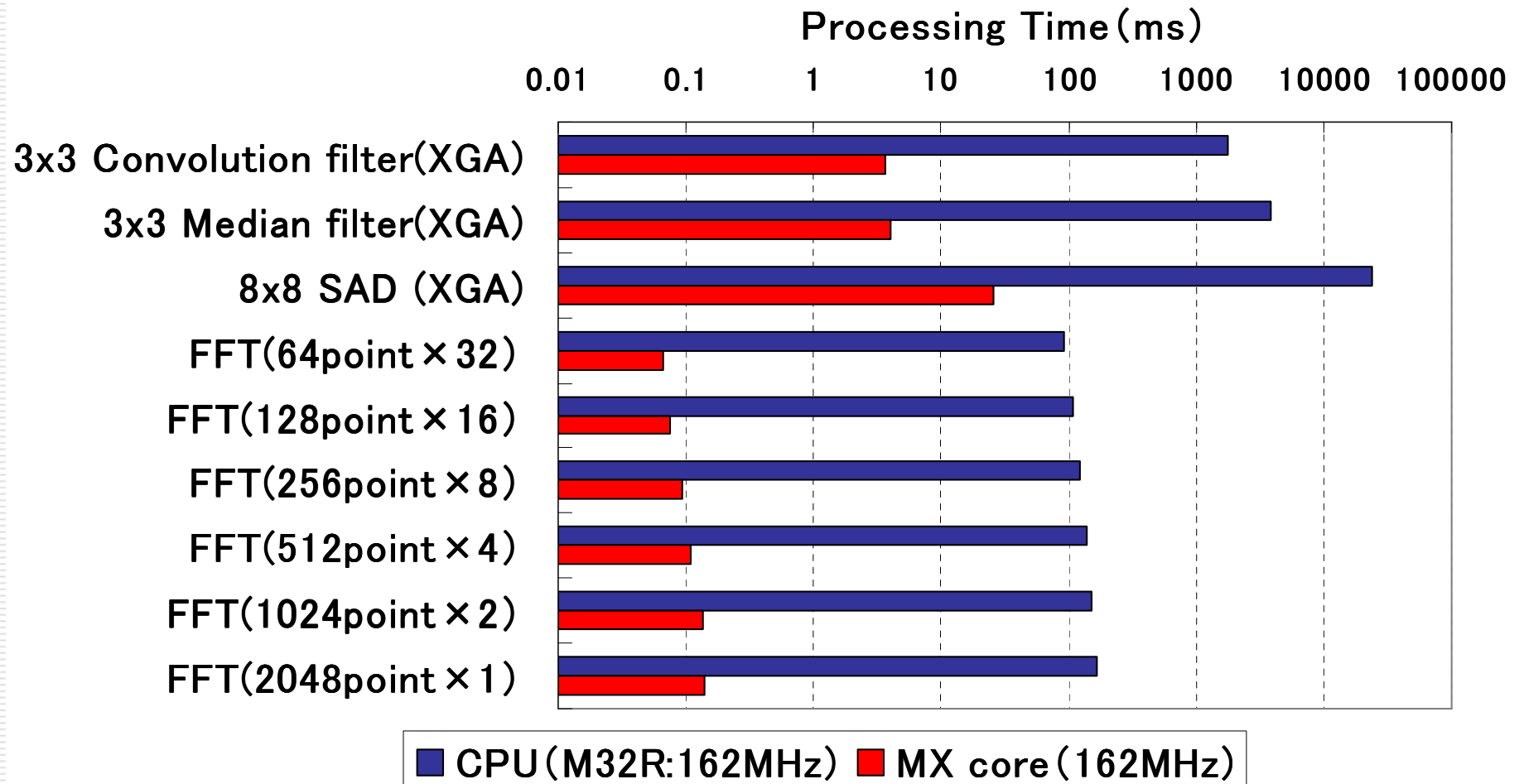
August 5th, 2008

Software Interface



Specific library layer conceals the super parallel structure of MX core.

Library Benchmark



Data flows in SoC with MX cores

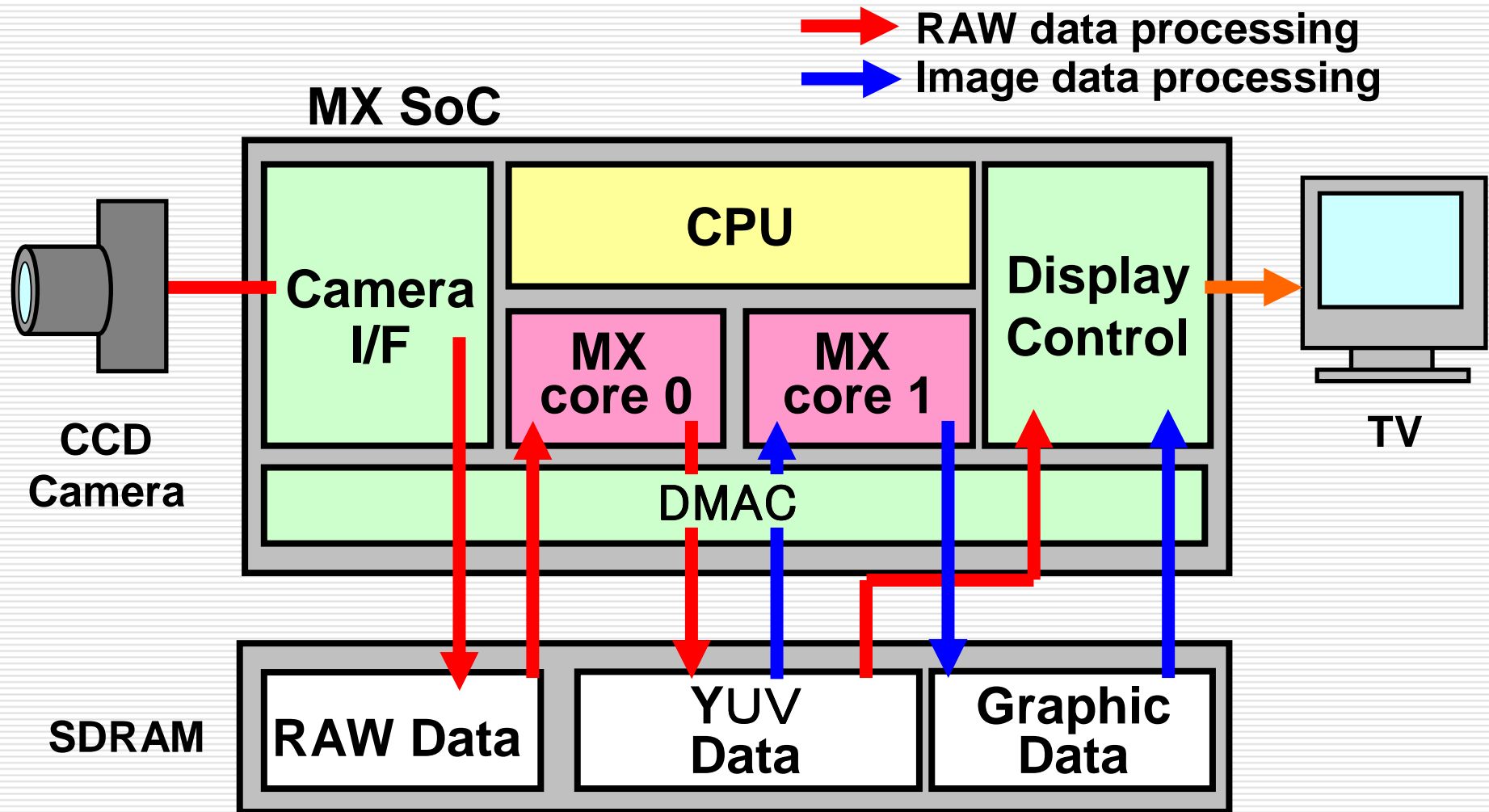


Image Processing Demo. (I)



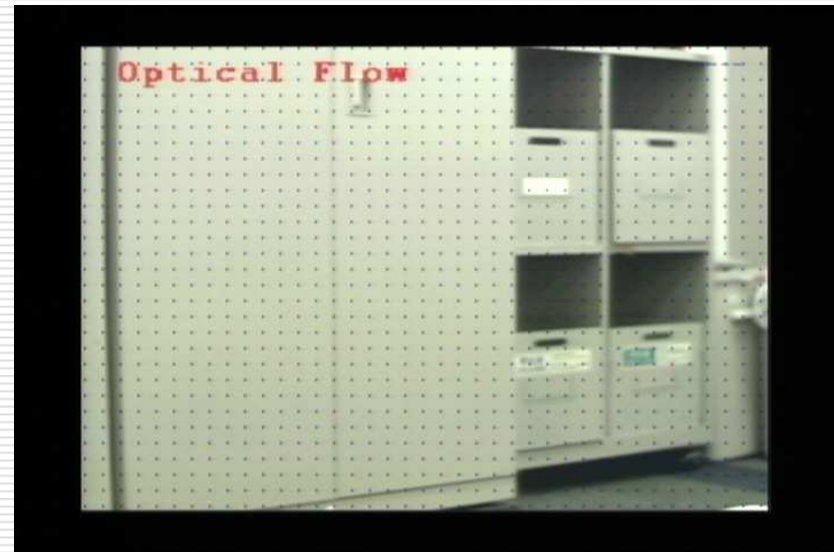
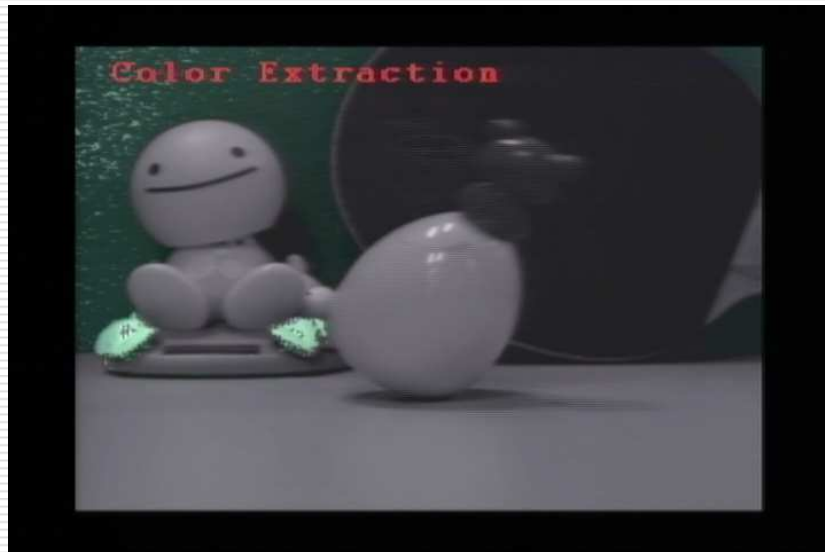
(a) by CPU



(b) by MX

CCD sensor signals are being processed to YUV data.

Image Processing Demo. (II)



Object Extraction with Color Motion Vector Extraction

**Additional algorithms are applied
to the processed image data.**

Summary

- ❑ **Embedded super parallel SIMD processor “MX” was introduced.**
 - **Hardware architecture**
 - ❑ **Unique super parallel fine-grained data path**
 - ❑ **Novel circuits for fast MAC operation**
 - ❑ **RISC CPU + dedicated controller**
 - **Software interface and Applications**
 - ❑ **Application specific library**
 - ❑ **Attractive applications in various fields**