Digital RF Synthesizing and Modulation: Toward Global Radio-TX for Multi-Standards Communication

Adil KOUKAB, and Michel DECLERCQ

adil.koukab@epfl.ch

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Outline

- Multi-Standard, Multi-mode Transceivers:
  - Motivation, Vision and Strategy
  - Polar Loop TX
- Multi Standards Carrier Generation System
  - Specifications and F. planning for GSM / WCDMA / WLAN
  - Architecture and Experimental results
- High Speed Digital Frequency Calibration
  - Motivation
    - RX/TX switching and Low-IF/Zero-IF reconfigurations
  - Architecture and Experimental results
- High Data Rate Phase/Frequency Modulation
  - Proposed Solution and Preliminary Results
- Conclusion

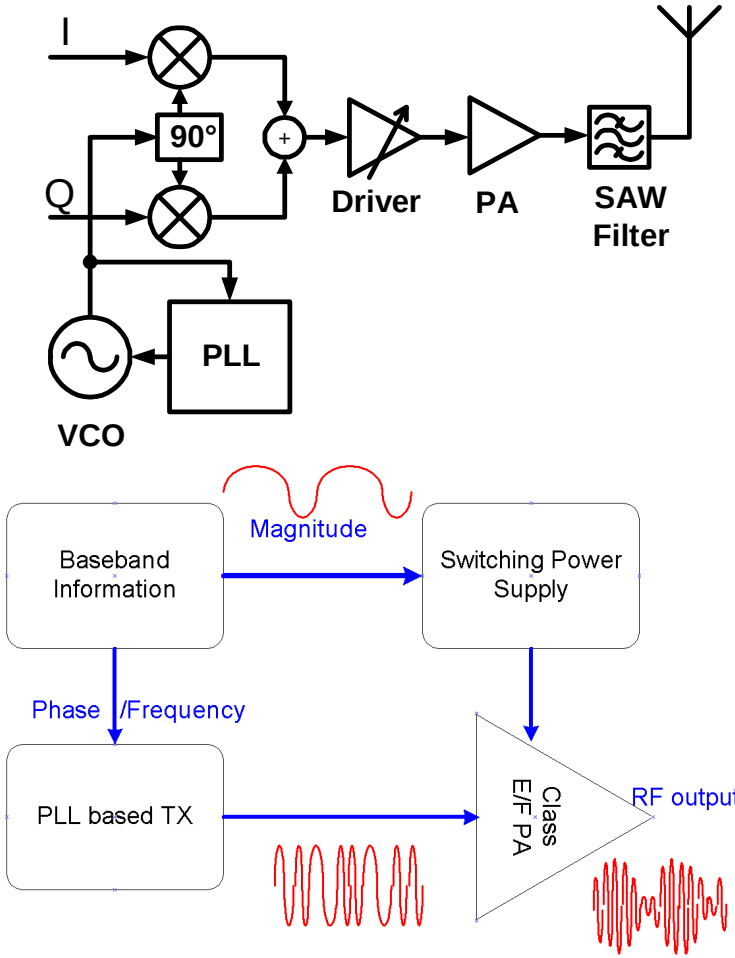
Motivation

- Global Mobility + Services Proliferation
  - Plethora of wireless networks “WPAN, WLAN, WMAN, WWAN”
  - Plethora of Standards, Specifications and Architectures
  - Multi-standards Convergence
  - Low Power/Cost/Area = Single Reconfigurable Hardware
- Strategy
  - More Simple / More Digital / Less Analog
  - Digital RF Proc with dig techno. :
    - Great flexibility in reconf. Radio
    - Relieve analog design complexity
    - Reduce cost power Cons.
    - Enable MS-SOC necessary in modern Hand. (Videos, TV, Camera)
- Focus and achievements

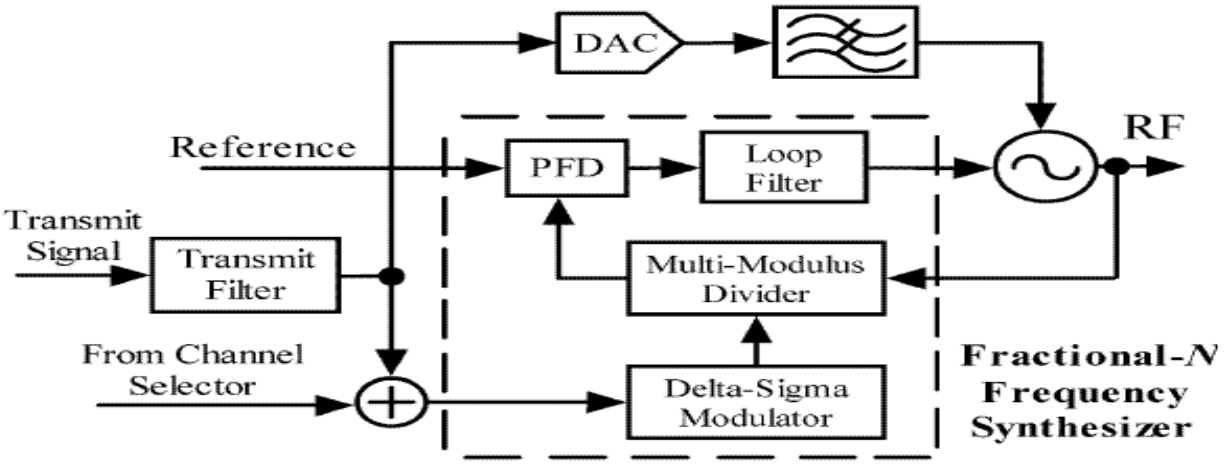
  Frequency Synthesizer / Polar Loop Transmitter

Polar loop TX

- Polar loop TX
  - Advantages
    - Envelope and phase information are separated in baseband (high accuracy/flexibility, easily reconfigured for Multi-Standard)
    - Saturated non-linear PA: High Efficiency
    - Take advantage of the inherent PLL filtering to reduce the noise and the harmonics
    - No pre- or post-PA filtering required to meet TX Noise in RX band
  - Drawbacks
    - Sensitivity to PVT,
    - Delay AM / PM paths
    - AM to PM in PA
    - DC offsets in the amplitude path
    - Spectral mask performance degraded by the bandwidth requirements of the AM and PM loops
  - Drawbacks exacerbated if analog AM/PM
  - Strong incentive for digital architecture solution

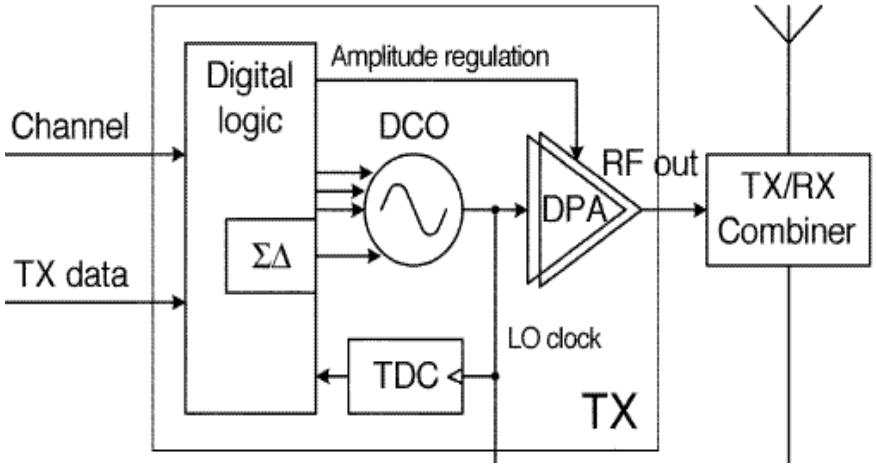


Phase / Frequency Modulator In Polar Loop TX



- Low cost/low power : Only PLL, One ADC (eventually), No Mixers, No RF filtering
- Open loop Modulator (wideband PM)
  - Frequency drift
- Closed loop modulator
  - Modulation by the Fractional-N divider
    - Conflict High data rate / Noise performance
    - Distortion due phase variation in the PLL transfer function (TypeII)
  - Two point Modulation VCO and divider
    - - - - Analog in nature, require a precise calibration of the VCO gain and a multi-bit D/A conv., Subject to process, temperature, and voltage variations (PVT).

Fully Digital Solution



R. B. Staszewski et al JSSC2005

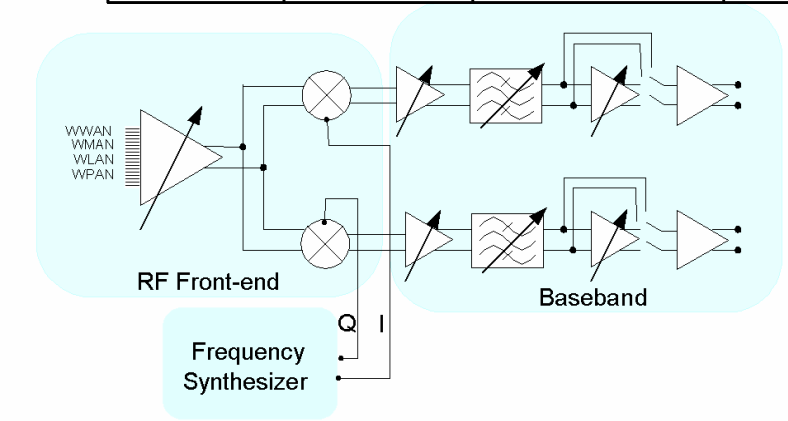
- All-digital PLL/PA:
  - Integ-track (64 bit, res~12KHz)
  - ΣΔ fract-track (3 bit res~39 Hz) (~ digital PM)
  - TDC measures Fref / DCO delay and correct F(DCO)
  - VCO gain estimation before each packet
  - Near-class-E digitally controlled PA (~digital AM)

- **Fully-digital two points modulation wideband PM/AM**
- **Validated for Bluetooth/GSM/GPRS/EDGE**
  - Digital tuning of the VCO is quite disturbing events
  - Sigma Delta dithering itself is a noisy process
  - Innovative solution was proposed to deal with these drawbacks
  - Huge complexity of digital control and high speed circuits (advanced MOS process)
  - Huge number of digital control bits control the RF (Incompatible with system in package or BiCMOS SiGe) .

Challenge for a Multi-Standards Extension

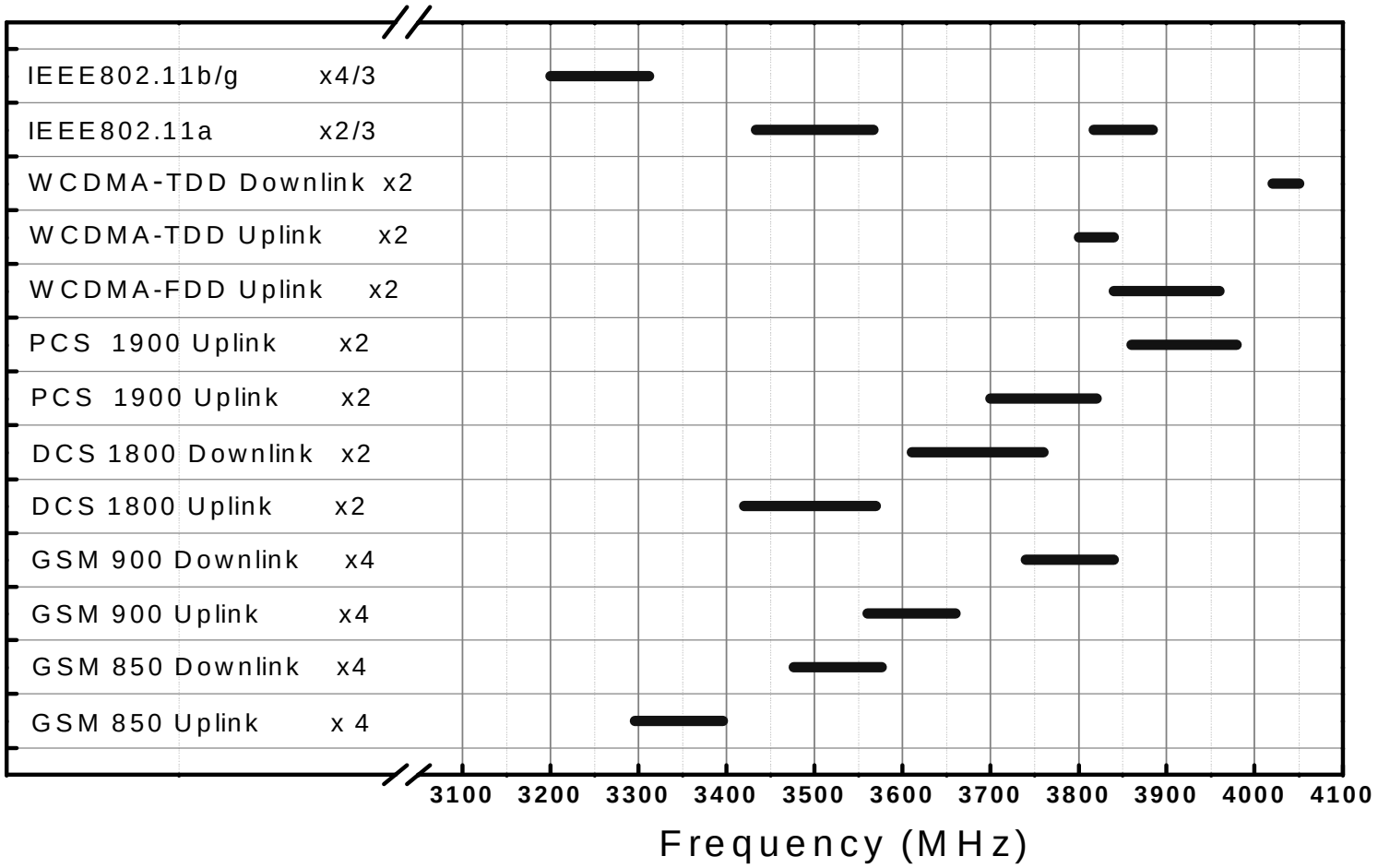
- GSM/UMTS/WLAN Frequency synthesizer

Standards		F[min-max] (MHz)	Channel (MHz)	PN (dBc/Hz)	Modulation	Suitable Architect.
GSM	850-900 DCS PCS	824-960 1710-1880 1850-1990	200KHz	RX:141@3MHz TX:-162@20MHz	GMSK	Z-IF L-IF
UMTS	FDD-TX TDD	1920-1980 1900-2025	5MHz	-120@3MHz -145@20MHz	QPSK	Z-IF
WLAN 802.11	a b g	5015-5850 2400-2484 2400-2484	16.6MHz 14MHz 14MHz	-102@1MHz	QPSK/QAM	Z-IF/L-IF Z-IF Z-IF

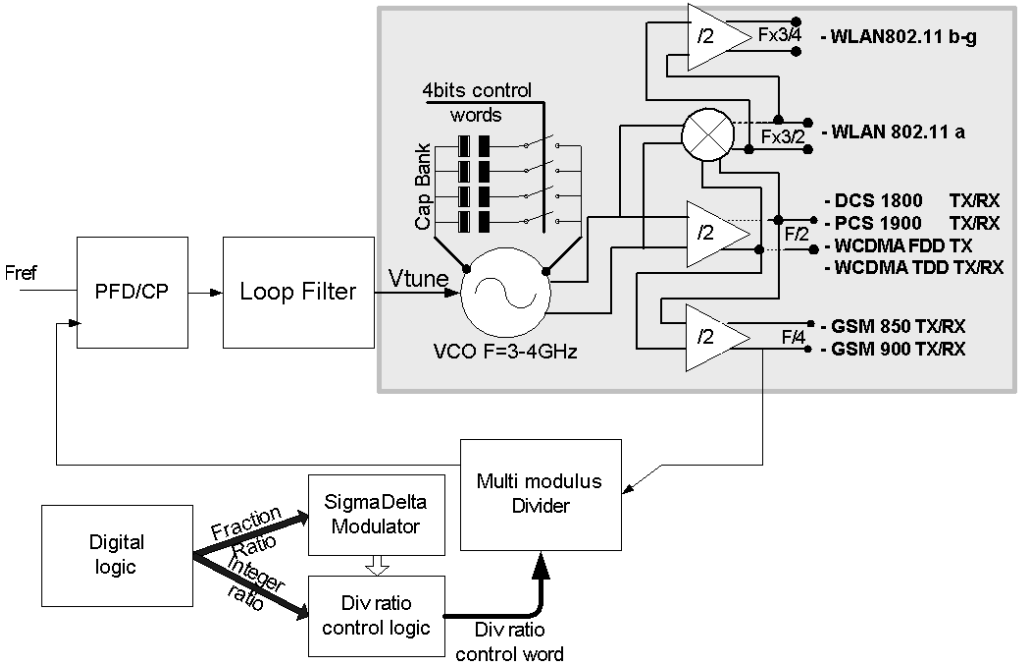


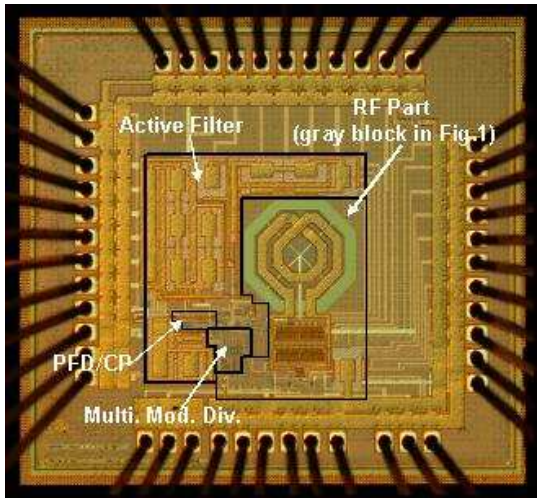
- Single Synthesizer Challenges:
  - Tuning range:5850-824x4=2554MHz
  - PN/RX: -141 dBc/Hz @3MHz
  - PN/TX: 162dBc/Hz@20MHz

Optimal frequency Planning



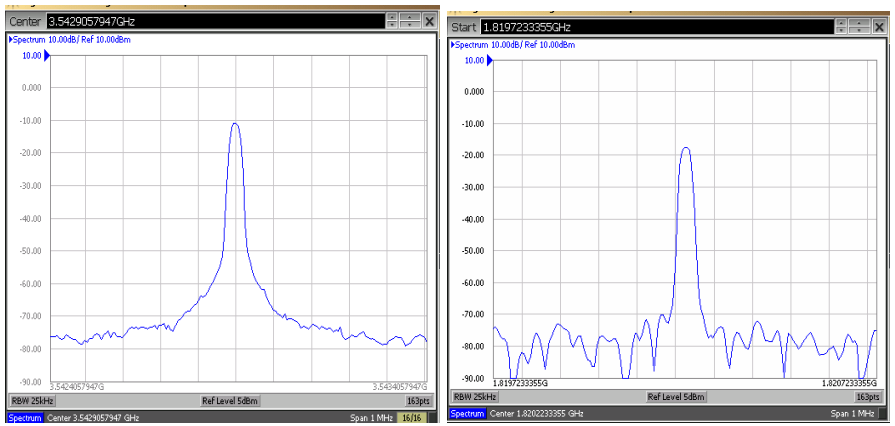
Multimode Frequency Synthesizer

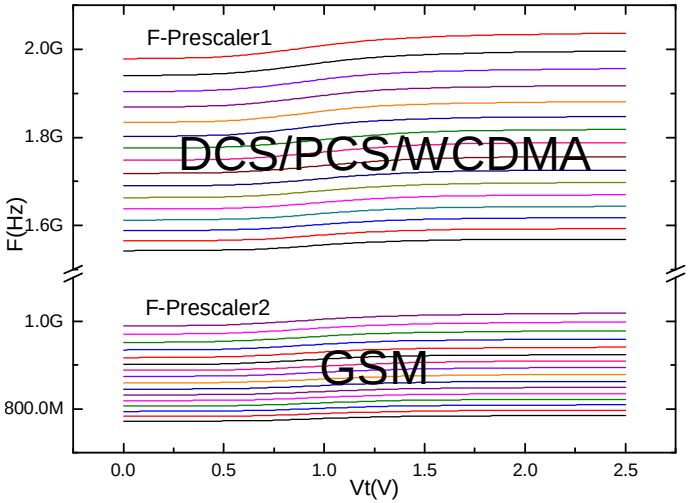


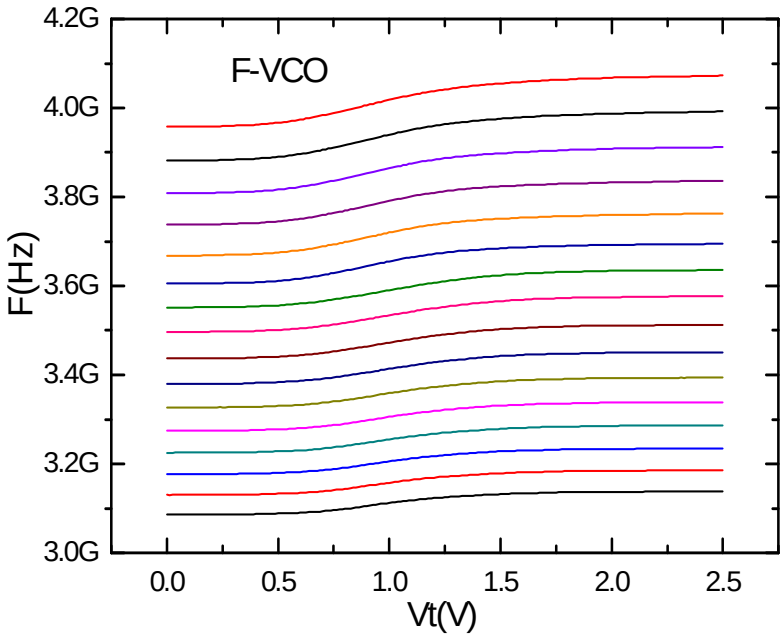


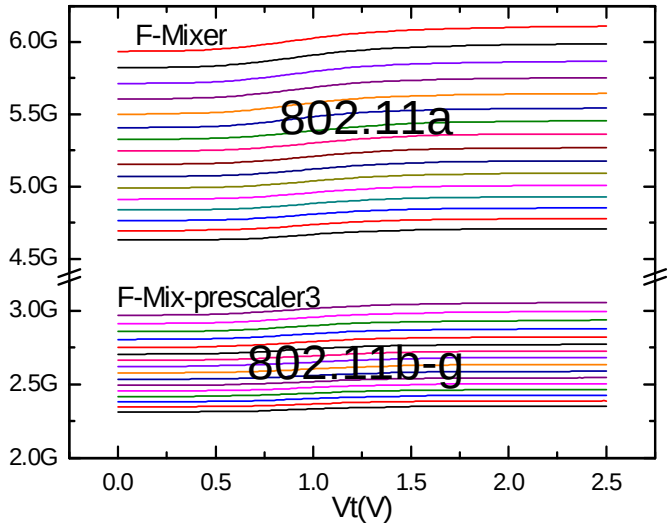
- A compact carrier generation: GPRS/GSM, WCDMA (FDD and TDD) and WLAN (802.11a/b/g) interoperability
- Process: 0.25um BiCMOS-SiGe

Experimental results (1)

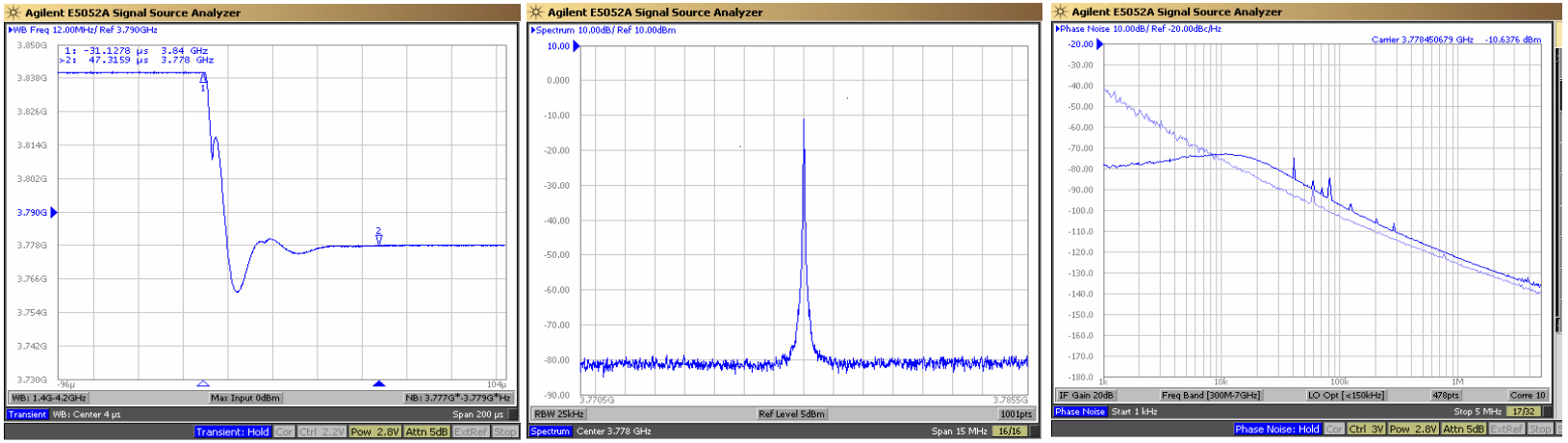






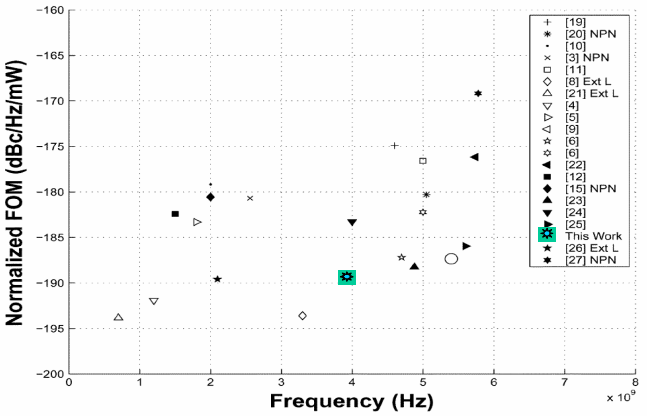


Experimental results (2)



$$NFOM = Ph(1MHz) - 20\log(F_c / \Delta F) + 10\log(P_{dis} / 1mW)$$
$$= -189 \text{ dBc/Hz/mW}$$

Frequency Offset	2.5mA@2.5V	1.7mA@2.5V
100 KHz	-104 dBc/Hz	-100 dBc/Hz
400 KHz	-118 dBc/Hz	-113 dBc/Hz
1MHz	-125 dBc/Hz	-119.5 dBc/Hz
3MHz	-135 dBc/Hz	-129 dBc/Hz
10MHz	-145 dBc/Hz	-139.5 dBc/Hz

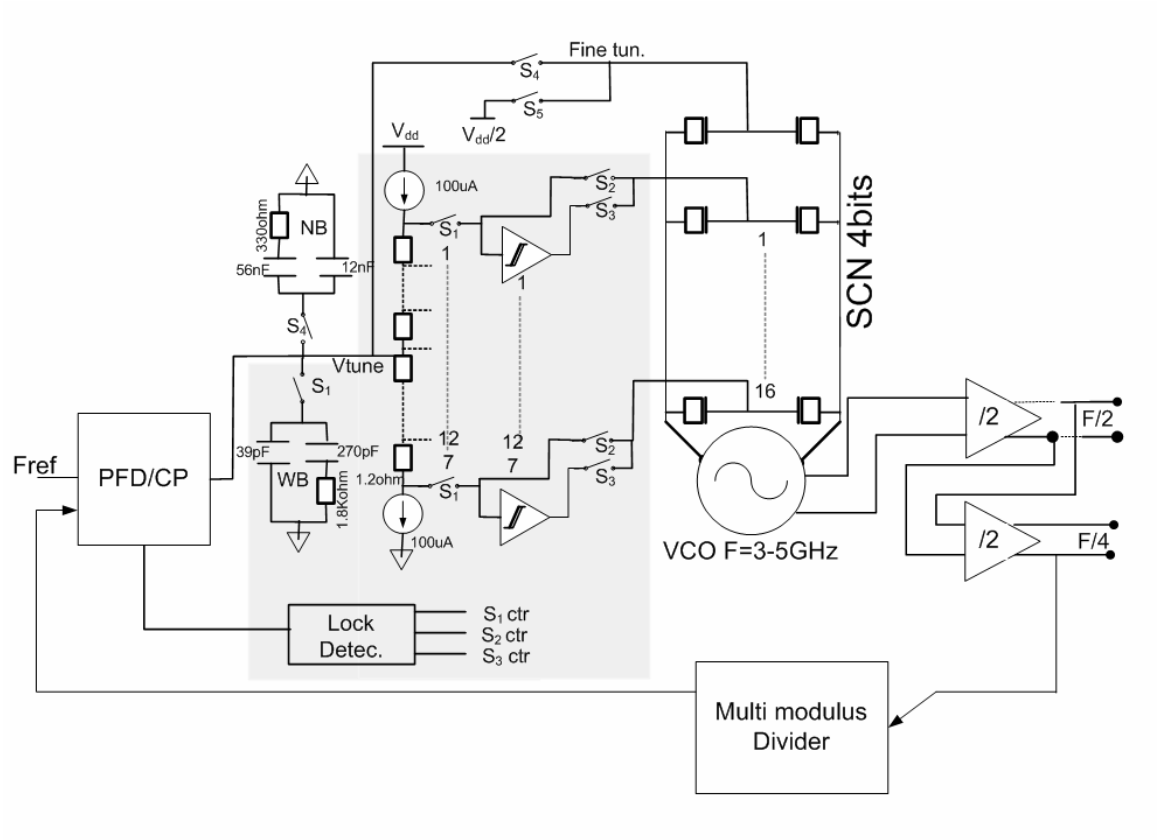


A. Jerng and C.G. Sodini JSSC2005

High Speed Digital Frequency Calibration

- EDGE RX/TX band switching
  - EDGE multi-slot technology imposes PLL RX/TX switching lower than 10 us
- Low-IF/Zero-IF reconfiguration
  - LIF-RX/ZIF-TX in 802.11.g-a need a very small settling time (e.g. < 16 us, the preamble of OFDM-WLAN)
- Classical Solution
  - Reconfigurable wide/narrow band PLL during the tuning operation
    - The glitch caused by the PLL bandwidth switching tend to limit the lock time improvement.
- Proposed Solution: ADFC

System and Tuning Flowchart



- WB-CT: Band-with = 1MHz and Icp=1.6mA
  - -noise has no effect before the conversion
- NB-FT: Band-With = 20KHz and Icp= 0.8 mA

•WB-CT Mode
•S1, S2, S4, S5 on
•WB filter charged to Vdd/2

•Start WB-CT
•S4 off

•PLL Locked
•Lock detector on

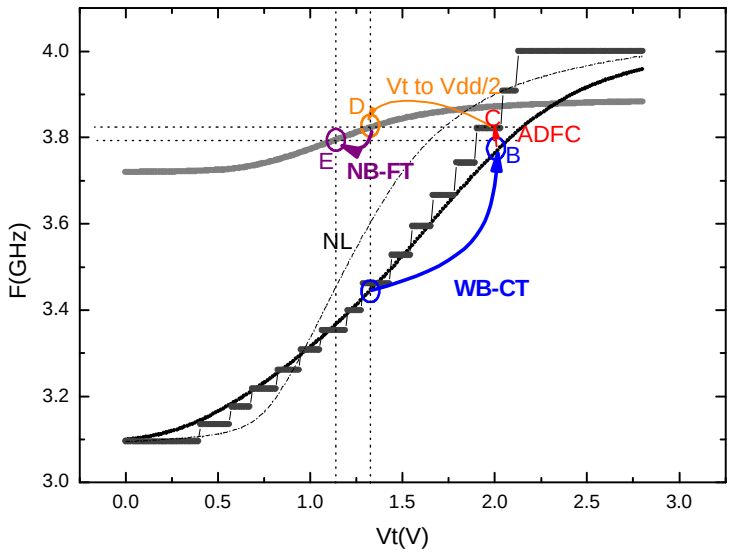
•S1 off, S3 on
•F digital Conversion

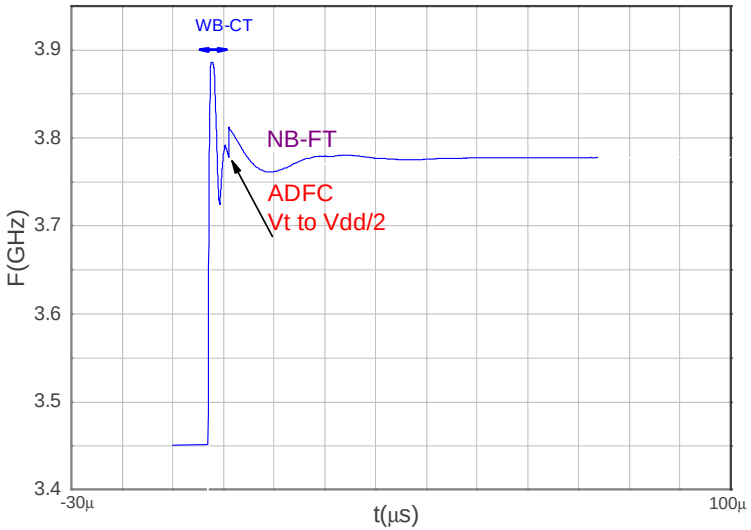
•NB-FT Mode
•S4 on
•NB filter charged to Vdd/2

•Start NB-CT
•S5 off

•PLL Locked
•END

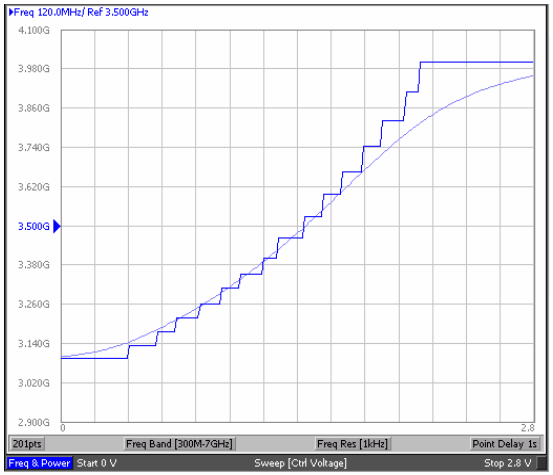
Results (simulation)

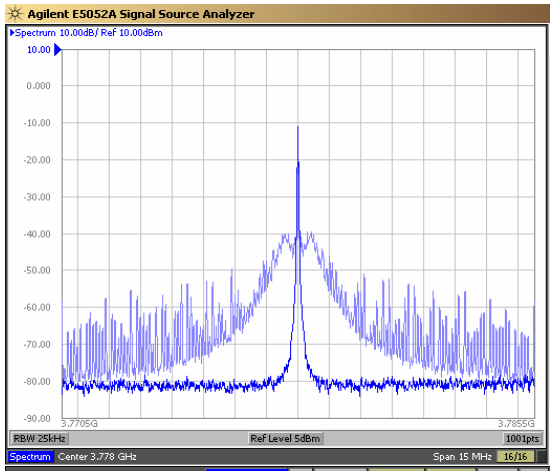


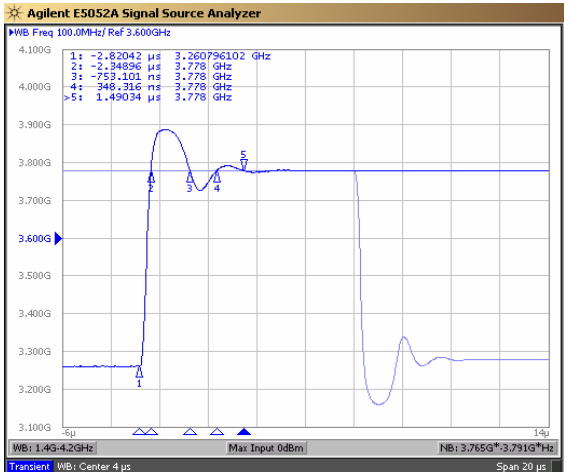


- High linear high speed WB-CT
- ADFC Quantization error very small except near Vdd
  - Nonlinearities at the borders
- Small Ferr compensated by NB-FT
  - Optimtized settling time
- NB normal operation / high noise performances

Results (measurements)



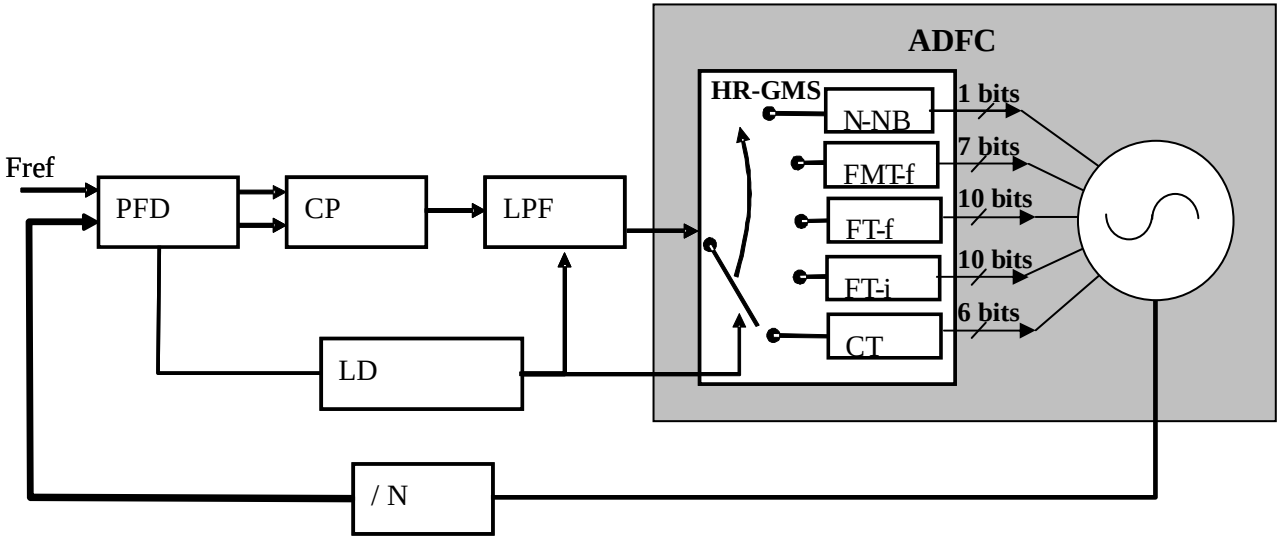




- High spectrum purity during normal operation (FOM=-189dBc/Hz/mW)
- High speed AFC: ts = around 3 to 5 us
- Independent Speed and noise optimization
- Highly promising for high data rate frequency modulation
  - Since Speed/noise PLL trade-off was the principal limitation.

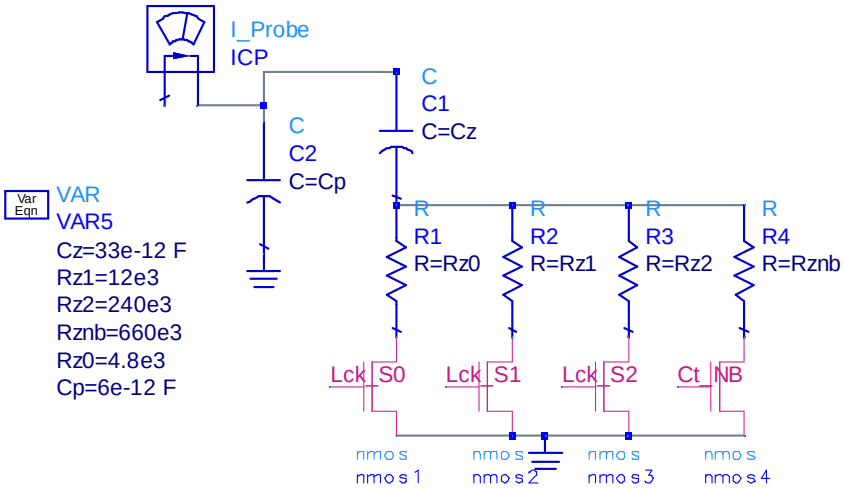
From Synthesizing to Modulation

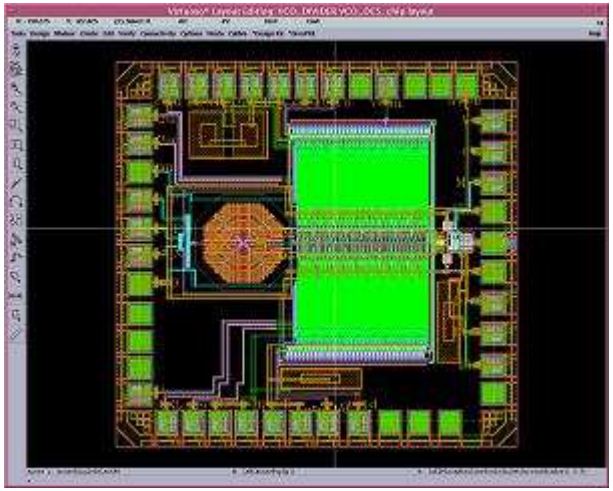
under development for Quad-GSM

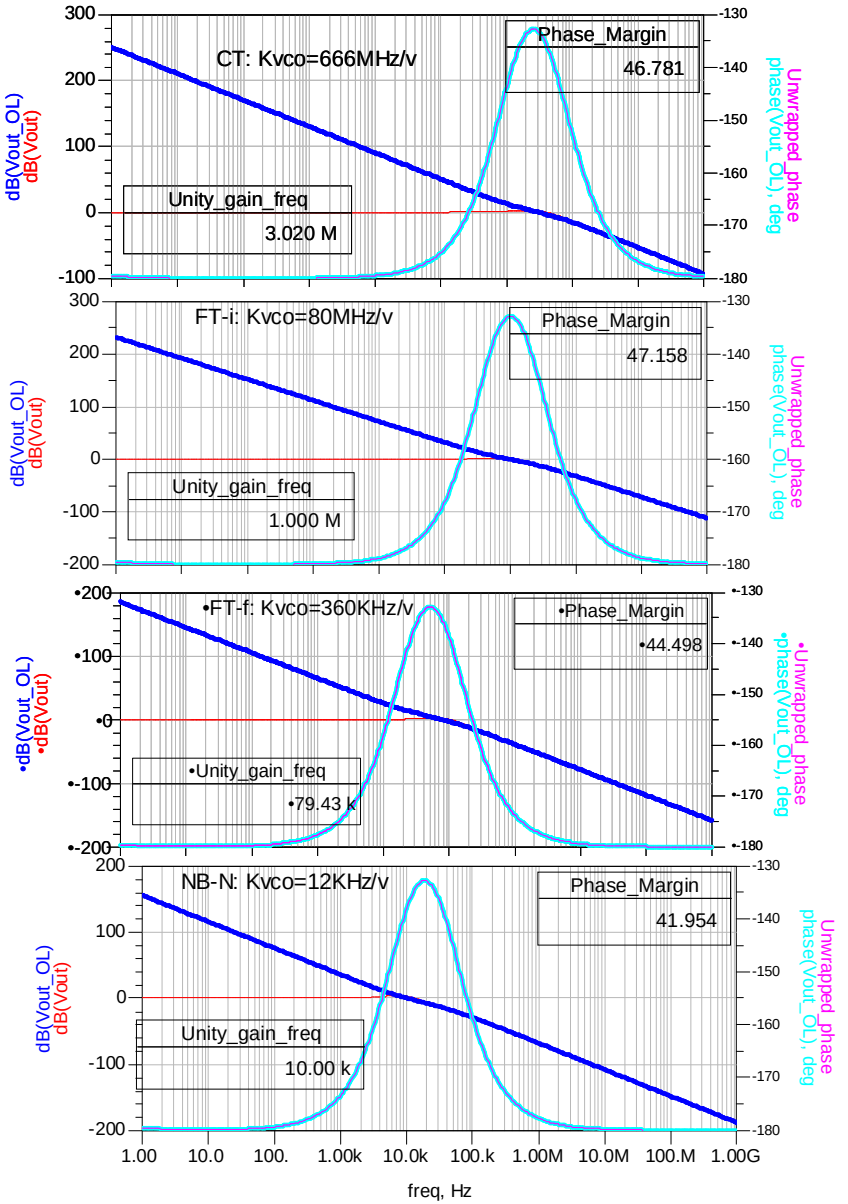


- **Principal challenge:**
  - **Extremely high resolution e.g. Tuning rang 1GH and final precision few 100Hz**
- **Frequency Planning:**
  - **Coarse tuning CT: 6 bits for Band selection; from 1 GHz to 15MHz)**
  - **Fine tuning integer FT-i: 10 bits for first Channel convergence; 180MHz to 180 KHz**
  - **Fine tuning fractional FT-f: 10 bits for final channel convergence; 400 KHz to 400 Hz (200Hz after prescaler)**
  - **Frequency Modulation tuning FMT-f: 7 bits for Capacitors array tuning for Modulation (2% précision)**

Filter, tuning ranges and PLL stability







Conclusion

- Ultimate objective:
  - A Compact Transceiver System For
    - GSM/GPRS/UMTS (FDD and TDD): for wide area coverage
    - WLAN (802.11a/b/g): for high data rate local coverage
  - Fully Digital Polar loop TX the best candidat
- A silicon implementation of a Carrier generation system fully compliant with quad-GSM, UMTS and WLAN standards was presented.
- ADFC technique overcomes Noise/Speed trade-off and enables ultra fast-low noise PLL
- Current developments: Wideband Frequency modulator based on ADFC technique