

Advances and Challenges in CMOS Imager Technology

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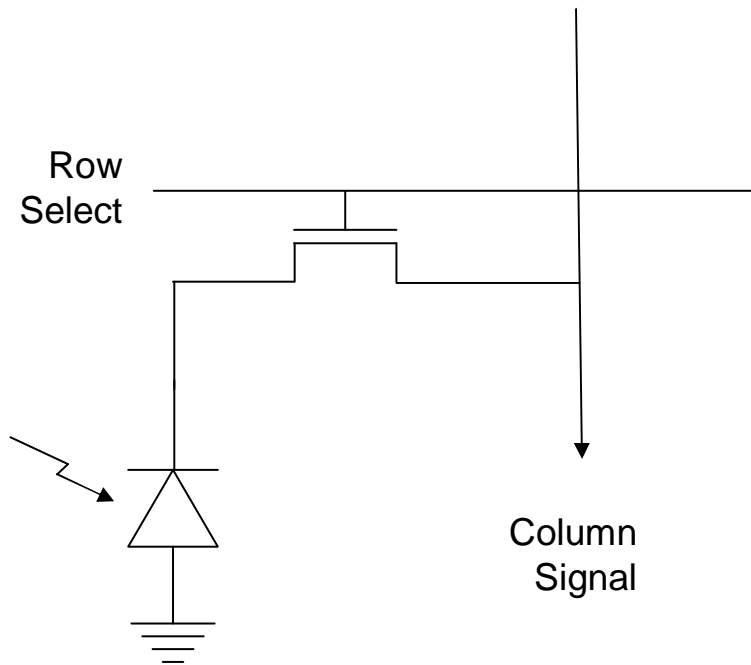
Introduction

- Historically CCDs have dominated the electronic imager market.
 - Excellent imaging quality
- CMOS imagers have been gaining market share and are now surpassing CCDs in volume
 - Integration
 - CCDs require external chips for timing generation, AtoD conversion, image processing, and multiple supply voltage generation. CMOS imagers require none of these.
 - Speed
 - CMOS imagers can be much faster
 - Functionality
 - CMOS imagers offer great flexibility in operation
 - Cost
 - Standard wafer processing and less support chips gives a lower cost overall solution

CMOS Imager Technology

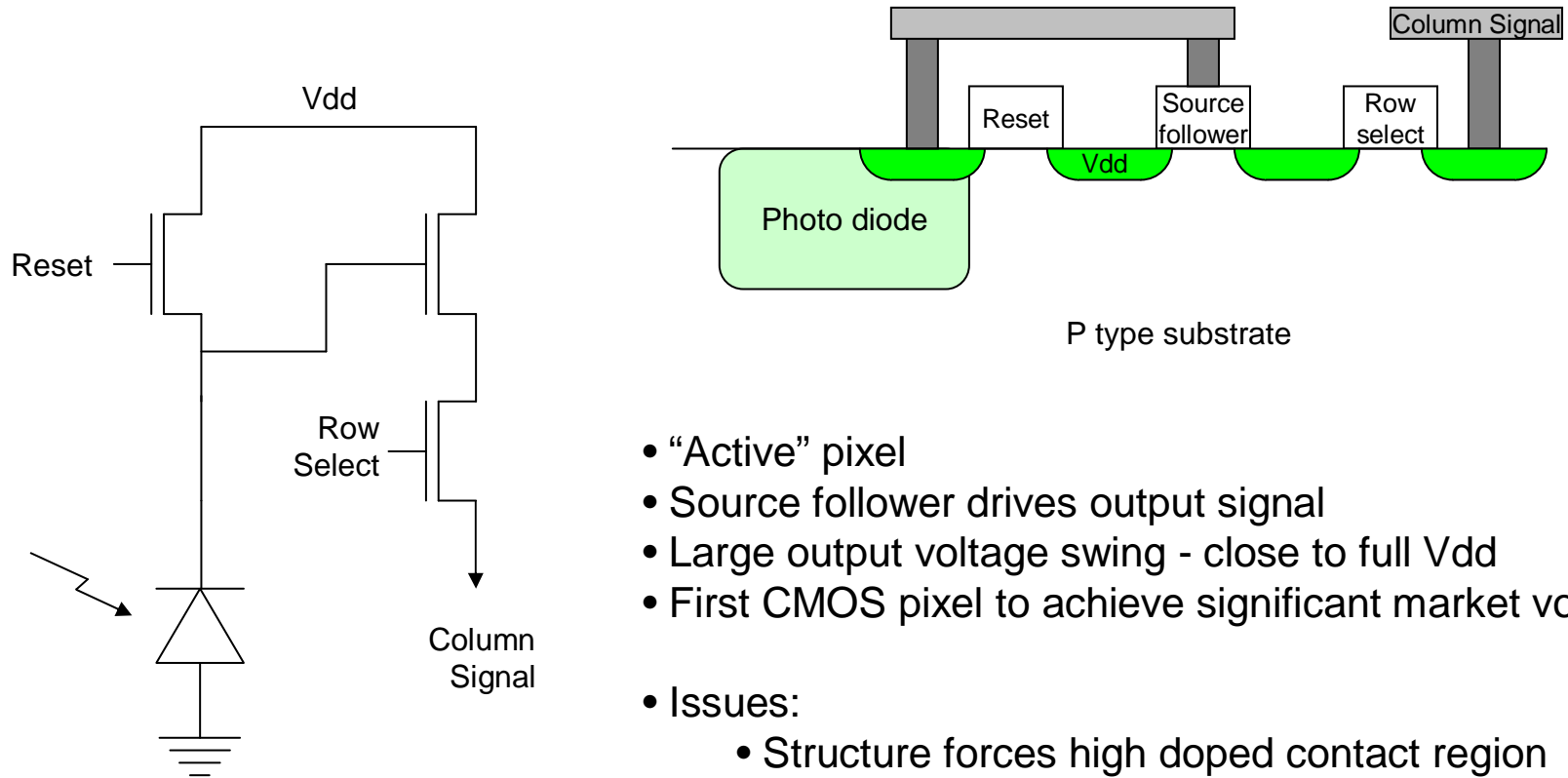
- CMOS Imagers hit mainstream late 1990's
- First CMOS imagers were at very low end of performance scale
 - Toys
 - Cell phone
- CMOS Imager pixel advances targeted on performance

Passive Pixel



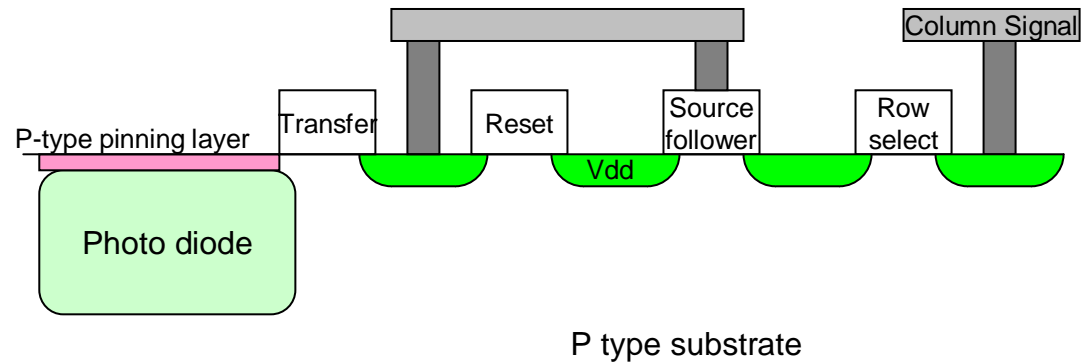
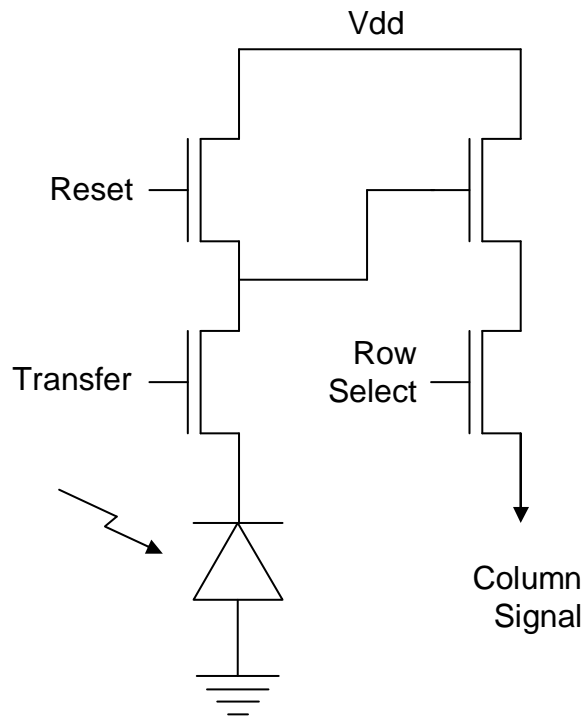
- 1 transistor per pixel
- Very poor output voltage swing
 - Capacitive charge sharing from diode to column line
- Very poor SNR
- Slow operation

3 Transistor Pixel



- “Active” pixel
- Source follower drives output signal
- Large output voltage swing - close to full Vdd
- First CMOS pixel to achieve significant market volumes
- Issues:
 - Structure forces high doped contact region
 - Diode must come to the surface
 - Dark current
 - Reset noise

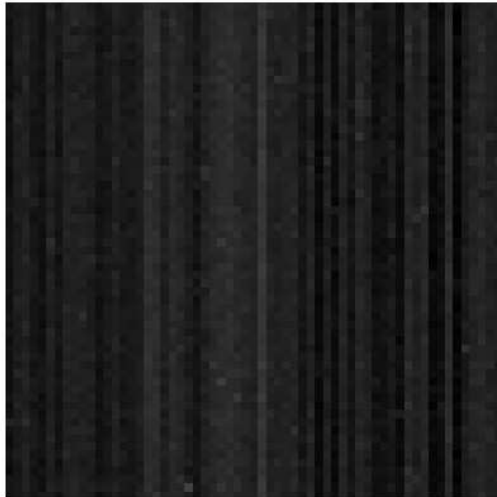
4 Transistor Pixel



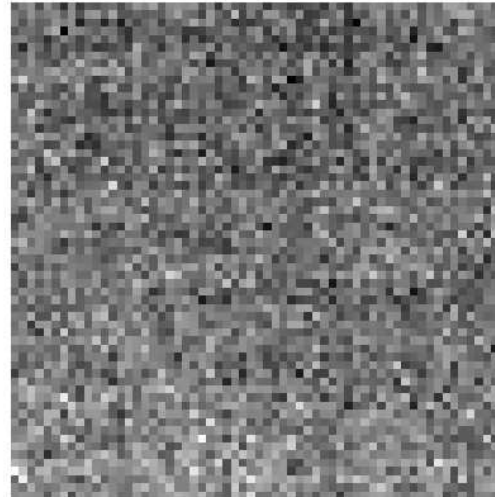
- Photo diode can be isolated from surfaces, low doped
 - Low dark current
 - Fully depleted reset
- Transfer gate allows true correlated double sampling
 - Greatly reduces reset noise and fixed pattern noise
- Draw back:
 - Voltage swing $\sim \frac{1}{2}$ of Vdd

Reset Noise and Fixed Pattern Noise

With correlated
double sample



With out correlated
double sample



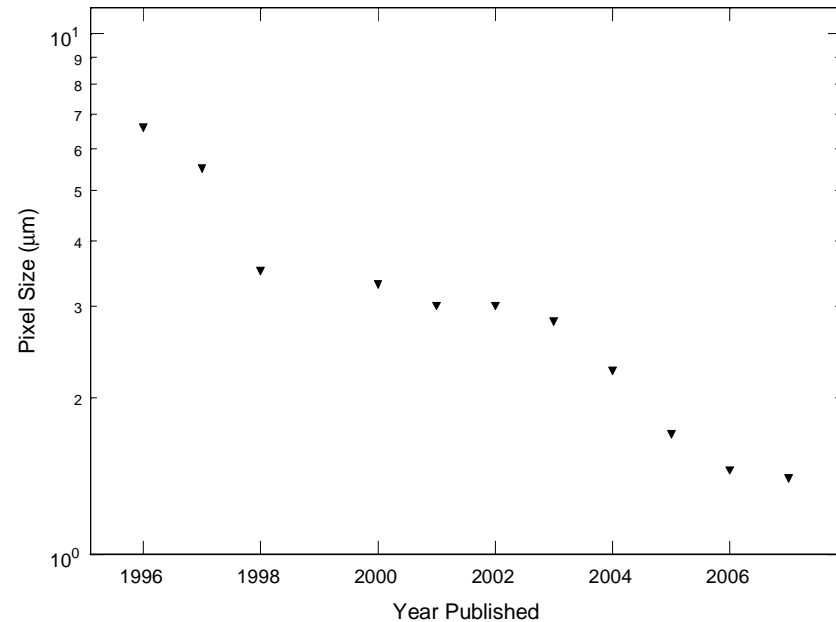
Ref: A. El Gamal, H. S. Philip Wong, ISSCC 1999 Tutorial

CMOS Imager Technology

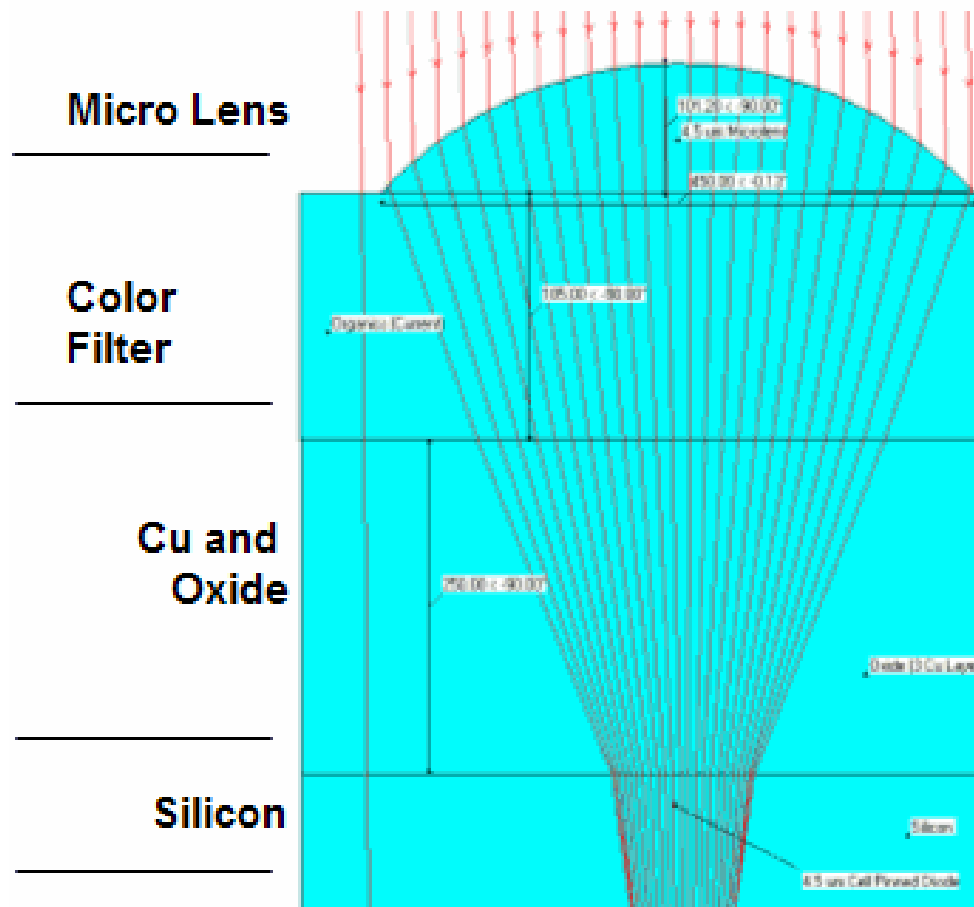
- In recent years CMOS imagers with 4T pixels and a low leakage low noise technology have yielded excellent quality images.
- High end DSLR now often using CMOS imagers

New challenge: Shrinking Pixel

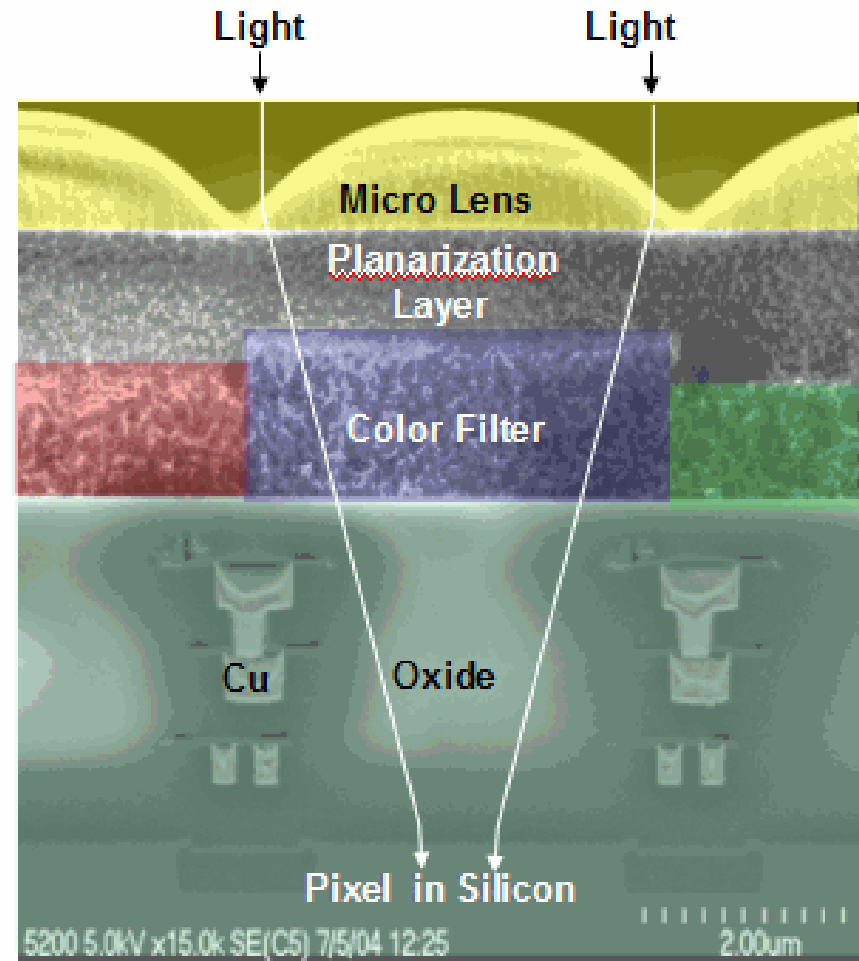
- Economics
- High pixel count without large lenses
- Form factor
 - Thin cell phones
 - Small “pocket” cameras
- Issues:
 - Light responsivity
 - Fill factor: much of the pixel not the photo diode
 - Typical small pixel fill factor <50%
 - Small light aperture
 - Reduced quantum efficiency
 - Reduced angle response
 - S/N
 - Resolution of lenses
- Strategy:
 - Focus available light on photo diode
 - Maximize portion of pixel which is sensitive to light
 - Less transistors per pixel
 - 4 → 3 → 2.5 → 1.75 → 1.5



The Micro-Lens Focuses Oncoming Light into the Pixel

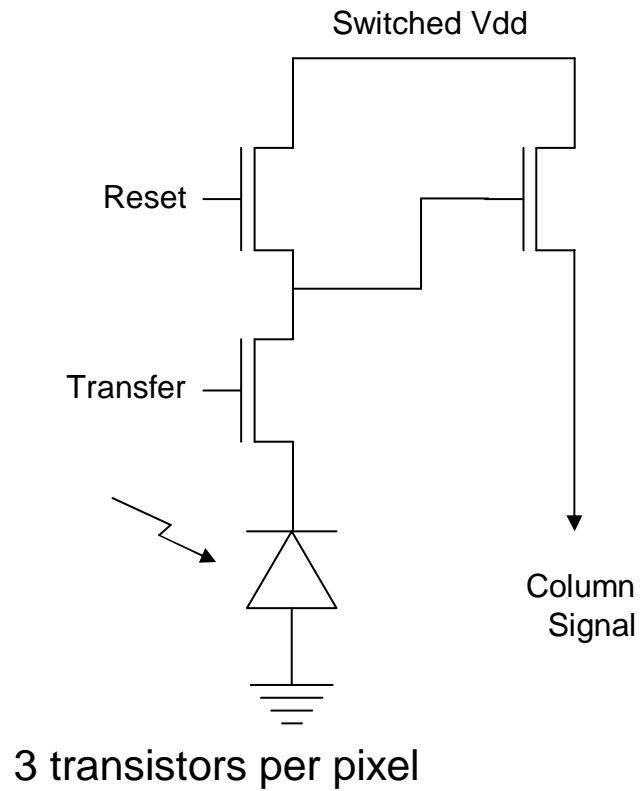


Light Ray Trace Model

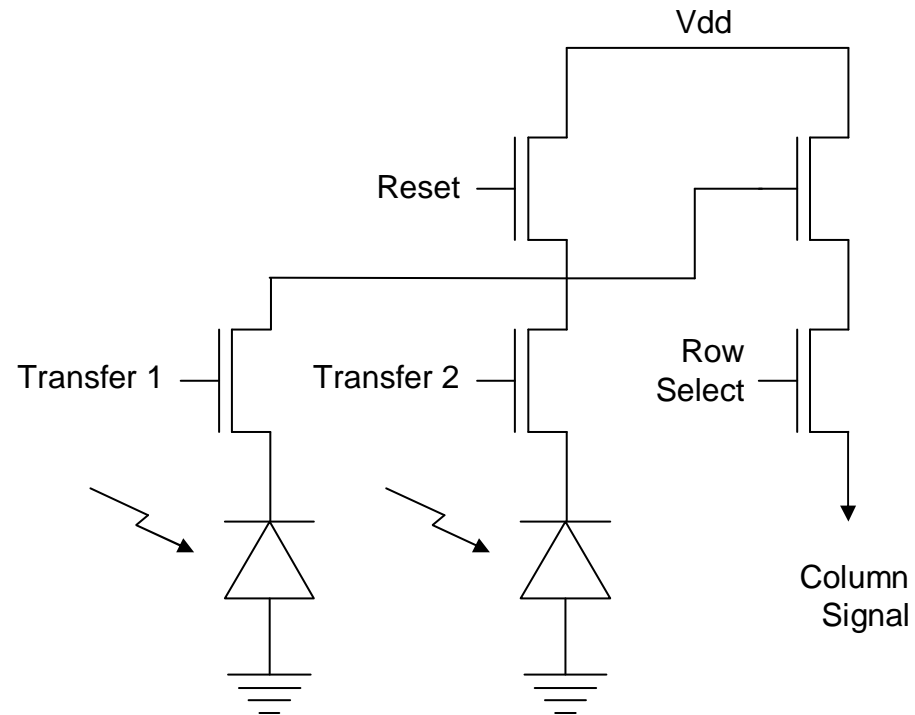


Colorized SEM Cross Section

Switched Vdd Pixel

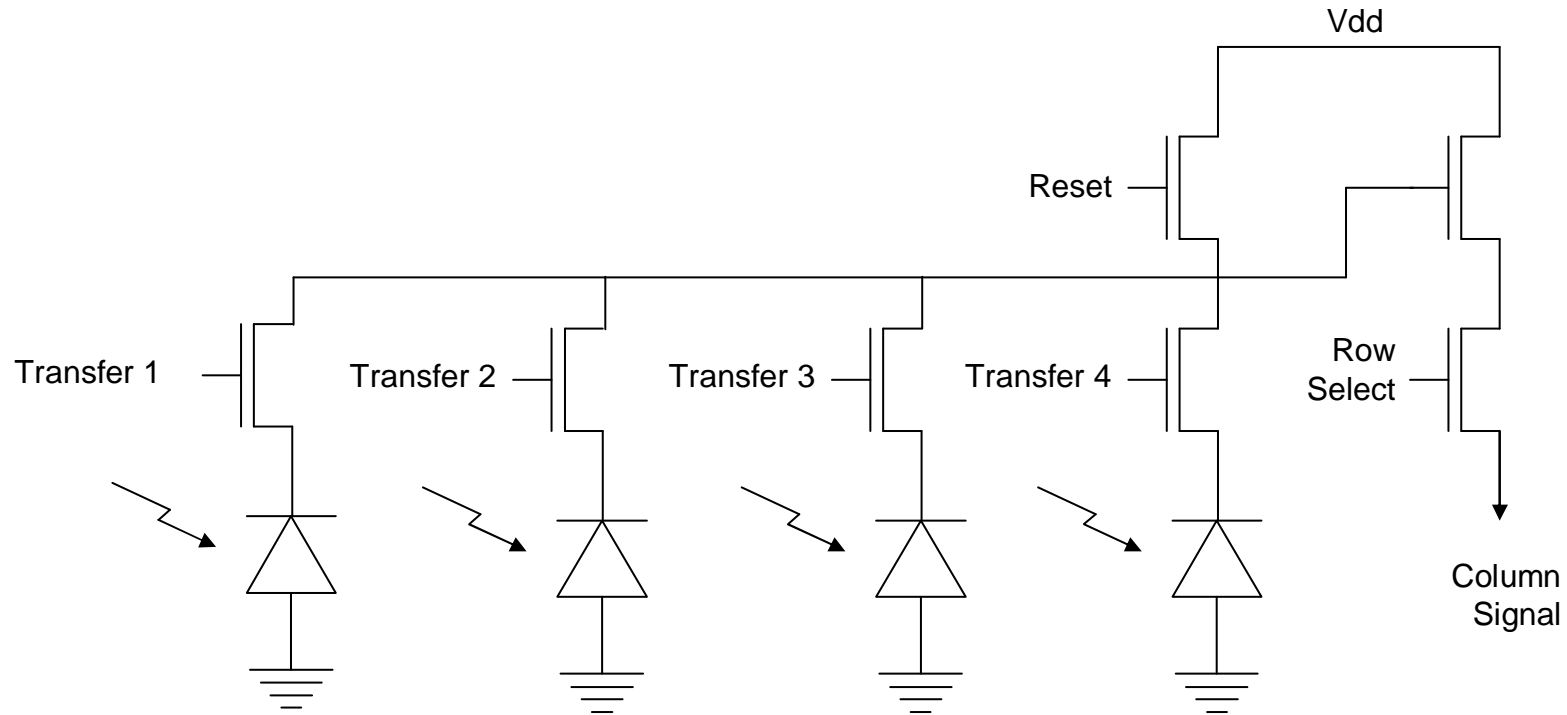


2 Shared Pixel



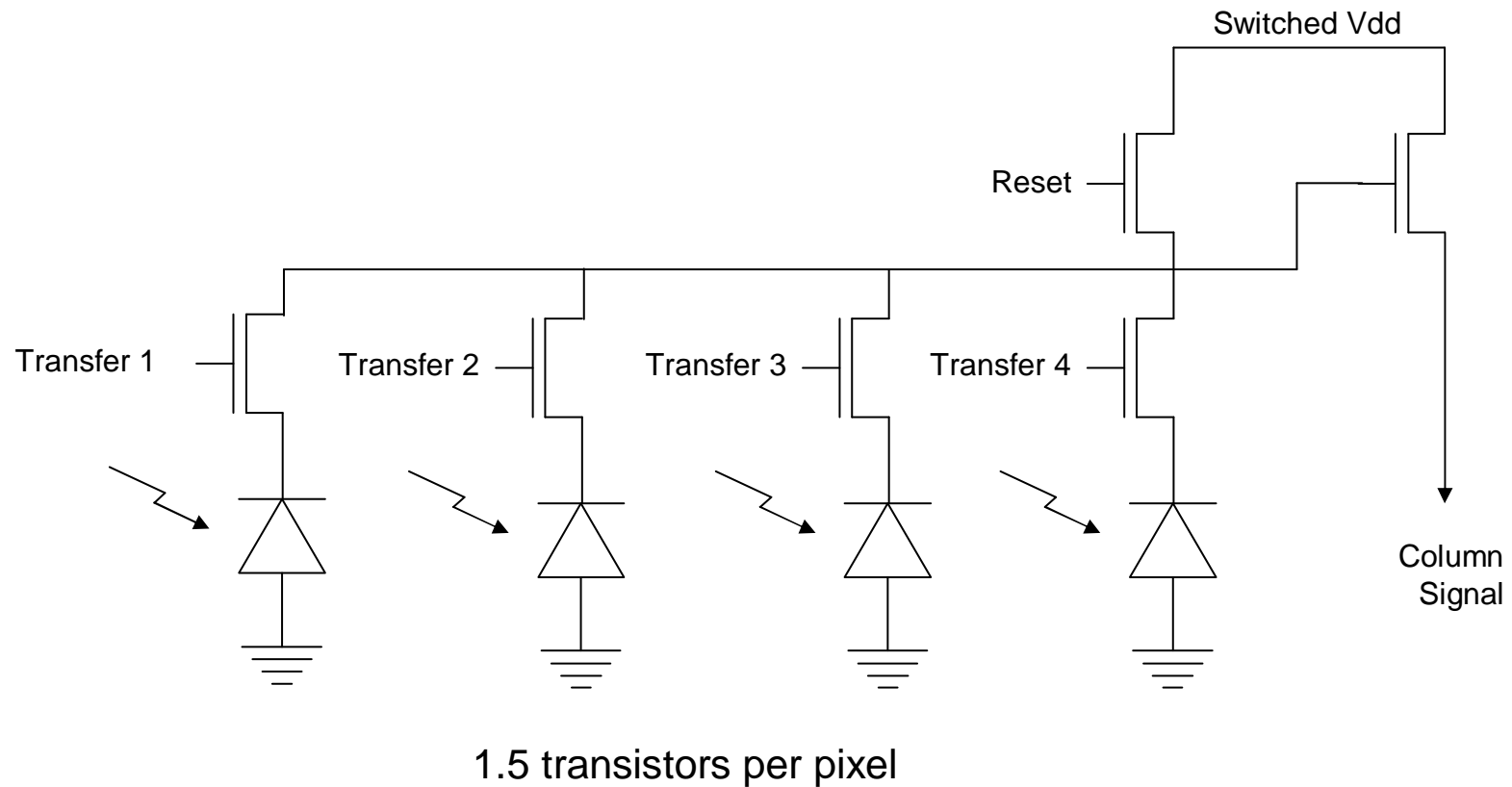
2.5 transistors per pixel

4 Shared Pixel

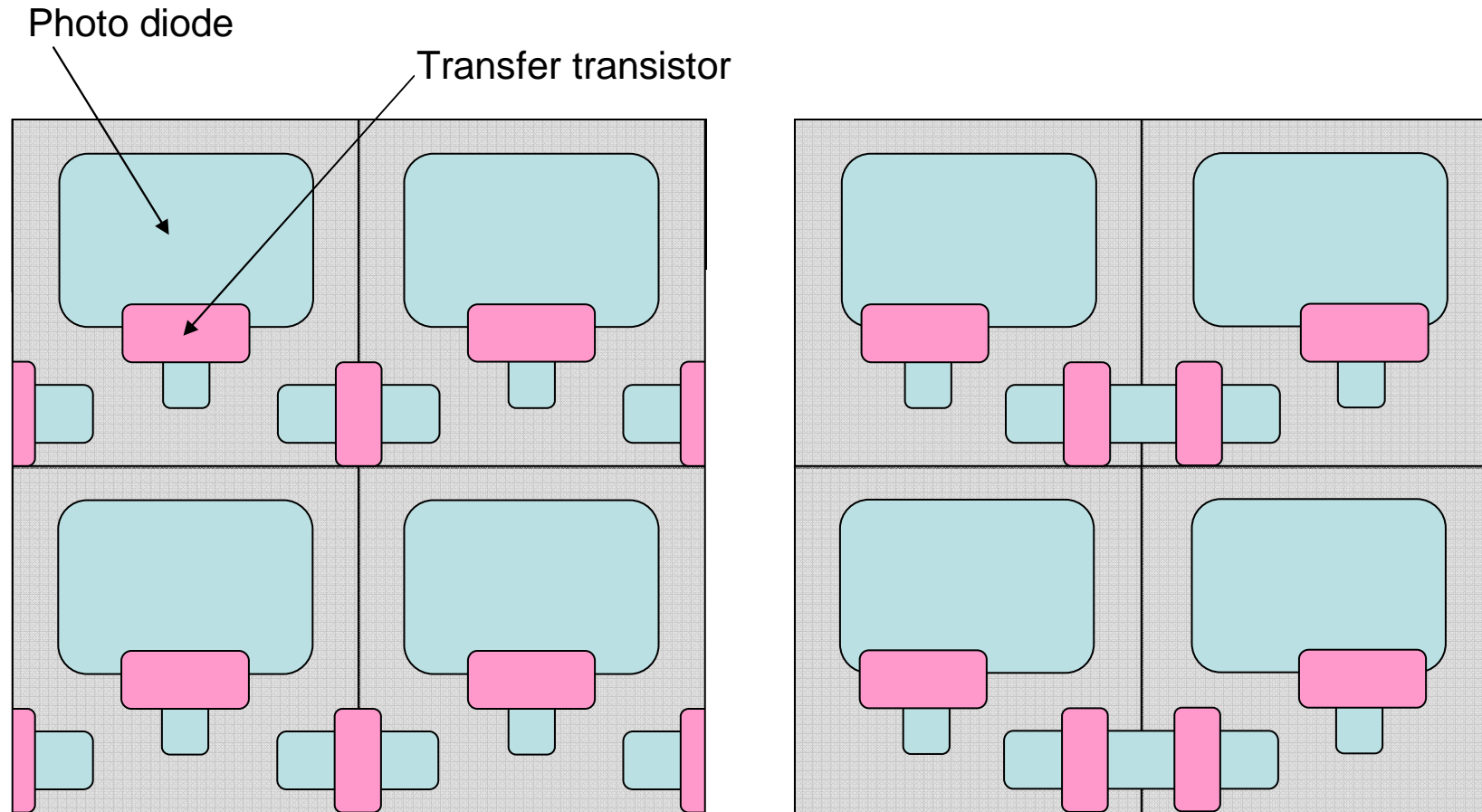


1.75 transistors per pixel

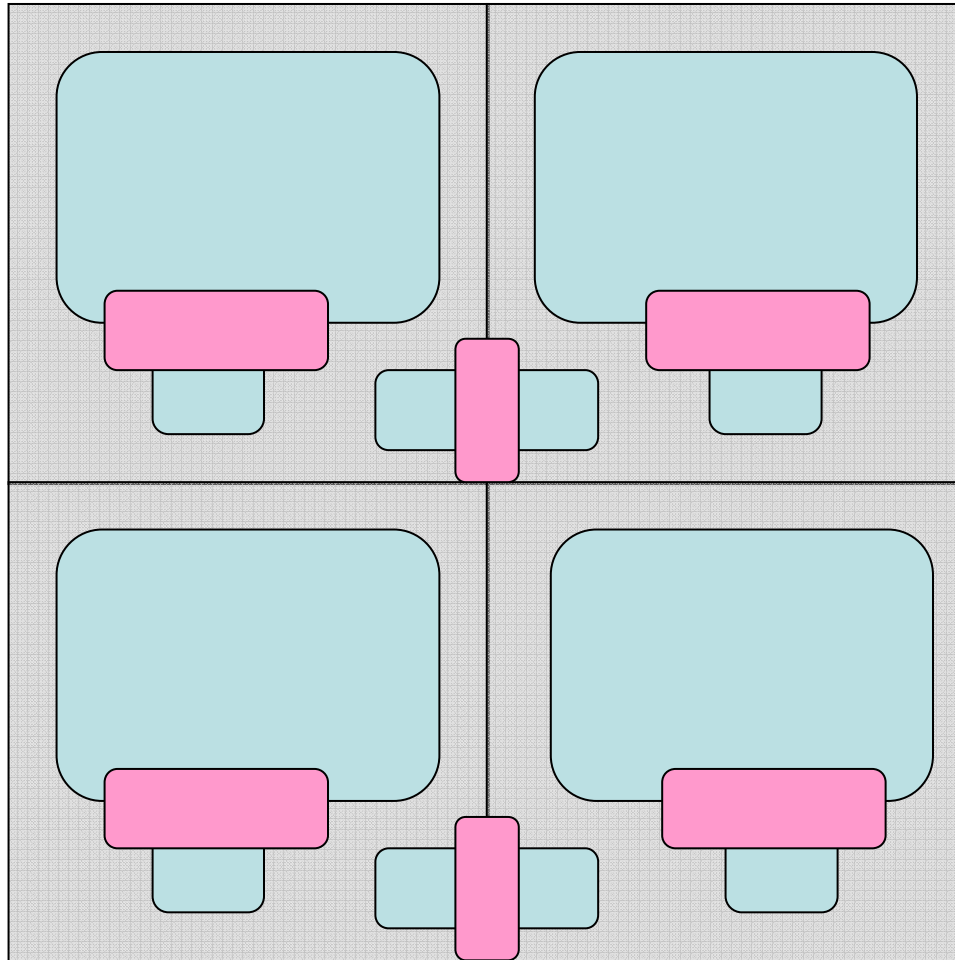
4 Shared Switched Rail



Typical Layouts – 2 transistors per pixel

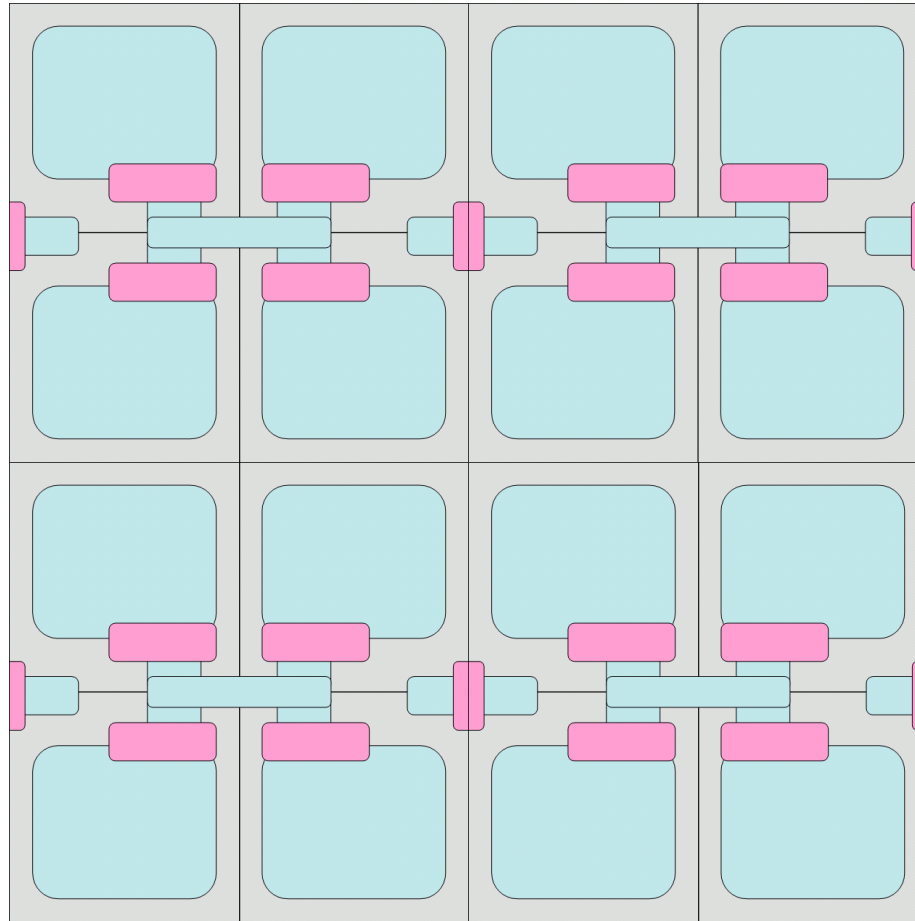


Typical Layout – 1.5 transistors per pixel



Does not buy much
In fill factor over 2
transistor per pixel
layout

Non-Periodic Photo Diode Layout – 1.5 transistors per pixel

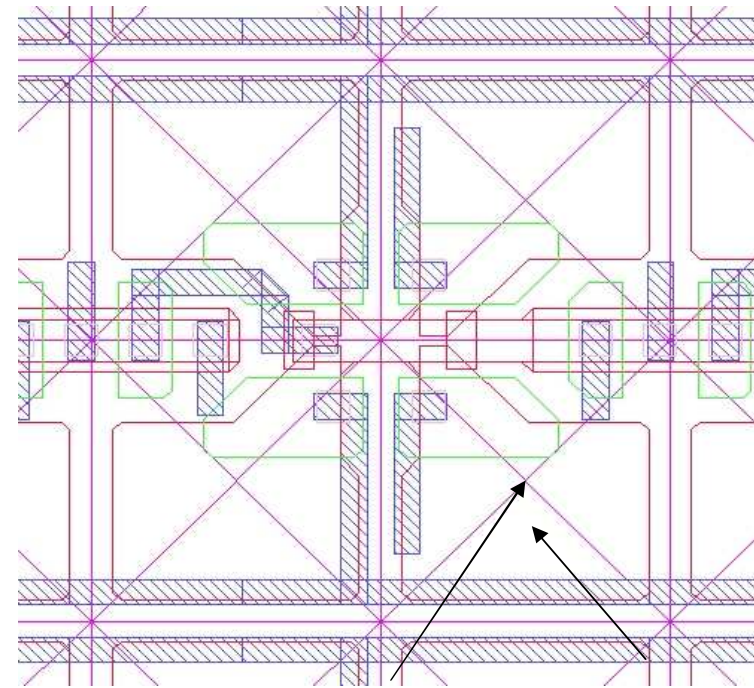
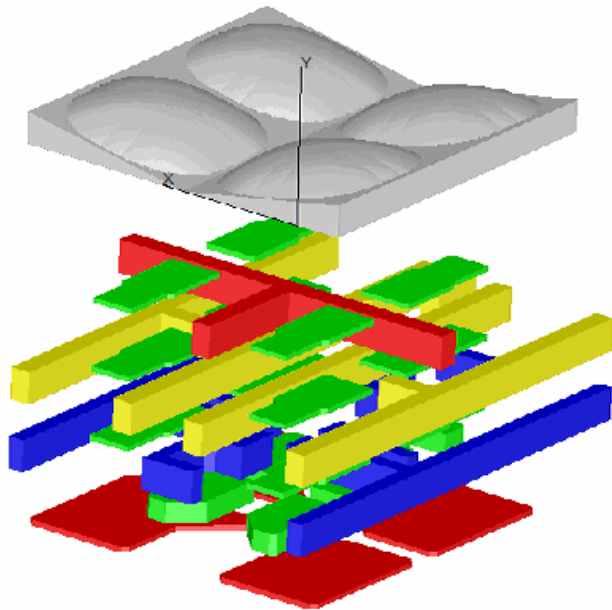


Symmetry drives
larger fill factor

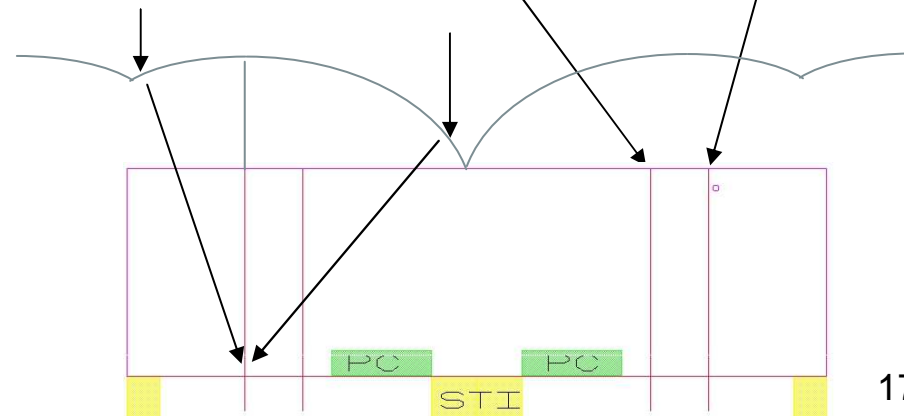
Non-Periodic Photo Diode Layout

Micro Lens Needs

- Non-traditional lens
 - Geometric center of pixel is not at the geometrical center of micro lens
 - Requires “tilt” of lens

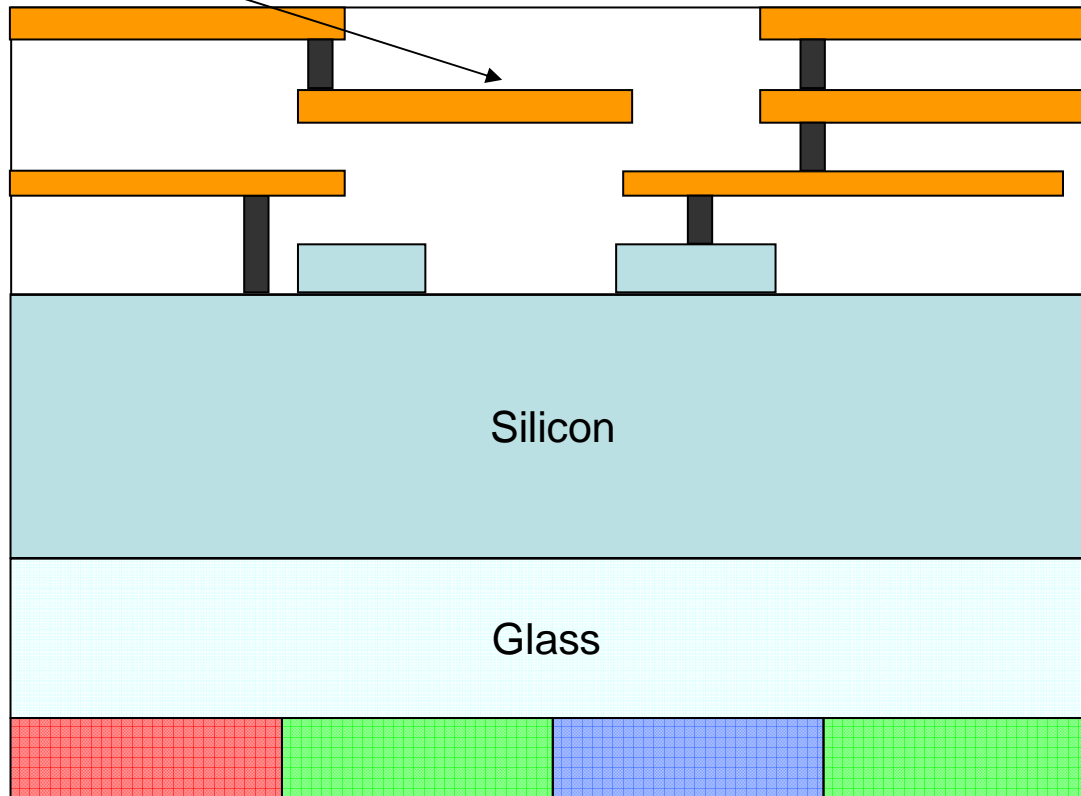


Center of pixel Center of photo diode



Back Side Imaging

Transistors and wiring



Substrate thinned.
Glass layer and color filters below.

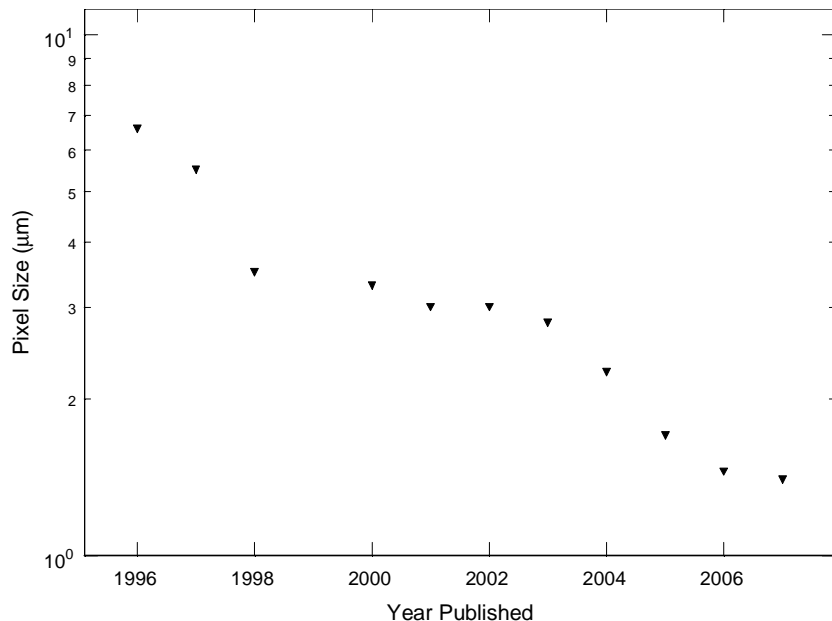
Light comes from the bottom.

Transistors and wiring
Do not block light from Silicon.

More expensive to build.

Illumination from the bottom

Pixel Size Limitations



- Semiconductor process lithography will take us a long way
 - 0.13 µm lithography making 1.75 µm pixels
 - Many litho generations to come:
 - 0.09 µm, 0.65 µm, 0.45µm, ...
- Semiconductor devices limitations
 - Devices and junctions typically get leakier as size shrinks
 - A challenge to overcome
- Color cross talk more challenging in smaller pixels
 - Ensuring that the red photons create signal in the red photo diode gets harder as geometries shrink
 - One component of noise that has to be managed
- Light responsivity
 - Smaller pixels means less photons per pixel per unit time
 - Either live with less signal or longer shutter times
 - Fundamental hit to signal to noise
- Optical diffraction limit
 - f/# 2.8 lens 550 nm light -> 3.7 µm
 - Color imagers may be able to cleanly image with 2X smaller pixels since color planes are sampled at 2X the pixel pitch
 - Not a hard limit: below that image blurring increased, sampling artifacts possible

Ultimate Pixel Sizes

- Pixel Shrinks are still possible
 - More noise
 - Images that are not as sharp
 - Less information per pixel
- Two limits:
 - Scientific
 - When do you stop gaining information content
 - Marketing
 - Can you get a higher pixel count and a “pleasing” image

Conclusion

- CMOS imager performance has significantly improved and is now close to CCD quality
- Pixel sizes have shrunk from very large to <2.0 μm
- The circuit tricks used to shrink are close to used up:
 - 1.5 transistors per pixel is probably close to the limit
 - Layout symmetry has already been used
 - Further pixel shrinks are pure lithography & process
- Limits to ultimate pixel size
 - Light diffraction
 - Light responsivity
 - Pixel cross talk
 - Signal to noise ratio