

CMOS Emerging Technology Workshop
2007

Ballistic Transistor Technology – Next Paradigm in IC Design

Martin Margala¹, and Quentin Diduck²

¹ University of Massachusetts Lowell

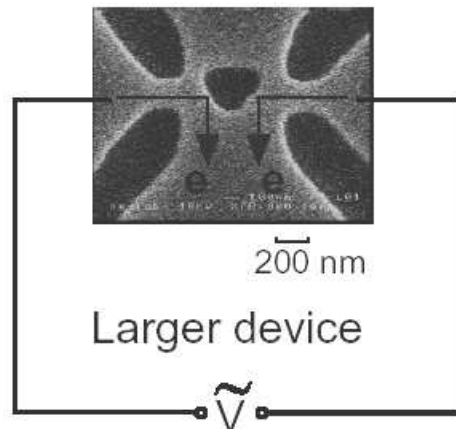
² Cornell University

Outline

- Review of Non-linear Ballistic Devices
 - Ballistic Rectifier
- Research Approach
- The Ballistic Deflection Transistor Concept (BDT)
 - Simulation Results
- HEMT versus BDT
- Properties of the BDT
- Experiments
- Analog and Digital Circuit Theory
- Summary

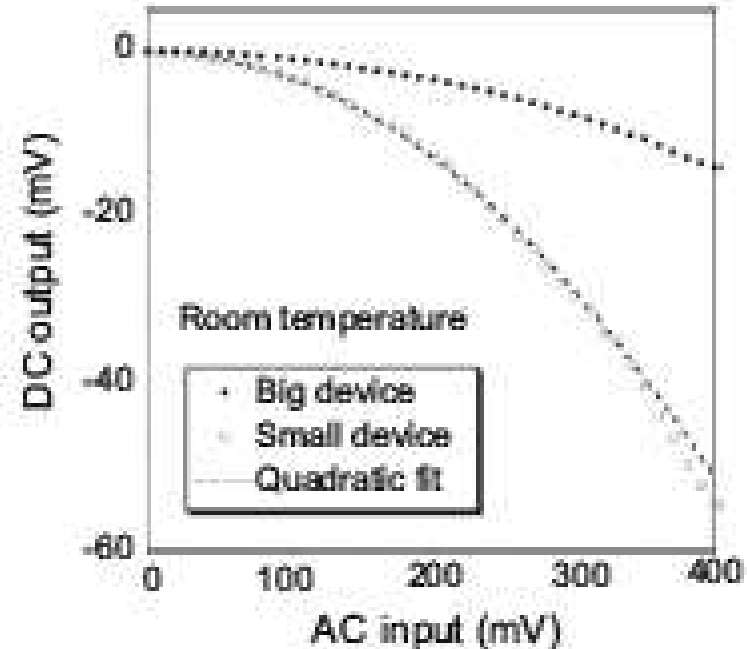
Ballistic Rectifiers

- Ballistic rectifier by Song et al. [Song et al., Jpn. J. Appl. Phys. 40, L909 (2001).]



SEM image of the Ballistic rectifier

- Dark regions are etched 2DEG
- Planar structure (low capacitance)
- Bridge rectifier behavior



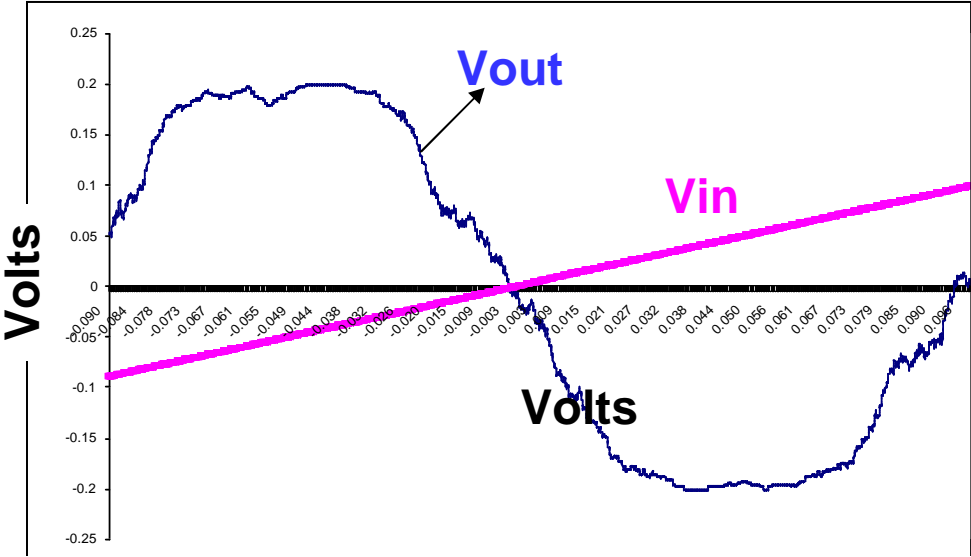
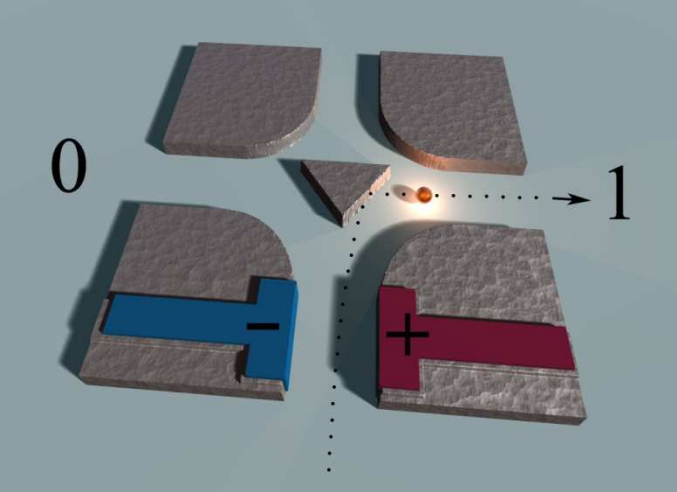
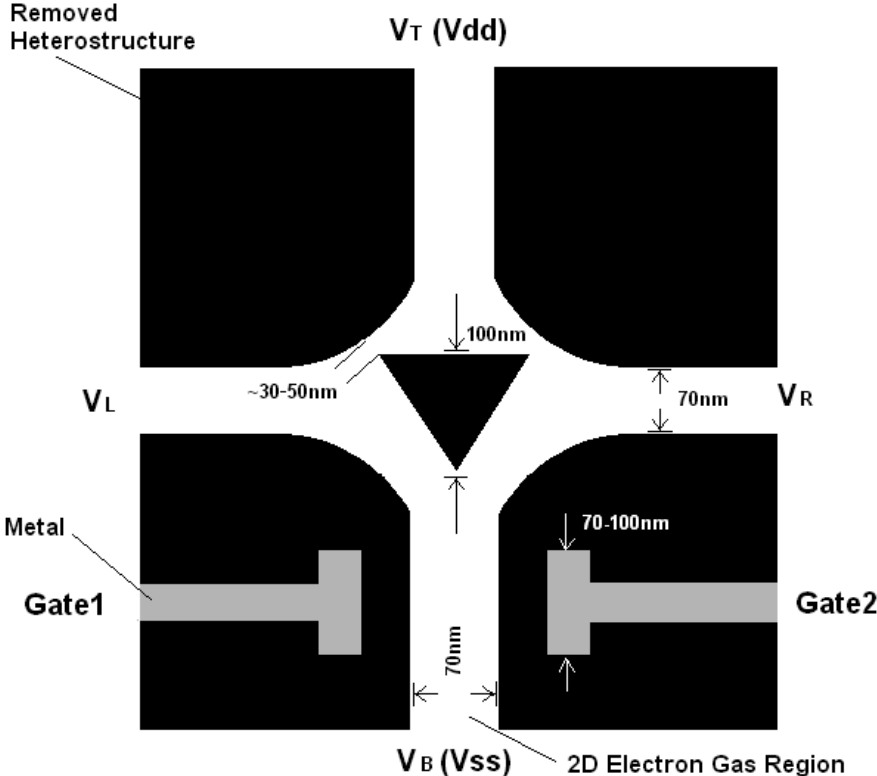
Room-temperature operation of the ballistic rectifier. The frequency of the input ac signal is 1 kHz. The dashed line represents a quadratic fit to the experimental result. The ballistic rectifier has been demonstrated only up to 50 GHz.

Our Research Approach

- The Landauer-Büttiker theory describes ballistic transport well at low temperatures (linear behavior), but fails to explain non-linear behavior at room temperature
 - **An extension to this theory is needed**
- 1. Currently performing room temperature experiments on ballistic devices:
 - Study the effect of deflection geometry (size, style),
 - Study of the depletion effects,
 - Investigating the possibility of a gate steering mechanism.
- 2. Develop a non-linear version of the Landauer-Büttiker theory and adapt it to our geometry
- 3. Develop a complete understanding of the principal mechanisms that drive room temperature terahertz conduction

Ballistic Deflection Transistor

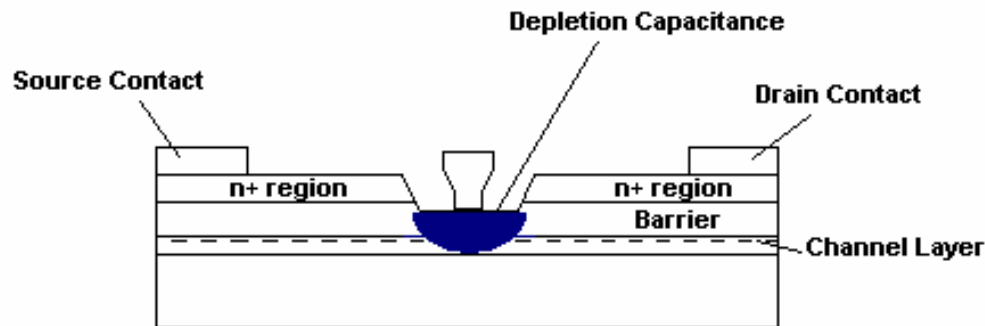
- Ballistic Deflection Transistor (BDT)



Monte Carlo -type Simulation of BDT switching at room temperature

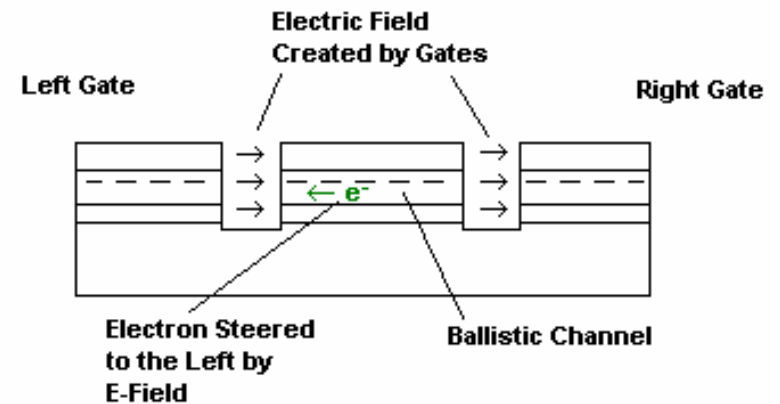
Conventional HEMT design VS Low Capacitance BDT

Cross Section of HEMT



- Large depletion layer – large capacitance
- 3-dimensional structure
- Runs very hot at high frequencies

Cross Section of BDT



- Very small capacitance (only gate to channel – no depletion)
- 2-dimensional structure, near planar geometry
- e⁻ are confined within 2-DEG
- Significantly faster than HBTs and HEMTs

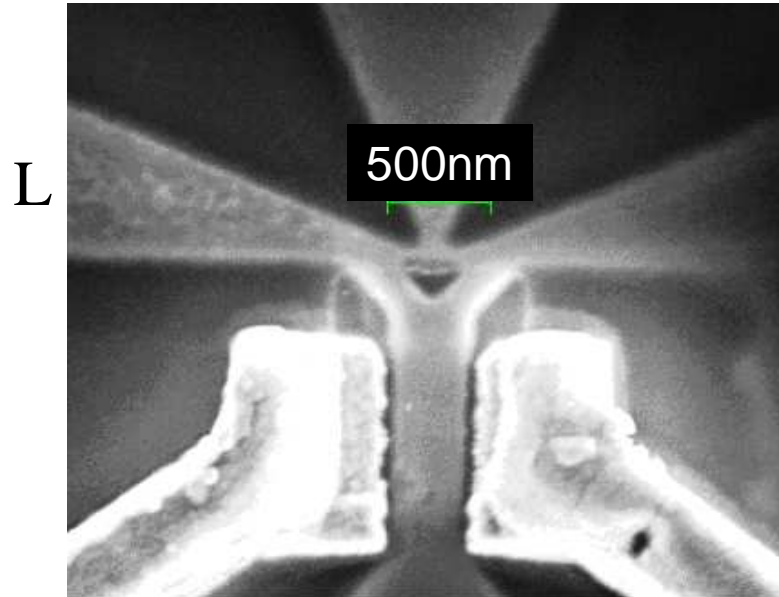
Properties of the BDT

- **Low power consumption**
 - rough calculation: $10 \mu\text{W}$, with no optimization
 - ballistic conduction not intrinsically dissipative
 - so great opportunities for low power design
- **Large nonlinearity: rectifier has $V_{\text{DC}} \approx V_{\text{pp}}/2$ at low f**
- **Unique operation principle: no junction or barrier structure**
 - mean free path $\lambda = 140 \text{ nm}$
 - simulation models indicate $> \text{THz}$ operation at room temp.
 - other models consistently agree $> \text{THz}$ operation for room temperature ballistic devices

Properties of the BDT: Noise

- **Conduction mechanisms not firmly understood**
- **No experimental data about room temperature noise**
- **Nevertheless (optimistically) extremely low noise anticipated**
 - **thermal noise minimal?**
 - ➔ **ballistic transport not coupled to the heat bath**
 - **i.e fluctuation-dissipation theorem doesn't apply**
 - ➔ **operates at V below kT/e ?**
 - **gate noise integration effect**
 - **some say, the low voltage limit is $h/e\tau$**
 - **shot noise sub-Poissonian?**
 - ➔ **according to Blanter and Büttiker, "Shot Noise in Mesoscopic Conductors," Physics Reports 336, 1-166 (2000)**

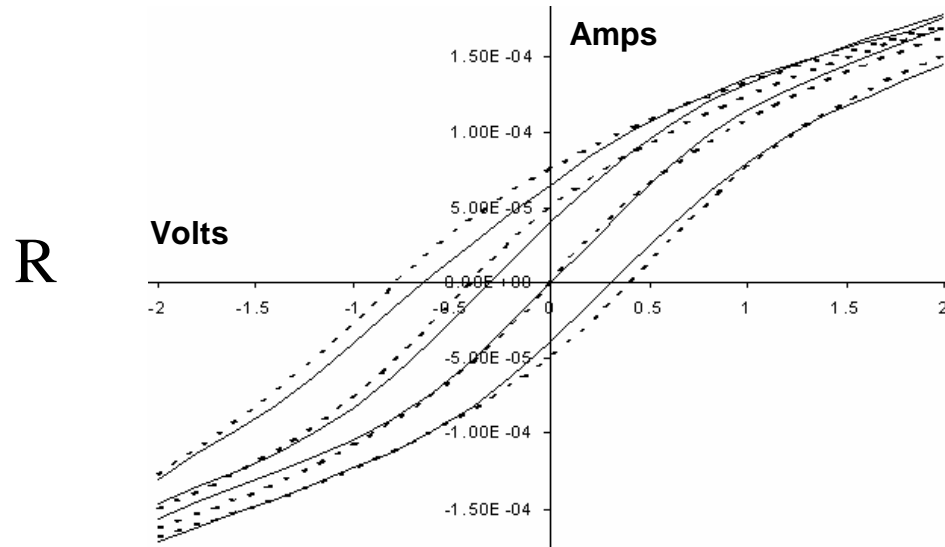
Winter 05 Experiments



B

SEM image of the measured
non-linear ballistic device.

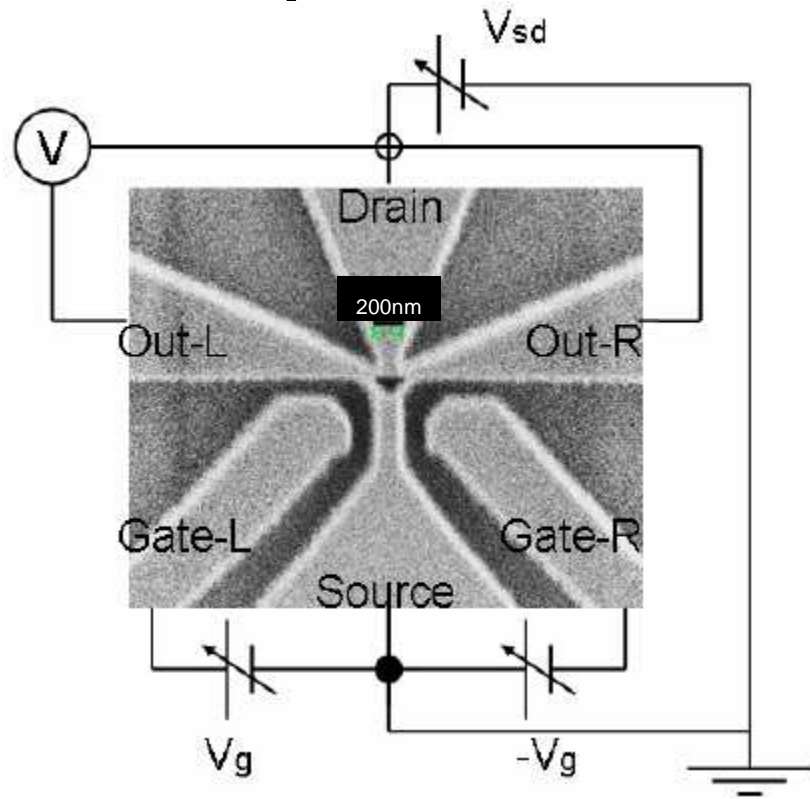
- Demonstrates Non-linear
behavior at room temperature



**Current vs. voltage, B=ground,
VL=VR, VT = -1 V, -0.5 V, 0 V, 0.5 V
from top to bottom.**

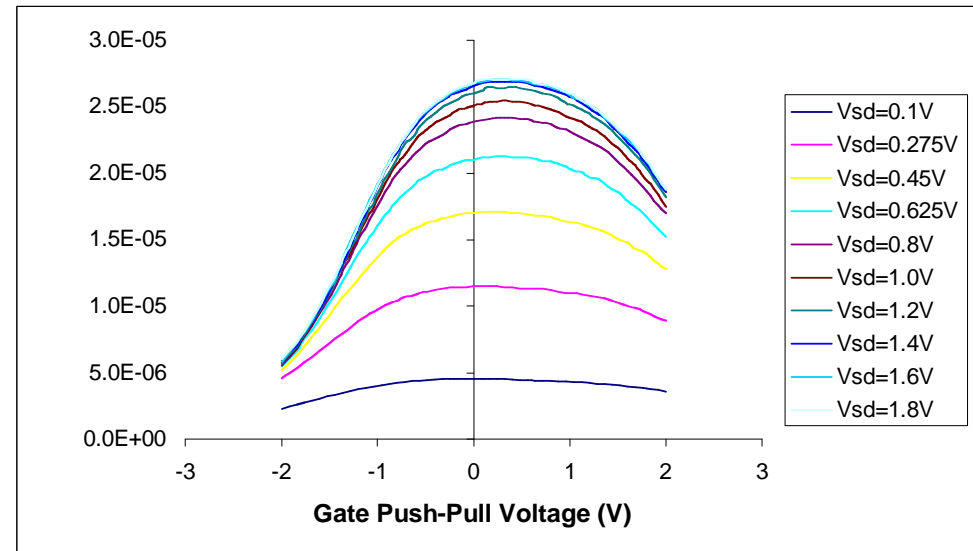
- Solid lines are experiment
- Dashed lines are calculated with only one estimated parameter.

Winter 06 Experiments



**SEM image of the measured
non-linear ballistic device.**

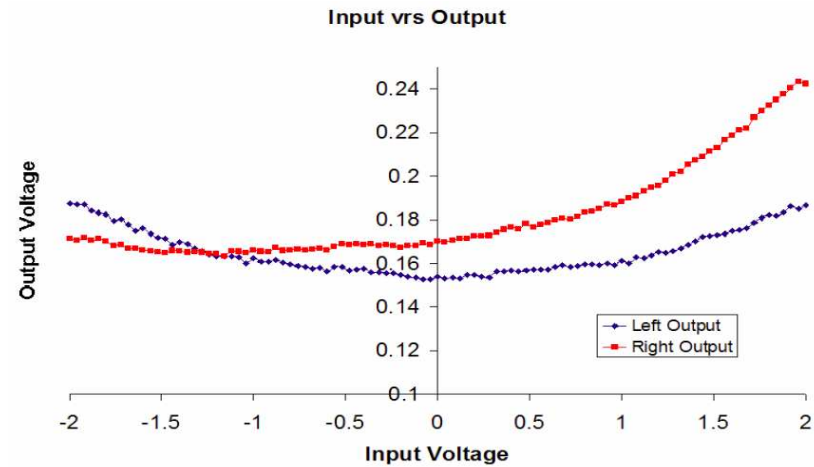
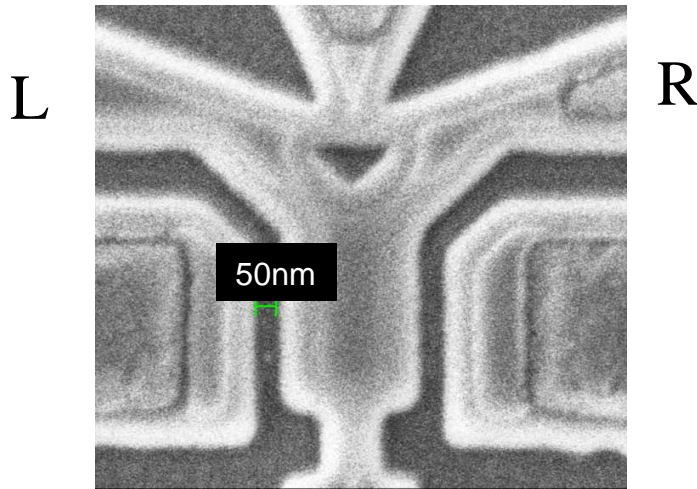
-Demonstrated Non-linear
behavior, the saturation
effect, and improved gain.



- Current increases with V_{sd} at low
 V_{sd} and saturates at $V_{sd} \sim 1V$

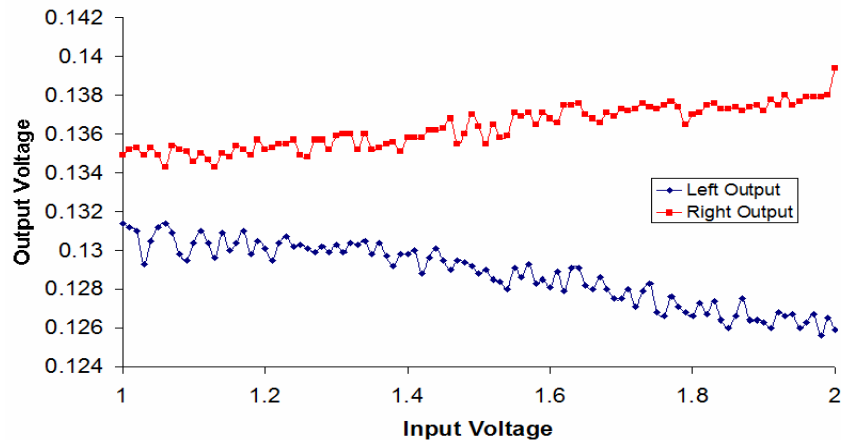
Spring 07 Experiments T

-demonstrates smallest feature
device size, improved gate
structure, and steering effect



B

Input vrs Output



Above - Field effect combined with steering effect, The left gate biased from -2 volt to 2, while the right gate is biased from 2 down to -2 simultaneously. Note that both voltages rise at the extremes due to field effect depletion.

Left – Pure Steering effect, Left gate biased from 1 volt to 2, while the right gate is biased from 2 down to 1 simultaneously.

Difference from Simulation

- Simulation results differ from experimental dramatically, why?
 - Lateral built in electric fields are created during the channel defining etch.
 - Surface states induce a greater field than the lateral gates induce, due to proximity.
 - It is expected that passivation will eliminated this effect
 - Revised simulation results with lateral potential built in fields indicate similar results

Potential Basic Circuit blocks and Simple Analog Structures.

- Basic BDT structure is expected to behave like a differential pair
- Analog circuits can be designed using an assumption that the basic building block is a differential pair.
- BDT makes a natural Comparator structure without any additional parts, but can be chained to increase speed.

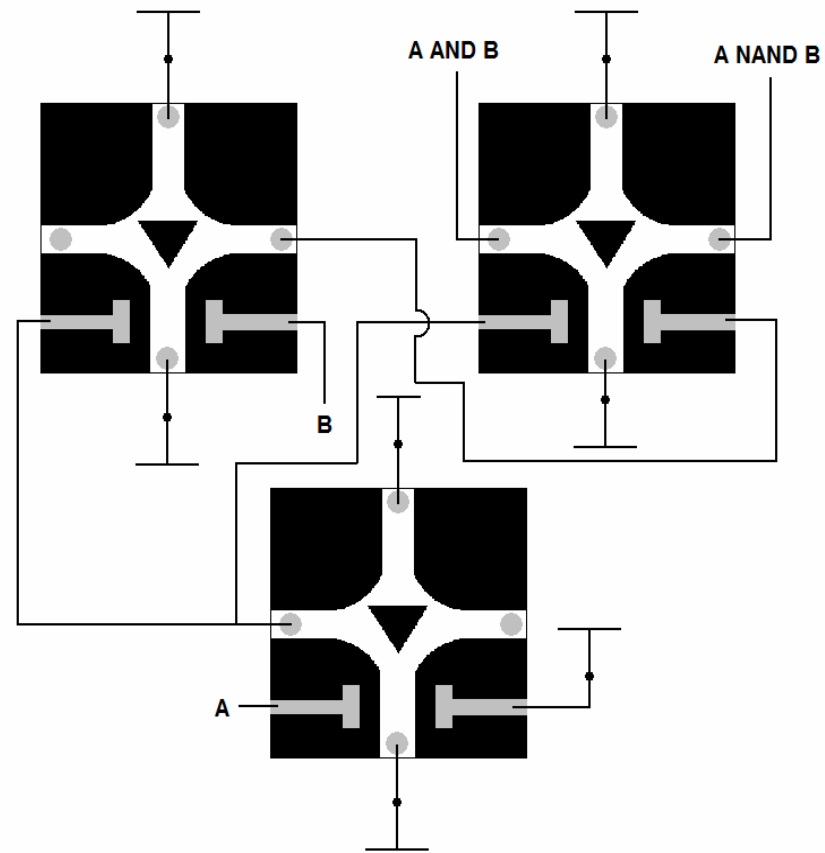
Expected Digital Behavior

- Simulation results indicate that there are 3 natural states to the BDT: High, Med, and Low.
- Gate Inputs and Expected Results
- Natural ternary logic style supported

Left Gate	Right Gate	Output-L	Output-R
Low	Low	Med	Med
Low	Med	High	Low
Low	High	High	Low
Med	Low	Low	High
Med	Med	Med	Med
Med	High	High	Low
High	Low	Low	High
High	Med	Low	High
High	High	Med	Med

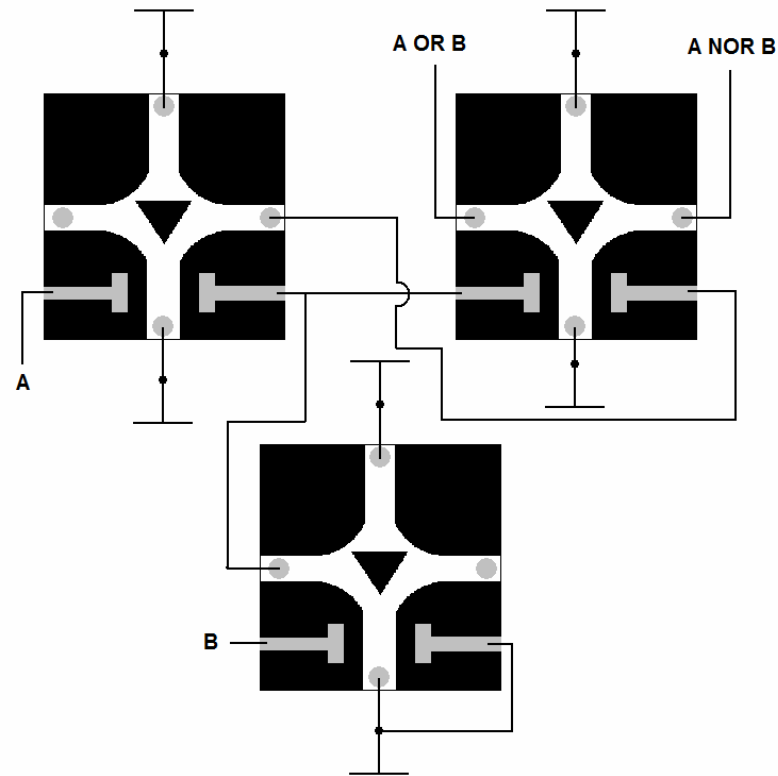
AND-NAND Circuit

- Two input AND-NAND gate can be created from 3 transistors.
- Half V_{dd} voltage states are internal to the circuit
- 3rd transistor eliminates all potential half vdd voltage states



OR-NOR Circuit

- Two input OR-NOR circuit is created from 3 Transistors
- Same internal half vdd voltages exist in this circuit
- No known way to eliminate the internal half vdd voltage states



Summary

- Reviewed non-linear ballistic transport using the ballistic rectifier as a device example
- Presented Simulation Results of the BDT
- Demonstrated non-linear behavior of BDT device at room temperature
- Demonstrated a gate steering effect at room temperature
- Discussed Analog and Digital circuit potential
- Presented basic digital logic circuits

Future Plans for BDT Project

- In near term:
 - conclude the investigation of process effects on device formation and gain,
 - identify the techniques for built-in potential reduction in the channel,
 - fully characterize the BDT
- In long term:
 - Investigate four different hypotheses that we developed to explain the non-linear ballistic conduction at room temperature,
 - Investigate two parallel tracks of BDT design: (a) ultra low-power and (b) terahertz operation,
 - Investigate the noise sources in BDTs and their effect on BDT operation;