

# **Data Converters, Navigating The Sub-Micron CMOS Landscape, or, When Will The Fun Ever Stop!**

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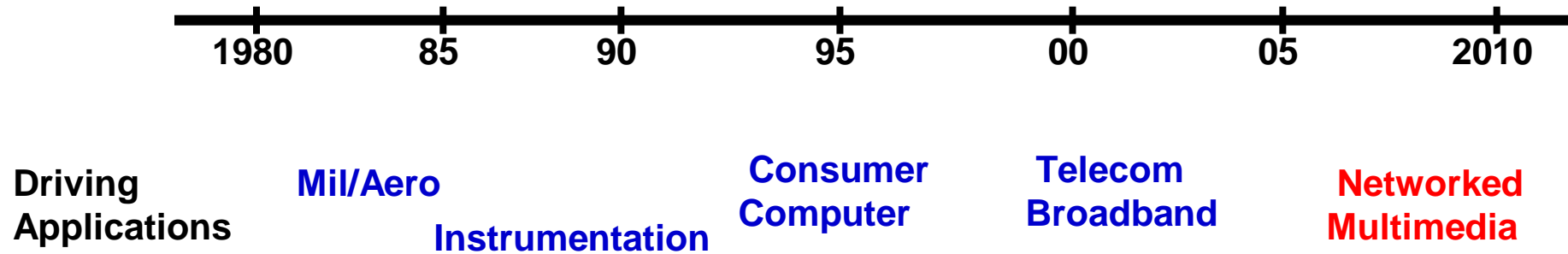
# Today's Topic

- ❑ **“The world is going digital”**
- ❑ **But the real world is analog!**
- ❑ **Data Converters bridge the two worlds**
- ❑ **Where will this “bridge” reside?**
- ❑ **Digits in Deep Submicron - - - -**
  - ❑ **But does it make sense for the Volts and Amps of analog signals?**  
( 0 dBm = 0.633 Vpp in 50 ohms  
25 mA to drive double terminated line )

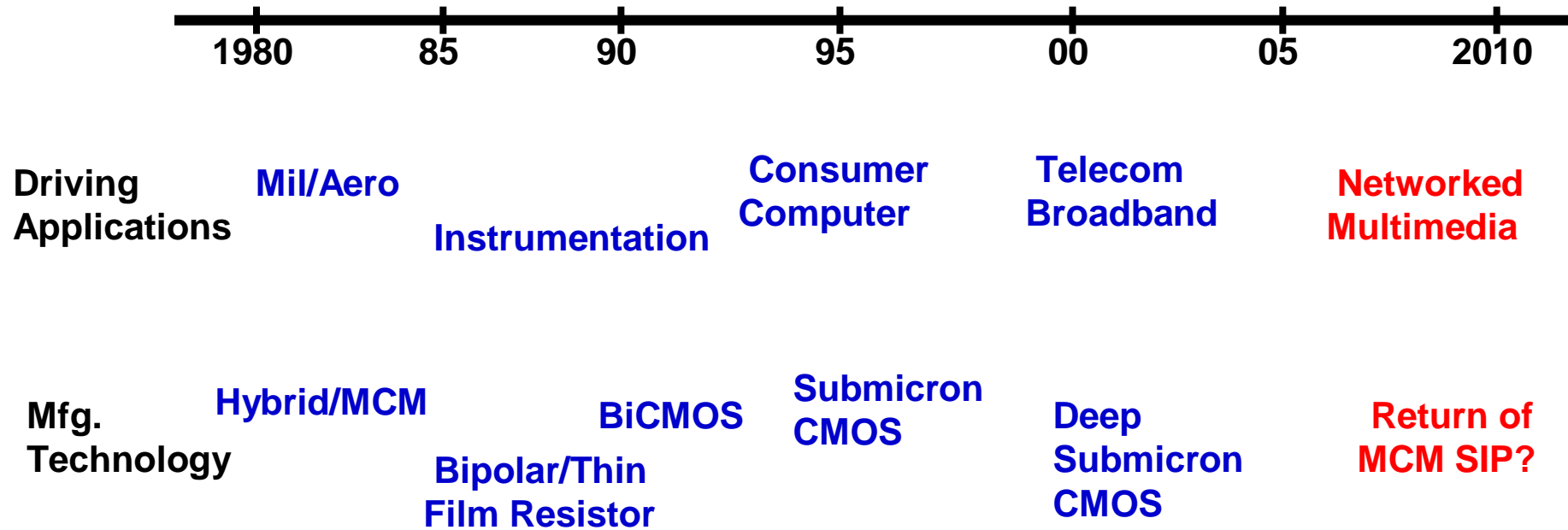
# Outline

- I. **Historical Perspective– Converters and Mixed Signal Over the Past 30 Years**
  
- II. Data Converter Trends for the Next 5-10 Years
  - Application
  - Implementation

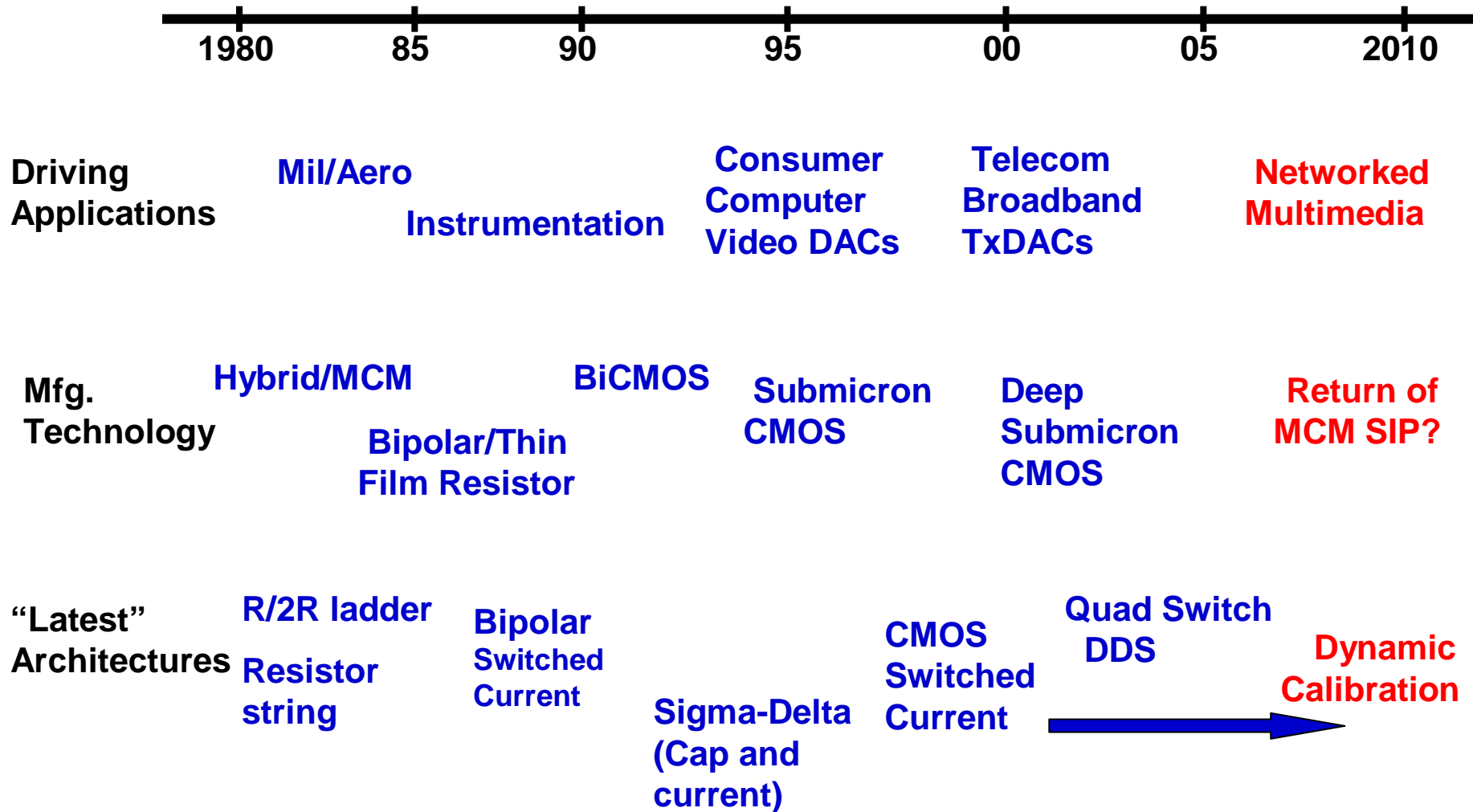
# Data Converter Timeline



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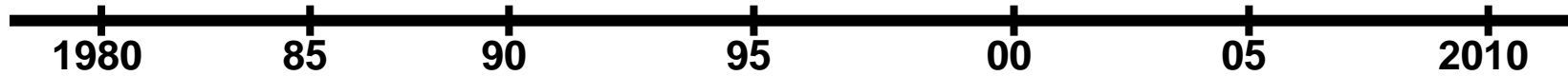
# DAC Timeline



# Data Converter Timeline

The “Bronze Age” of Integration

The “Tarnished Age” of SOC



The “Golden Age” of CMOS

Driving Applications

Mil/Aero Instrumentation

Consumer Computer Video

Telecom Broadband

Networked Multimedia

Mfg. Technology

Hybrid/MCM Bipolar/Thin Film Resistor

BiCMOS Submicron CMOS

Deep Submicron CMOS

Return of MCM SIP?

“Latest” Architectures

SAR/Flash Voltage mode R/2R Folding Sigma-Delta (S.C.)

Pipeline Switched Cap

Current mode Sigma-Delta (C.T.)

Digitally compensated analog?

# The Challenges of Scale – SOC for Everything?

Integration (power reduction, process/supply migration) continues to drive 70% of conference paper submissions, BUT:

How many applications can support a \$50 to \$100M development cost?

What are the alternatives?

- is there an analog / mixed signal FPGA?
- will the next wave of innovation be about “breaking the tyranny of scale”
- partitioning and packaging

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“the Golden Age of CMOS” with interchangeable processes and accessible foundries was as much a phenomenon of economic scale as it was technology

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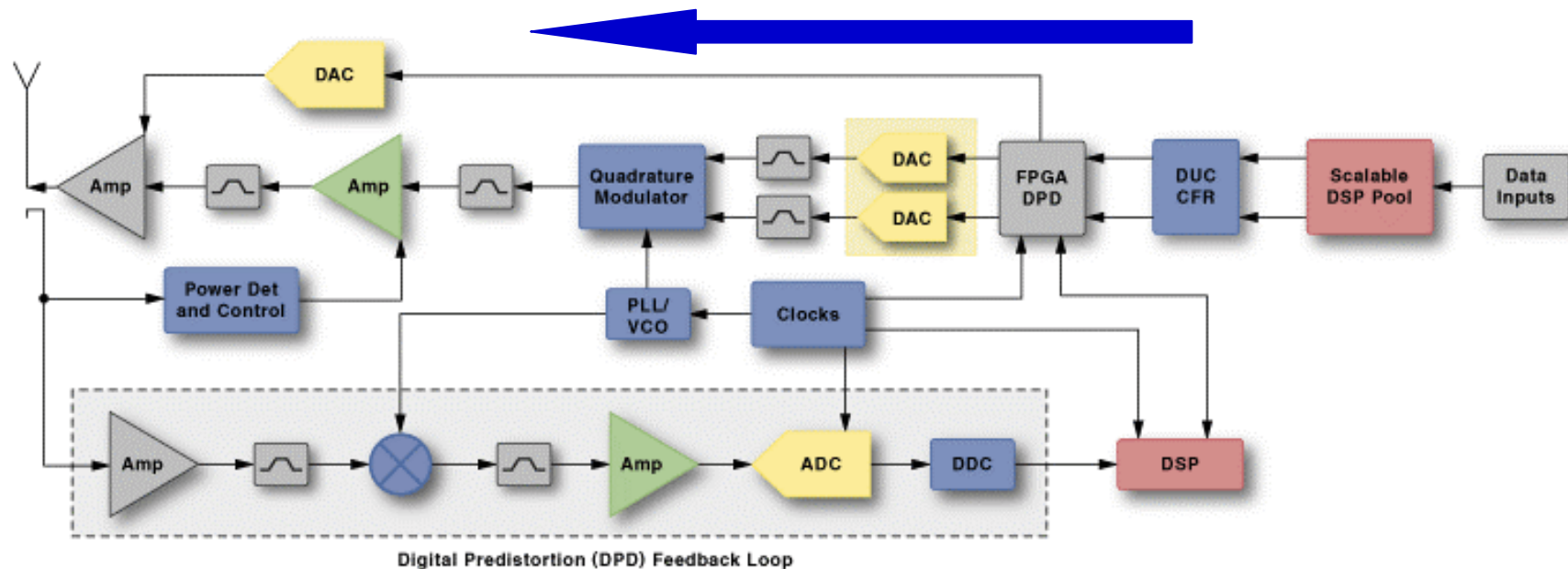
# **New Applications: Si “Boldly Going” Where Si Has Not Gone Before**

- ❑ **Communications: Voice→ Data→ Multimedia**
- ❑ **Ubiquity: portability, mobility**
- ❑ **Power aware “Green” products**
- ❑ **New Sensor Technologies: detecting the previously undetected**
  - **Accelerometers, Gyroscopes**
  - **Chemical and Gas Sensors**
  - **Biology Health Applications**

**Enablers: lower cost, smaller size, lower power, new capabilities**

# Application Trend: Move Converter Closer to “the Load”

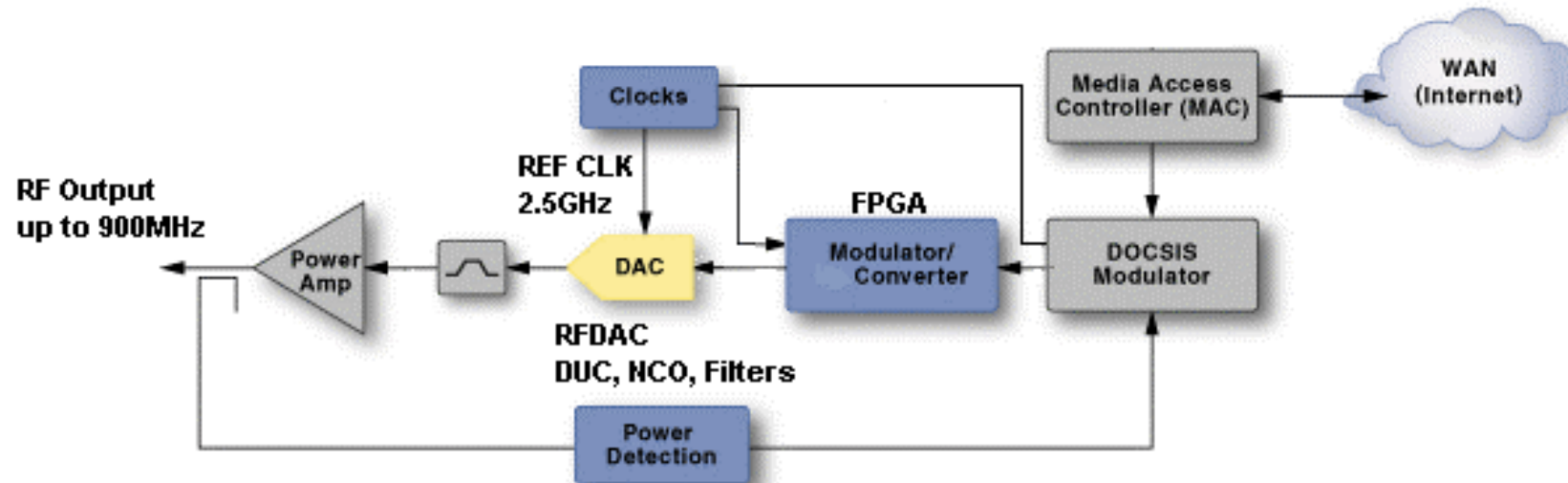
*As the DAC moves towards the antenna, eliminating up conversion stages, analog signal processing is replaced by digital . . .*



## Conventional Direct Conversion Transmitter Chain

Pre-distortion requirements increase both Converter dynamic range and bandwidth.

# RFDAC Architecture (Utopia DAC) Concept 2 - 3 years out



- DAC is running at >2GSPS output sample rate
- DAC includes NCOs, Filters, Digital Mixer ( DUC )
- RF output covers all the spectrum up to 900MHz
- The goal of this concept is to:
  - reduce power consumption further
  - Have a fully flexible RF output system
  - Get away from high speed links between FPGA and DAC

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# Data Converter & Mixed Signal Trends: Greater Use of Parallelism

**“Sure, the devices are crummy– less gain, and leaky– but you get a lot of them . . . “**

- ❑ **Traditional analog circuits may not scale as aggressively as digital– seek to take approaches that can take advantage of the technology scaling**

## **Examples:**

- ❑ **K. Poulton, et. al.; “A 20GS/s 8b ADC with a 1MB Memory in 0.18u CMOS,” ISSCC Dig. Tech Papers, pp. 318-319, Feb. 2003**
- ❑ **J. McNeill, et. al.; “A Split-ADC Architecture for Deterministic Digital Background Calibration of a 16b 1MS/s ADC,” ISSCC Dig. Tech Papers, pp. 276-277, Feb. 2005**

# Data Converter & Mixed Signal Trends: Digitally Compensated Analog

**“Sure, the analog is compromised, but digital is practically free, so fix things up in the digital domain.”**

- ❑ **Reduced headroom and low gain devices mean poor amplifiers, but with sophisticated signal processing, these effects can be digitally compensated/corrected.**
- ❑ **Happening at the system level, not just the circuit level**

## **Examples:**

- ❑ **Transmit Power Amplifier Digital Predistortion Schemes**
- ❑ **B. Murmann, et. al.; “A 12b 75MS/s Pipelined ADC using Open Loop Residue Amplification,” ISSCC Dig. Tech. Papers, pp. 328-329, Feb. 2003**
- ❑ **K.L. Chan, et. al.; “A 14b 100MS/s DAC with Fully Segmented Dynamic Element Matching,” ISSCC Dig. Tech. Papers, pp. 582-583, Feb. 2006**

# Data Converter & Mixed Signal Trends: Shrinking Supply Voltage

“Sure, the supply voltage is low, but I can use current to represent the signal.”

- ❑ Supply voltage doublers and clock boosting techniques are used in ADCs but can such techniques be applied to DACs? Or is there some other circuit tricks that can be applied.
- ❑ High output resistance, low capacitance current sources difficult to achieve with low headroom.
- ❑ Operate devices in sub-threshold.

## Examples:

- ❑ J. Deveugele, et. al.; “A 10b 250MS/s Binary-Weighted Current- Steering DAC” IEEE, J. Solid State Circuits, vol. 41, No. 2 pp. 320-329, February 2006
- ❑ Y. Cong, et. al.; “A 1.5V 14-bit 100 MSPS Self-calibrated DAC”, IEEE, J. Solid State Circuits , vol. 38, No. 12 pp. 2051-2060, December 2003

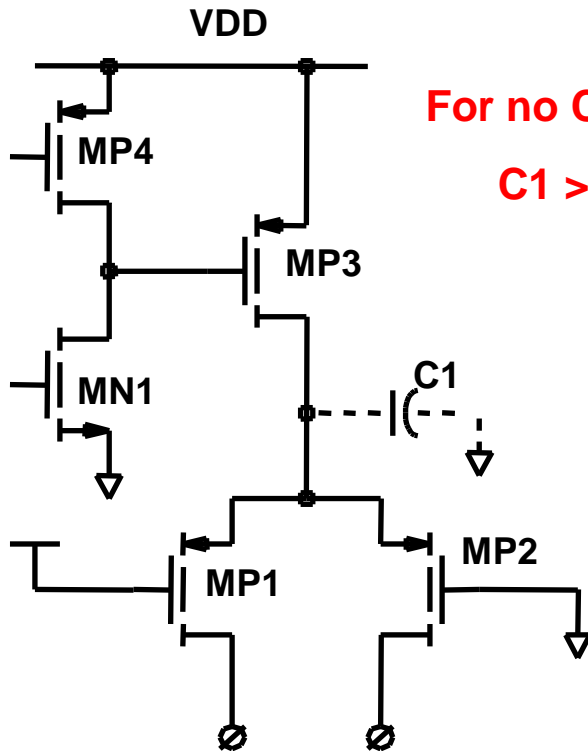
# “Silicon Knows How Big a Volt Is.”

- ❑ Data converters need an accurate, temperature stable voltage reference
- ❑ No obvious zero TC, low voltage device in first bipolar process, or in CMOS
- ❑ Base-emitter voltage of bipolar transistor, predictable over temperature
- ❑ Ratios of resistors and junction area are insensitive to process variations
  - ❑ Port to CMOS: substrate PNPs are “free” ( deep Nwell NPN )
  - ❑ Digital trimming improves accuracy, reduces TC

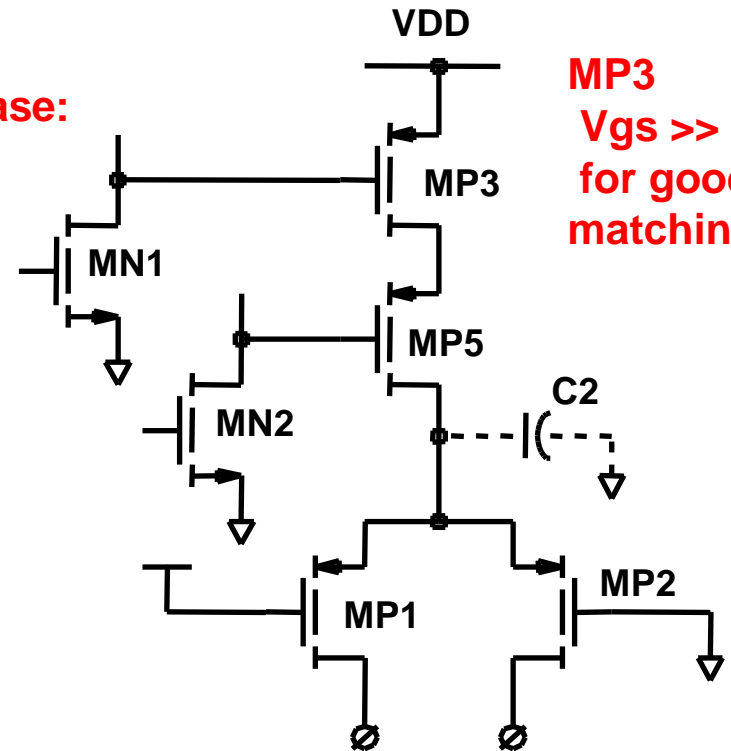
$$V_{out} = V_{BE} + 2 \frac{R_1}{R_2} \frac{kT}{q} \ln \frac{A_1}{A_2} \approx 1.2V$$

Paul Brokaw, October 2006

# Lower Limits on Supply Voltage in Deep Submicron CMOS – ( basic DAC cell )



For no Cascode Case:  
 $C1 \gg C2$



MP3  
 $V_{gs} \gg V_t$   
 for good matching

Case without cascode:

$$V_{dd} > V_{gs} (MP2) + V_{dsat} (MP3) \text{ or}$$

$$V_{dd} > V_{gs} (MP3) + V_{dsat} (MN1)$$

Case with cascode:

$$V_{dd} > V_{gs} (MP2) + 2 * V_{dsat} (MP3,MP5)$$

$$V_{dd} > V_{gs} (MP5) + 2 * V_{dsat} (MN2,MP3)$$

# Data Converter & Mixed Signal Trends: Higher Sample Rates

**“Sure, you lose dynamic range, and everything leaks, but boy, can you go fast.”**

- ❑ **Exploits the natural strengths of very deep submicron technology**
- ❑ **Oversampling techniques applied to a broader class of applications**
- ❑ **New applications (UWB) lean towards bandwidth over dynamic range to expand “Shannon’s box”**

## **Examples:**

- ❑ **G. Mitteregger et. al.; “A 14b 20mW 640MHz CMOS CT Delta Sigma ADC with 20MHz Signal Bandwidth and 12b ENOB,” ISSCC Dig. Tech Papers, pp. 62-63, Feb. 2006**
- ❑ **D. Baranaukas, et. al.; “A 0.36W 6b up to 20GS/S DAC for UWB Wave Formation, “ ISSCC Dig. Tech Papers, pp. 580-581, Feb. 2006**

# Data Converter & Mixed Signal Trends: DACs that can reconstruct signals at higher and higher output frequencies

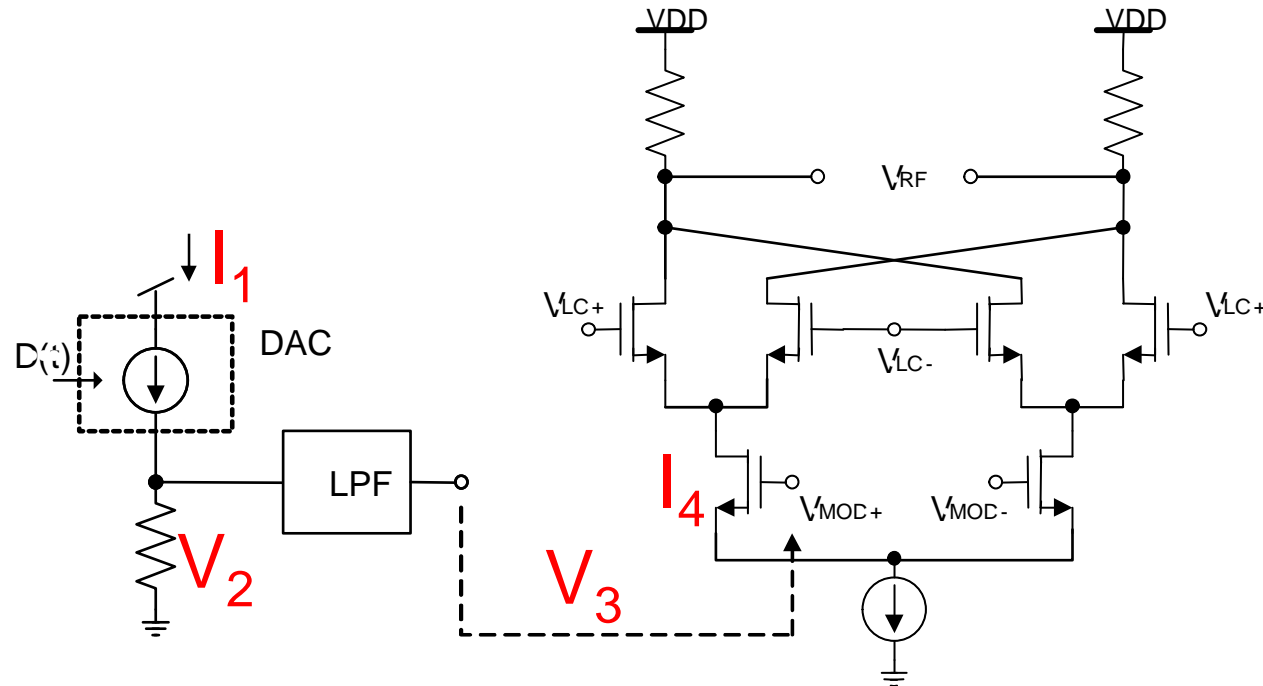
“Deep sub-micron devices have extremely high  $f_T$ ,  
Why not use it?”

- ❑ Increase sample rate.
- ❑ Use 2<sup>nd</sup> and 3<sup>rd</sup> Nyquist zones ( RTZ DACs )
- ❑ Pulse output DACs
- ❑ Up-conversion “Mixer” DAC

## Examples:

- ❑ B. Schafferer, et. al. ; "A 14b 1.4 GS/s 3V CMOS DAC for Multi- Carrier Applications;" ISSCC Digest of Technical Papers, February 2004
- ❑ S. Luschas, et. al. ; “A 942 MHz Output, 17.5 MHz Bandwidth, -70dBc IMD3  $\Sigma\Delta$  DAC”, CICC Digest of Technical Papers Sept. 2003 pg.131

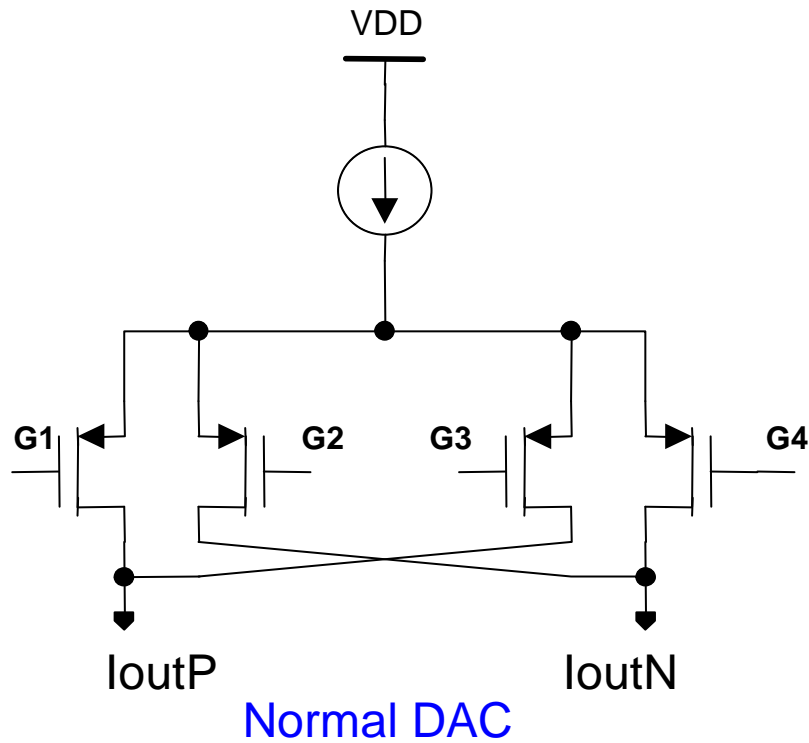
# Up-conversion with Gilbert Mixer



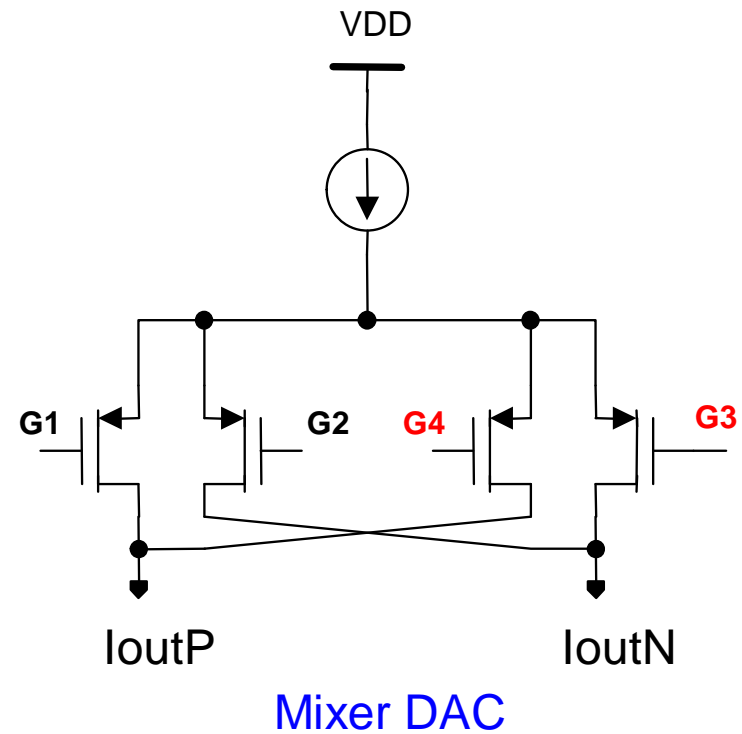
- ❑ LPF cannot be integrated
- ❑ I to V and back to I conversion
- ❑  $V_3$  to  $I_4$  conversion cause distortion



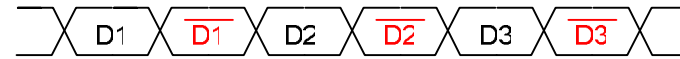
# Quad-Switch - Mixer DAC



Normal DAC  $I_{outP} = I_{out1} + I_{out3}$



Mixer DAC  $I_{outP} = I_{out1} + I_{out4}$



# Conclusion: Future of Analog is Secure

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