# Directions for Ultra-Wideband ADCs

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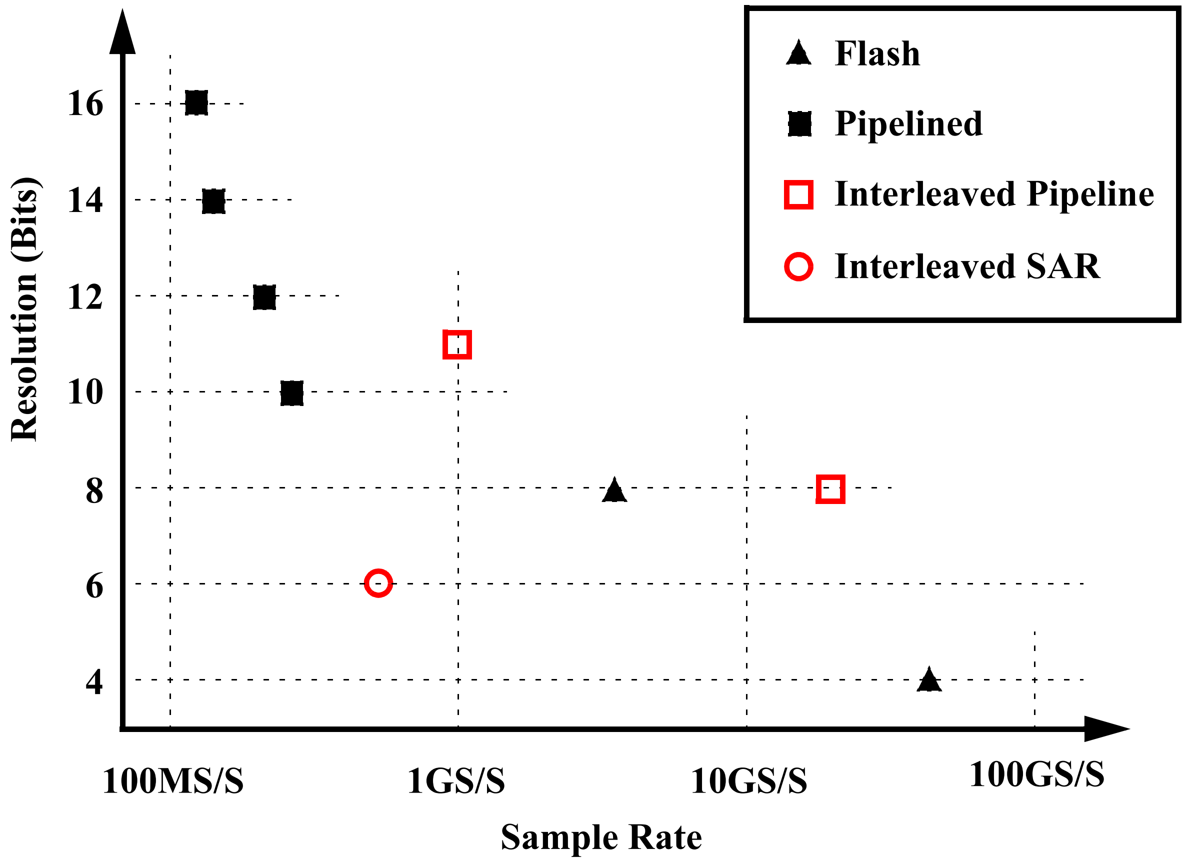
# Current CMOS ADC Performance



# Architectures for High-Resolution Wideband ADCs

$f_{BW} \geq 500\,\mathrm{MHz}$ $\qquad$ $N \geq 6$-bits

**Flash:**

- includes sub-ranging techniques

**Pipelined:**

- mainly Switched Capacitor based, some Switched Current

**Interleaved:**

- a system approach

# Flash ADCs: Basic Operation

**Objective:** **Compare input to all levels simultaneously**

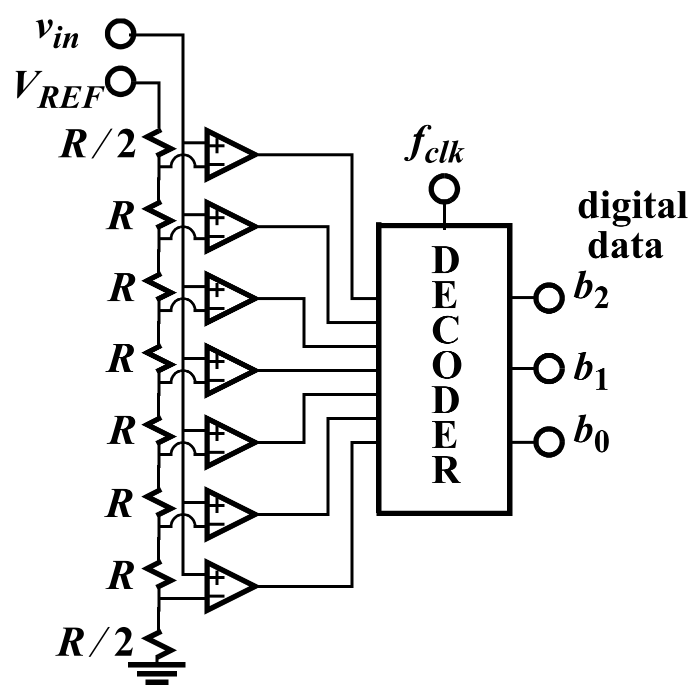
**Fast:**

- **speed:** $f_s = f_{clk}$
- $f_{clk}$ **~ Latch Speed**

**Expensive:**

- **hardware & power:**

  $\alpha\ 2^N$



# Flash ADC Design Requirements

**Speed:**

- **comparator and pre-amp settling limit speed**

$$f_s \propto \frac{g_m}{2\pi C_{gs}} \propto \frac{1}{L}\sqrt{\frac{I_{BIAS}}{WLC_{ox}}}$$

**Accuracy:**

- **comparator and pre-amp offsets limit accuracy**

$$2^N \propto \frac{V_{DD}}{\sigma_{\Delta V_{gs}}} \propto \frac{V_{DD}}{A_{Vt}}\sqrt{W \cdot L}$$

- **devices are small for speed *versus* large for accuracy**

# Flash ADC Power Limitations

**Power:**

$$\textbf{Power} \propto f_s^2 2^{2N} \left[ \frac{L^2 C_{ox} A_{Vt}^2}{V_{DD}} \right]$$

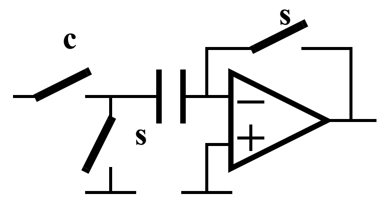
- **speed extracts a hugh power penalty**
  - motivates interleaving
- **mismatches have a large impact**
  - need better design approaches

# Solutions to the Mismatch Limitations

**Analog Solutions:**

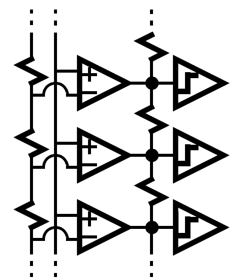
- **auto-zeroing**

  - sample and cancel the offset




- **averaging (Kattmann *ISSCC'91*)**

  - offset is the average of the offsets



**Digital Solutions:**

- **digital calibration**
- **redundancy**

  - 1 device, $\sigma = 1/2$, Prob(offset < 1/2) = 70%

  or for the same area:

  - 4 devices, $\sigma = 1$, Prob(offset < 1/2) = 85%

# High-Speed Flash ADCs

**4 - 6-bit ADCs:**

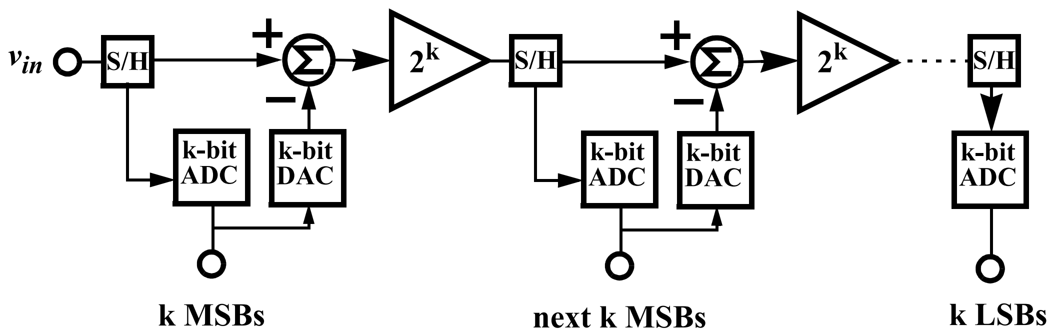
- **analog solutions**
  - exploit area & averaging for matching

**8-bit ADCs:**

- **calibration to minimize size & capacitive loading**

# Pipelined ADCs: Basic Operation

**Objective:** work on multiple samples simultaneously use "M" stages and M - N/M bit ADCs




- low-resolution stages for simplicity and speed
- inter-stage gain for hardware reuse and speed
- fewer bits/stage simplifies the design

# Pipelined ADC Design Requirements

**Accuracy:**

- **solved with digital error correction and calibration**

**SNR:**

- **sampling leads to thermal noise limitations**

$$C_L = \frac{2kT2^{2N}}{V_{sig}^2}$$

**Speed:**

- **high-speed operation is limited by linear settling**

$$f_s \propto \frac{g_m}{NC_L} \propto \frac{\sqrt{I_{BIAS}}}{NC_L}$$

# Pipelined ADC Power Limitations

**Power:**

$$\text{Power} \propto f_s^2 N^2 2^{2N} \left[ \frac{C_L}{V_{DD}} \right]$$

- **speed extracts a hugh power penalty (once again)**
  - motivates interleaving
- **increasing resolution (*i.e. N)* has a large impact**
  - could use slew - limited settling to achieve

$$\text{Power} \propto f_s 2^{2N}$$

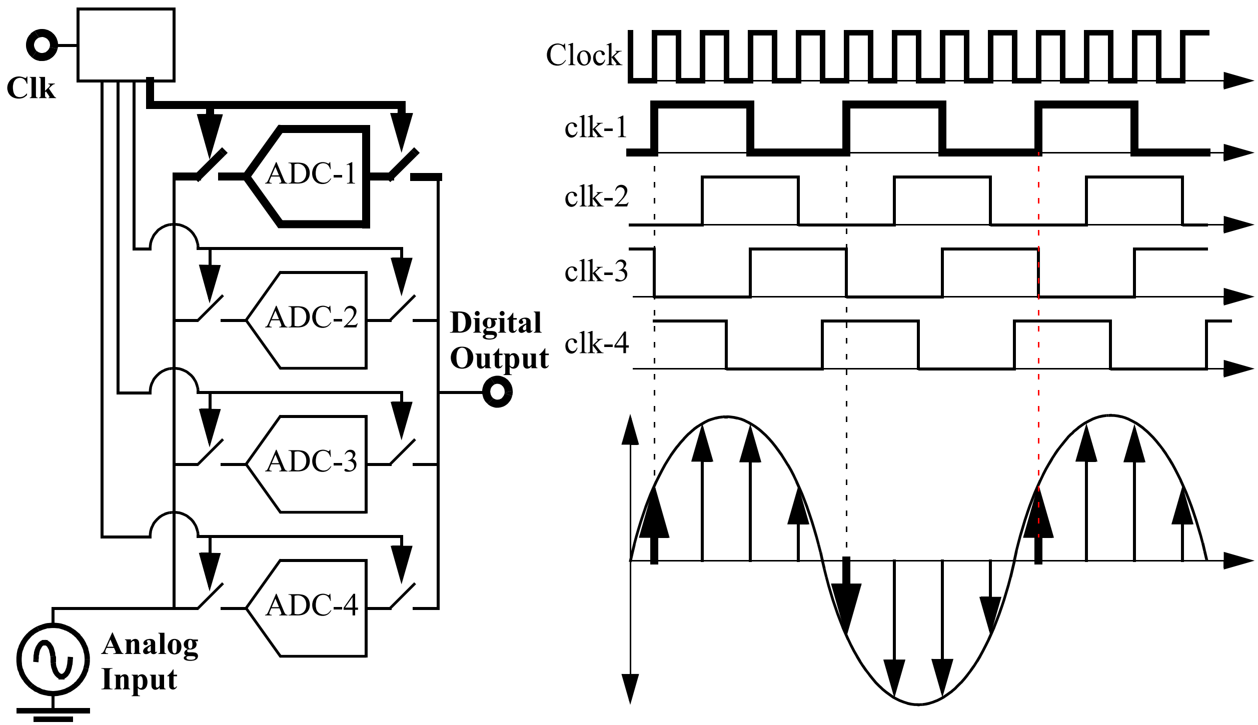
# High-Speed Pipelined ADCs

**Alternate Amplifier Designs:**

- **fast low-gain amplifiers (Hernes, *ISSCC'07*)**
  - resulting gain error can be calibrated
- **comparator based op amps (Sepke, *ISSCC'06)***
  - leads to slew like settling behaviour
- **open-loop gain stages (Murmann, *ISSCC'03*)**
  - non-linear gain must be calibrated

# Interleaved ADCs: Basic Concepts

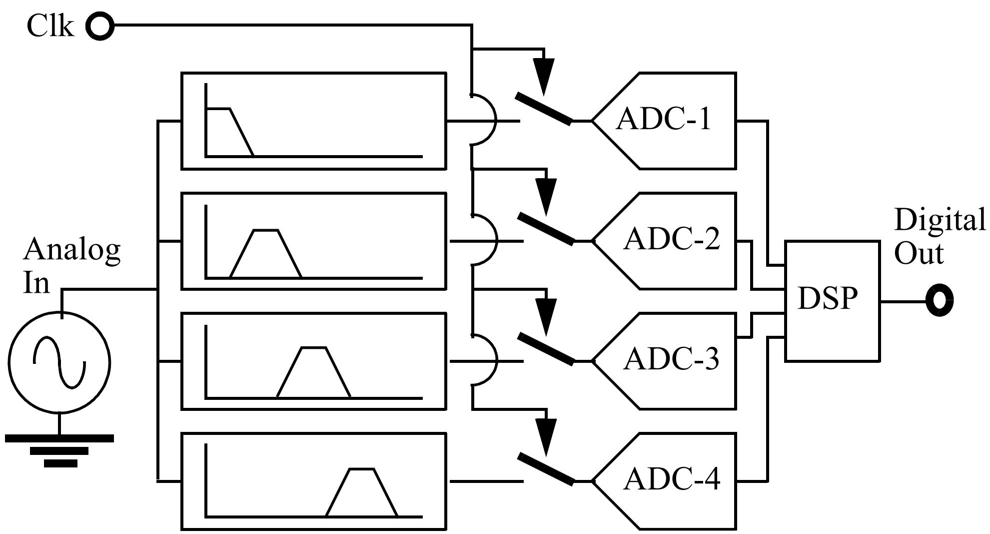
- use a collection of “slow” ADCs to make a “fast” ADC
- also known as “ping-ponged” or parallel ADCs



# Other Approaches to Interleaving

- **many alternatives**

## Band-Splitting




- **DSP recombines the ADC outputs**

# Why so few Interleaved ADCs?

1) Complexity

- large numbers of ADCs require a large area
- CMOS VLSI helps

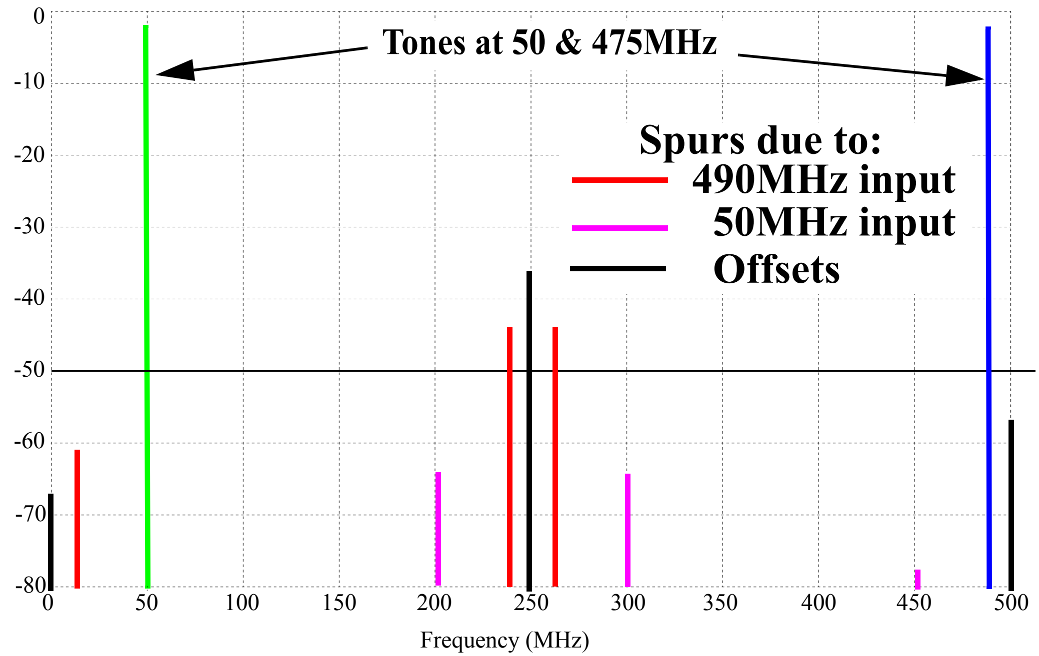
2) Channel matching

- very small channel-to-channel mismatches are significant
- calibration is essential

3) Bandwidth requirements

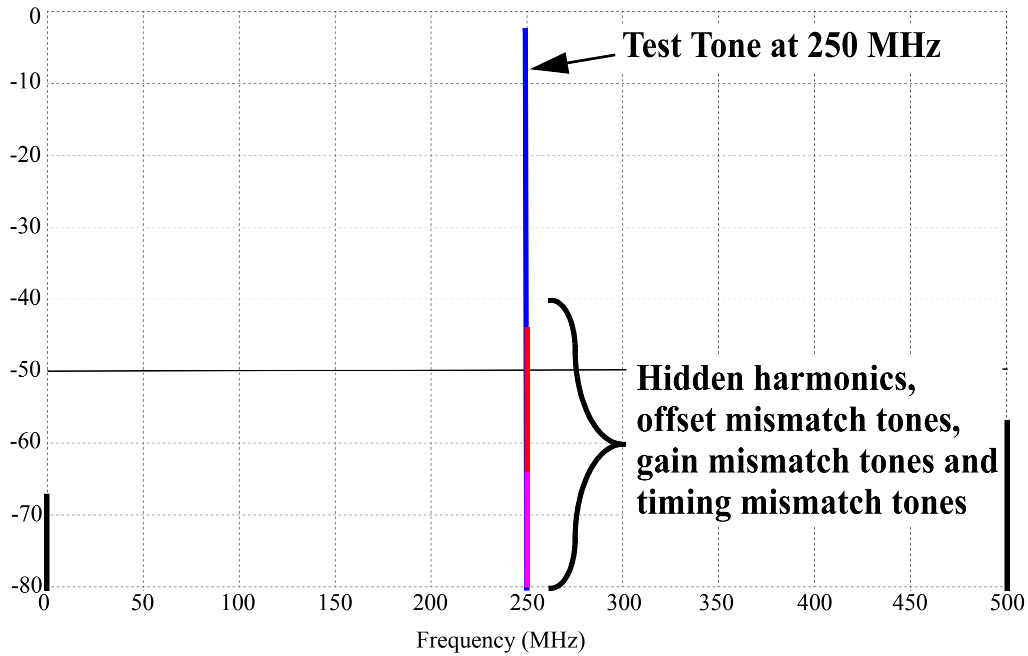
- ADC input bandwidth must exceed the Nyquist rate

# A Sample of What Mismatches Do



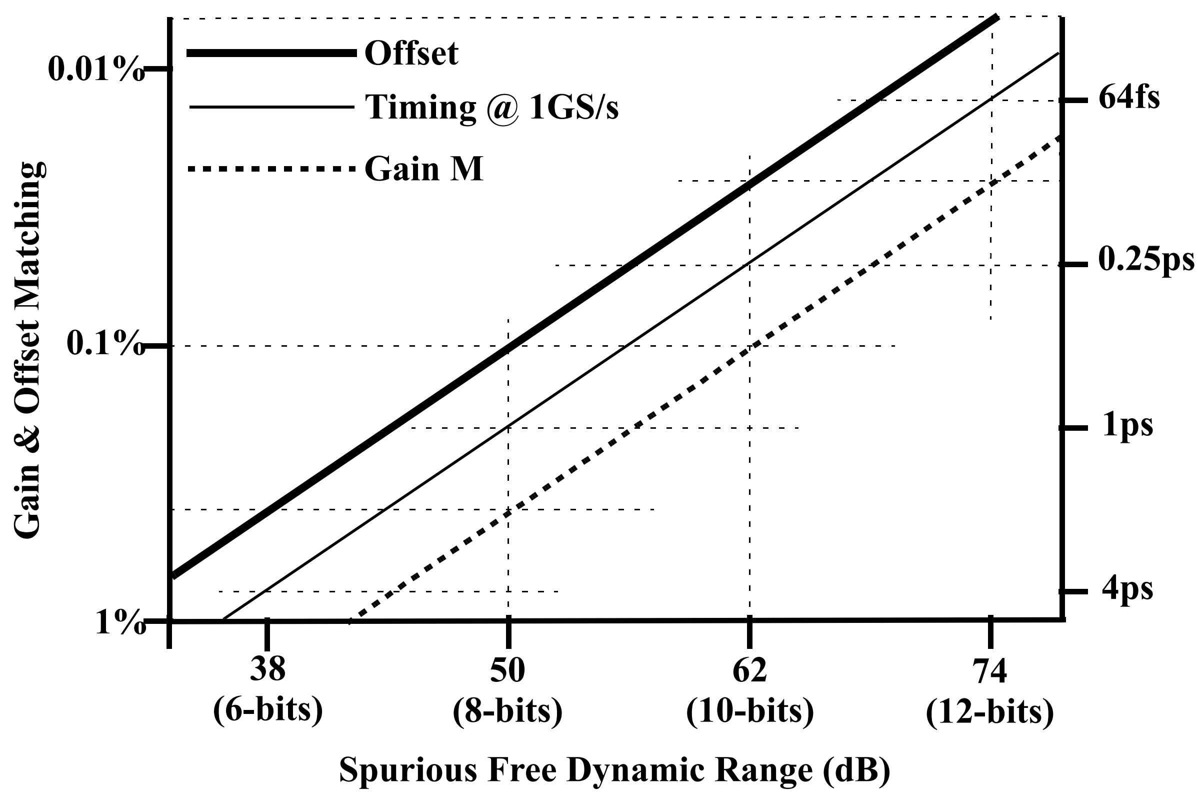

- 4, 250MSPS ADCs to achieve 1GSPS,
- offsets ~ 0.4%, timing skew 5ps

# Hiding Mismatches!




- test tone at $f_s/4$
- same offsets and timing skews as before

# Matching Requirements for Interleaving



# Correcting Offset and Gain Mismatches

**Offsets:**

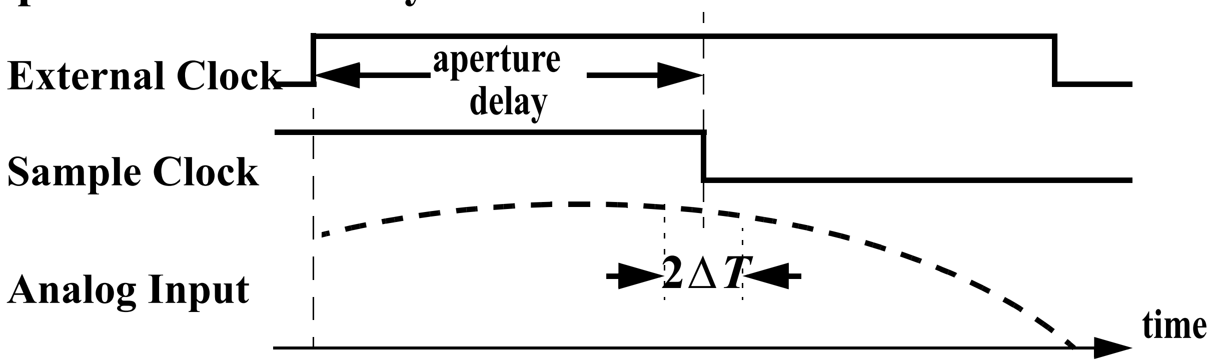
- **estimate with averaging**
- **correct with**
  - random chopping (Ekland, *ISCAS* 2000)
  - digital correction

**Gain:**

- **estimate with average or RMS power**
- **correct with:**
  - trim reference (Hummels, *Inst. & Meas. Conf. 1996)*
  - digital multiply

# Correcting Timing Skew

**Aperture Uncertainty:**




**Correction:**

- **estimate with correlation & frequency analysis**
- **correct with**
  - digital filtering!
  - analog timing skew adjustment

# Choosing ADCs for Interleaving

**Fast ADCs:**

- **minimizes number of ADCs required and complexity**
  - flash for 8-bit performance
  - pipelined for > 8-bit performance

**Small low-power ADCs:**

- **reduces power and die area**
  - successive approximation is attractive

# Directions for Ultra-Wideband ADCs

**Simplest Solution:**

- **single ADCs minimize complexity**
  - flash with calibration
  - pipelined with innovative amplifiers

**Lowest Power Solution:**

- **interleaving breaks the Power $\propto f_s^2$ barrier**
  - selection and design of an optimal underlying ADC