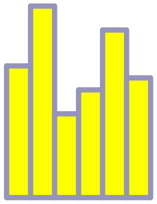
RECONFIGURABLE RECEIVERS FOR NEXT-GENERATION WIRELESS APPLICATIONS

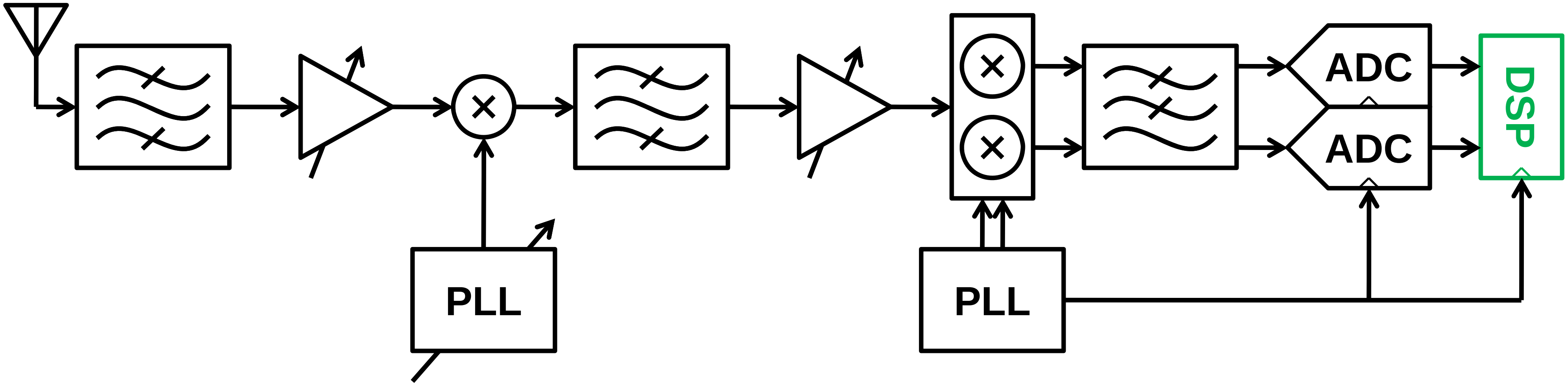
Tony Chan Carusone
Associate Professor

Kentaro Yamamoto
Ph.D. Candidate

University of Toronto
Electrical and Computer Engineering

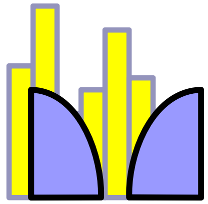
Conventional Wireless Receiver

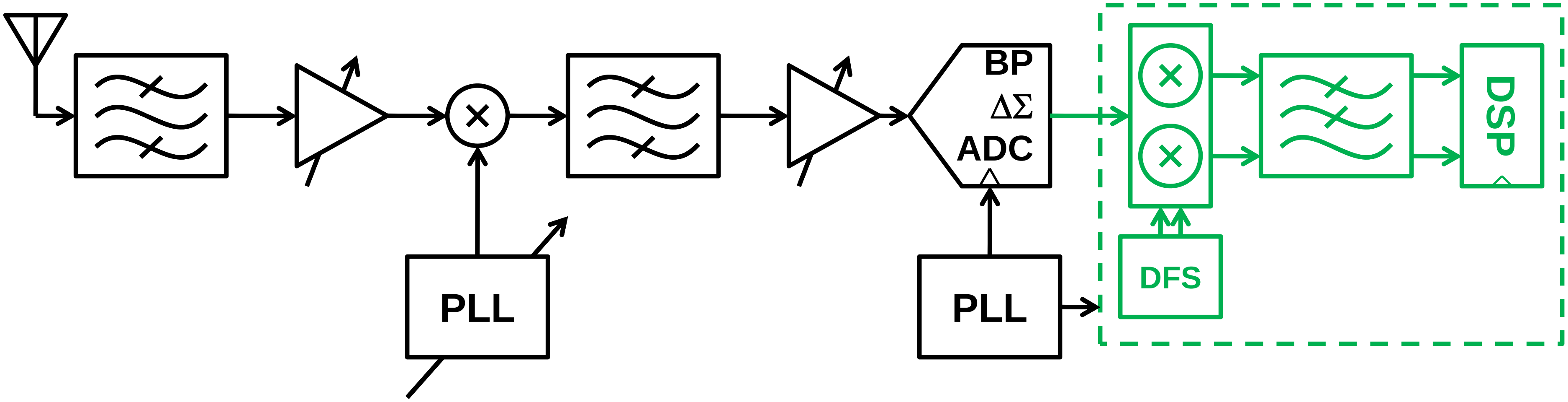




Digital Channel Selection

Digitization of one channel at a fixed-IF

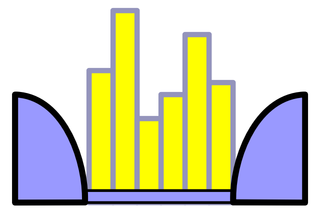


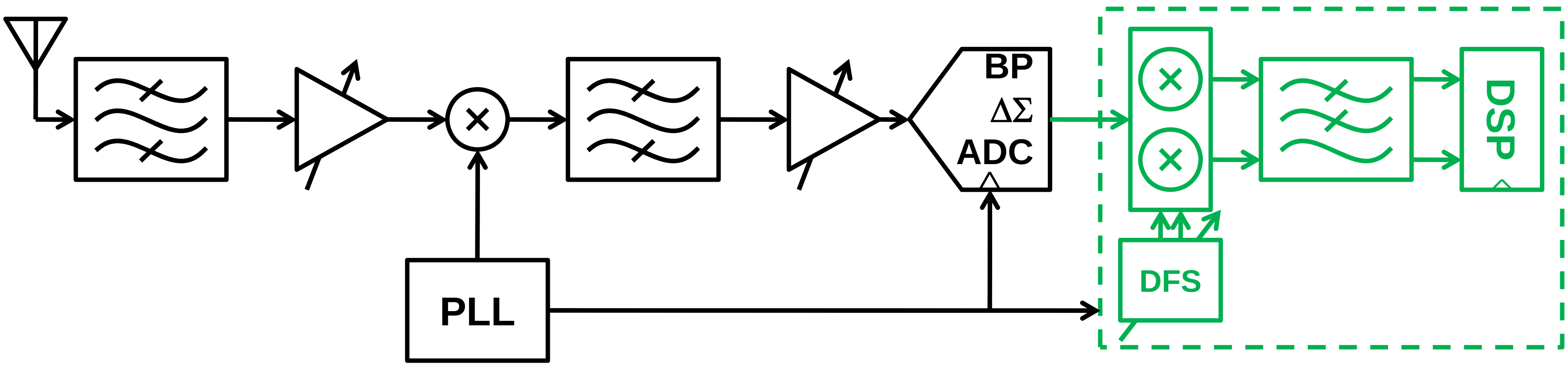


e.g. Sala et al., JSSC Jul. 2004

Digital Channel Selection

Digitization of all channels

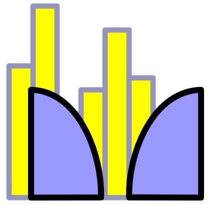


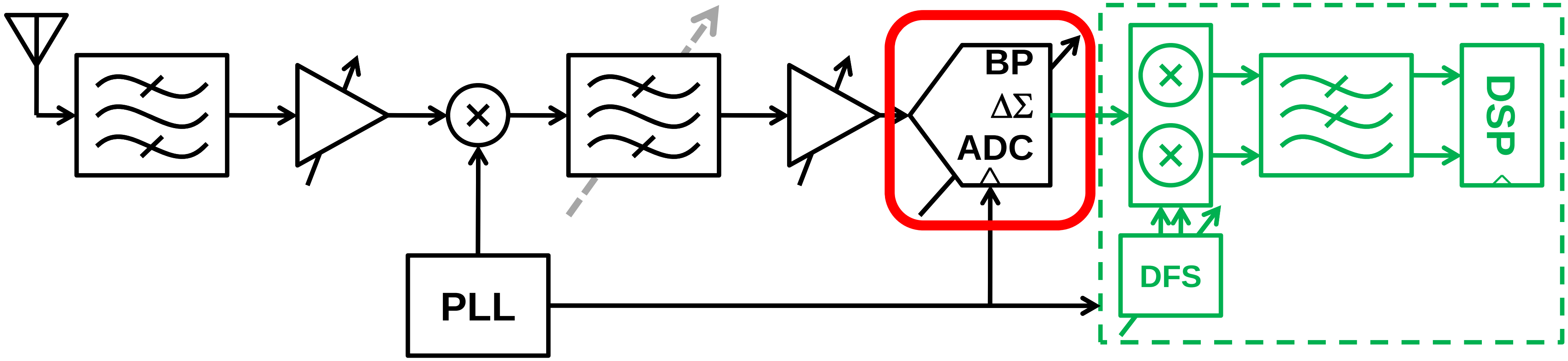


e.g. Breems et al., JSSC Dec. 2007

Digital Channel Selection

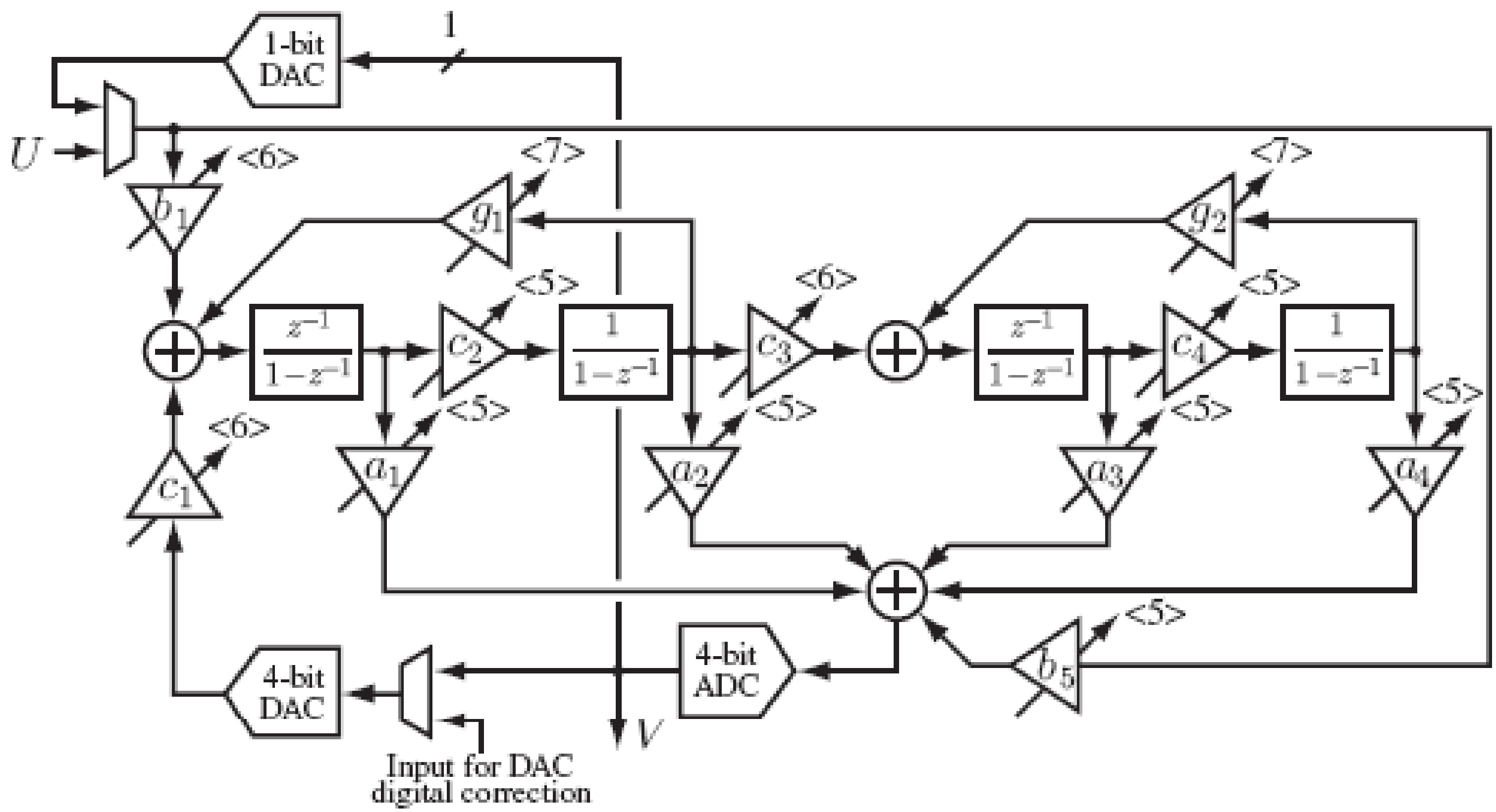
Digitization of one channel at a variable-IF





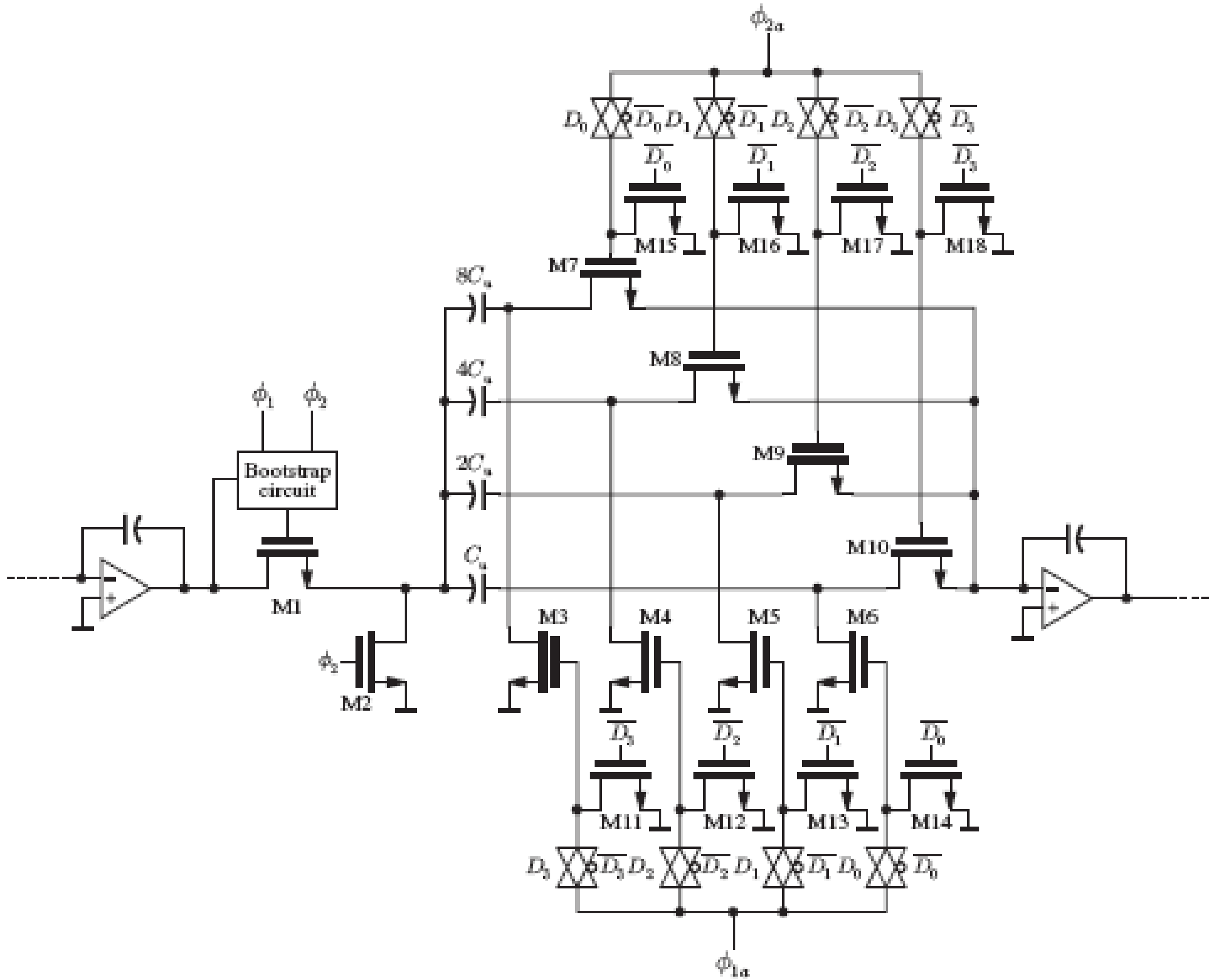
Objective: To provide a programmable passband with a performance comparable to state-of-the-art fixed-passband modulators

Modulator Architecture



CRFF architecture provides a programmable centre-frequency with the fewer programmable gains than a CRFB

Programmable Modulator Coefficients



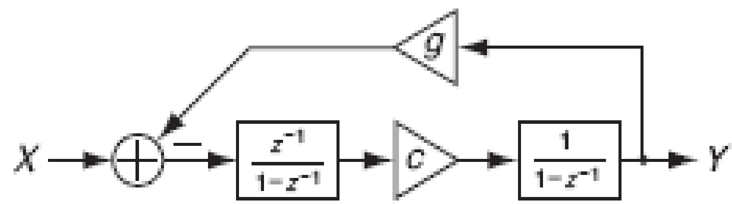
Quantization of the integrator gains introduces some overhead in the design

⇒ Want to minimize the resolution required to quantize each of the coefficients without sacrificing performance

Quantization of the Coefficients

- The modulator's SQNR is most sensitive to the accuracy of the resonant frequency of the resonators

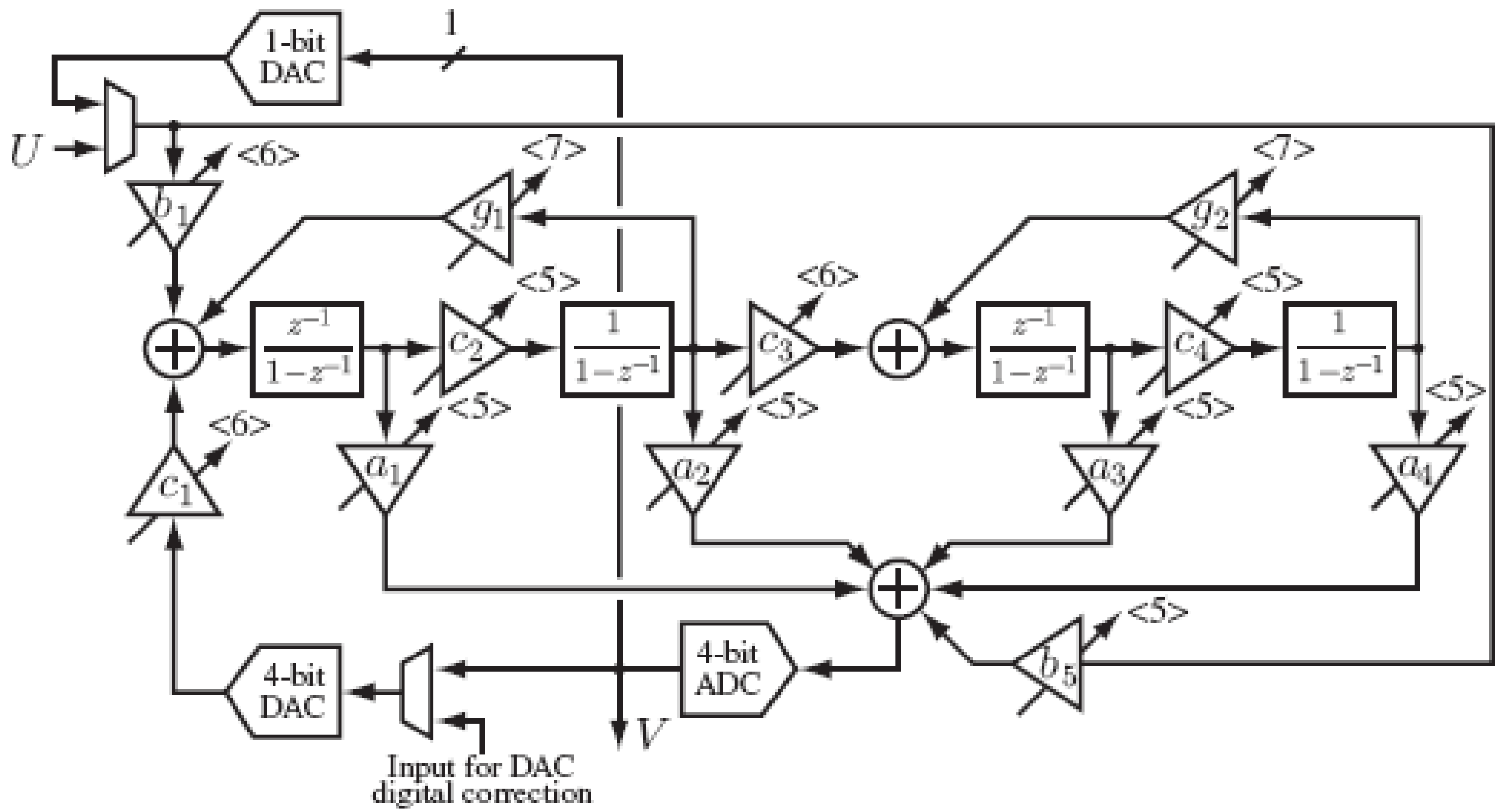
$$\omega_r = \tan^{-1}\frac{\sqrt{4cg-(cg)^2}}{2-cg}$$



- These only depend upon the product (*cg*), not on *c* or *g* individually

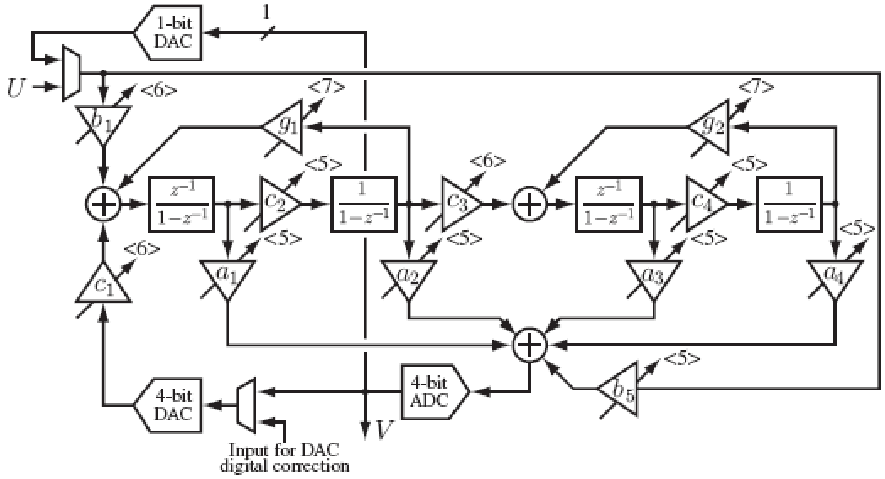
- It is possible to quantize one coarsely
- Then, quantize the other with more resolution in order to accurately set (*cg*)

Modulator Architecture



Quantization of the coefficients does not limit the modulator`s performance

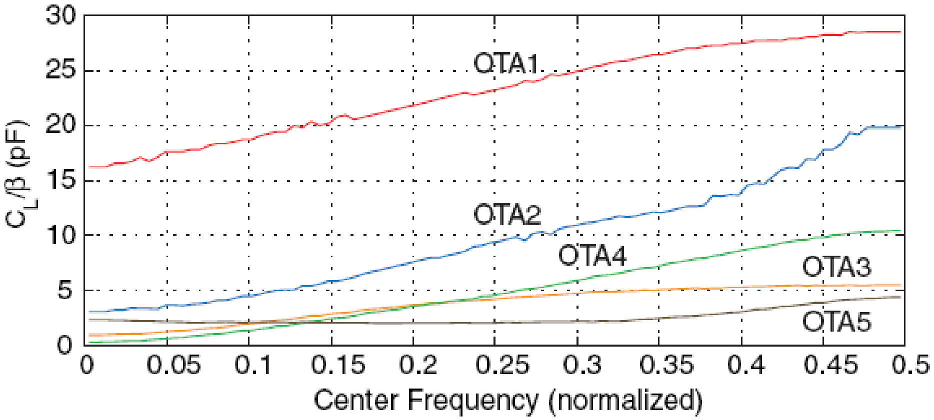
OTA compensation



- Settling time-constant at the OTA outputs:

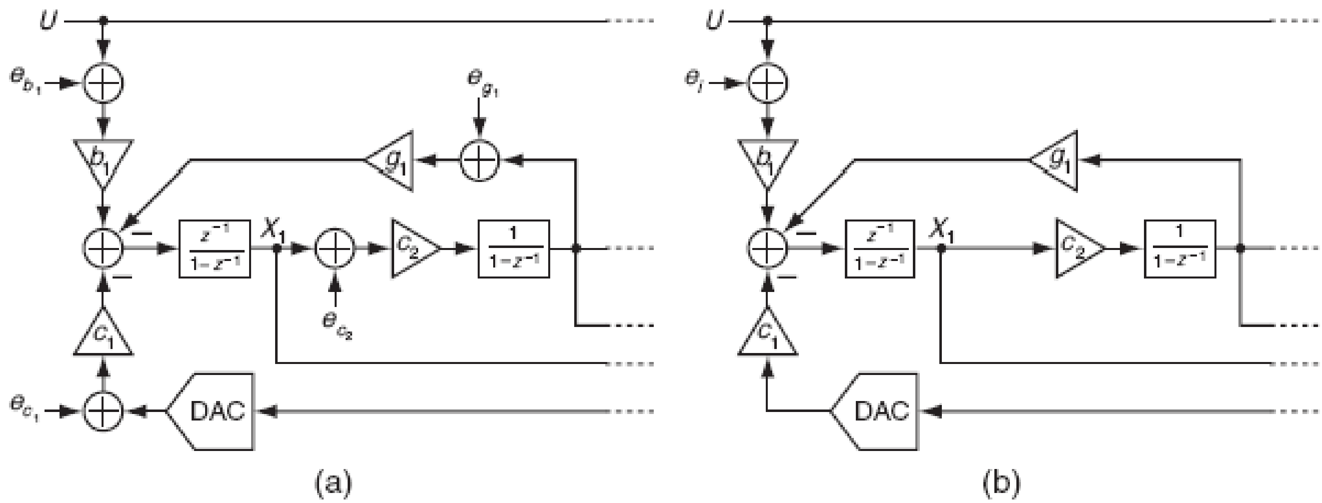
$$\tau = \frac{C_L}{\beta g_m}$$

- OTAs have to be designed for the worst-case, which arises at high centre frequencies
- Difficult to achieve competitive performance at lower center frequencies



Thermal Noise Analysis

The thermal noise in the first resonator dominates the noise floor of the modulator.

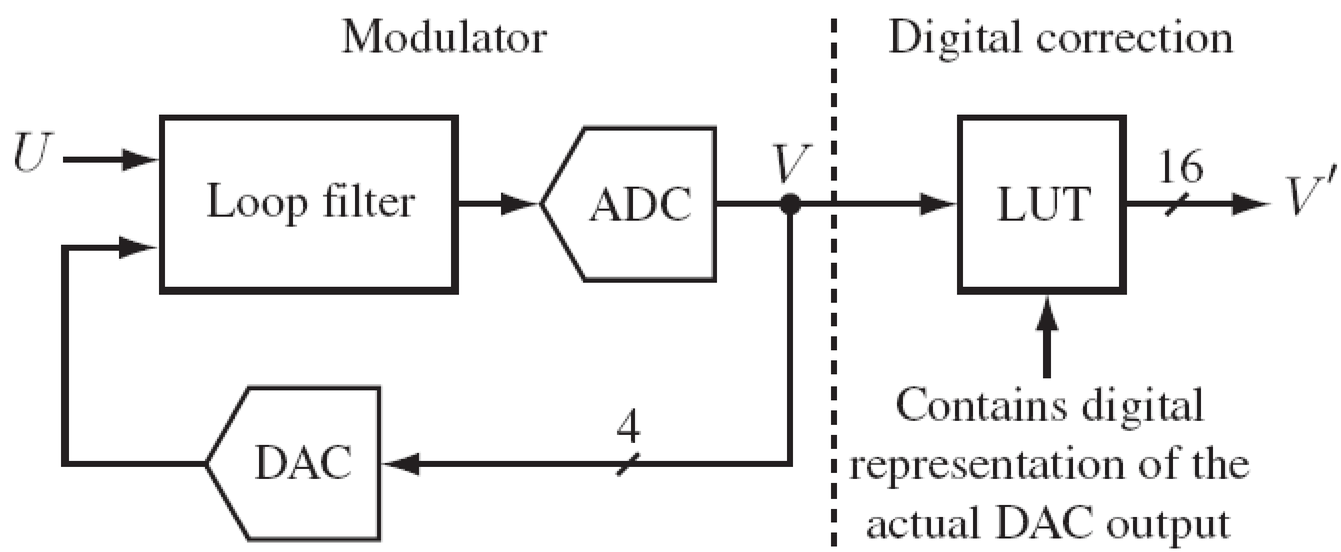


The thermal noises can be referred to the input of the modulator as

$$\overline{e_i^2} = \frac{4kT}{OSR}\left[\frac{2}{n_{b_1}C_{u1}} + \left(\frac{n_{g_1}}{n_{b_1}^2 C_{u1}} + \frac{\left|1-e^{-j2\pi f_c}\right|^2}{b_1^2 n_{c_2} C_{u2}}\right)\right]$$

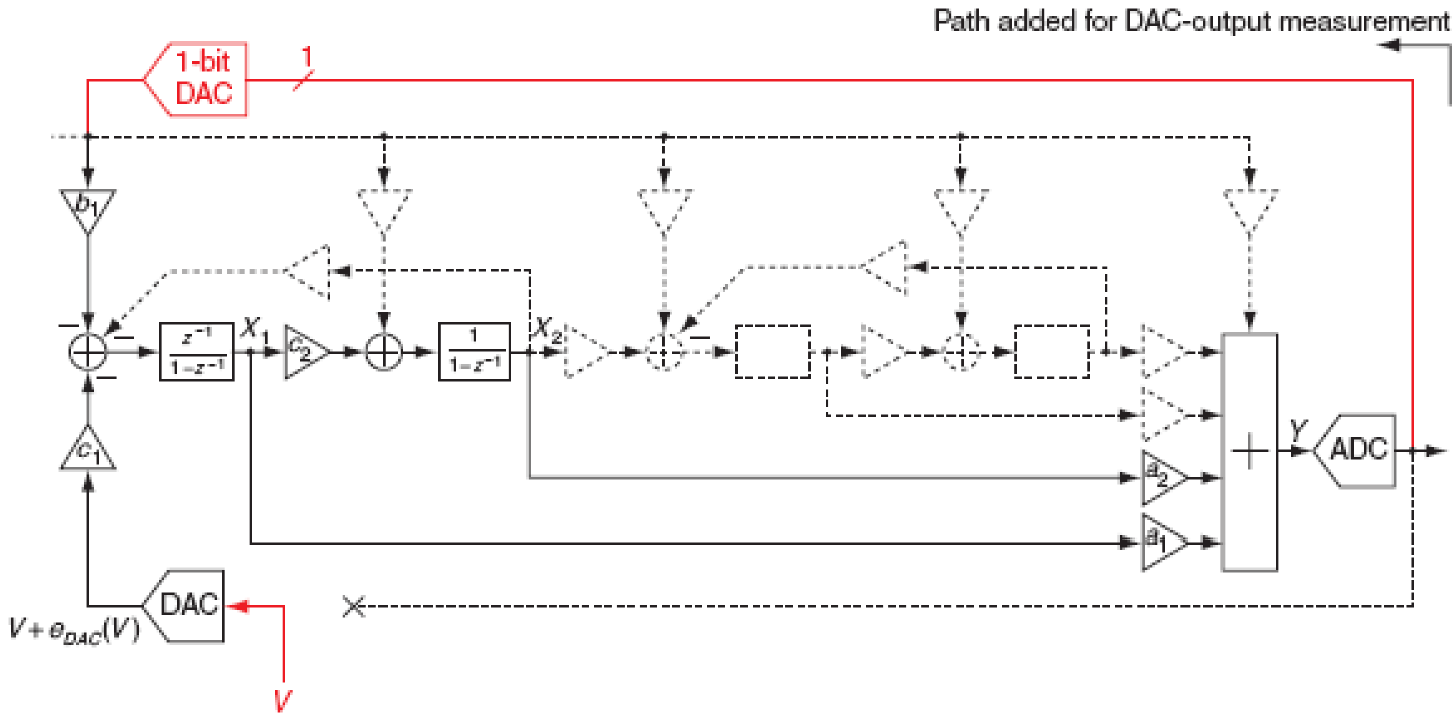
DAC Nonlinearity Compensation

Dynamic element matching would have been complicated since the passband is programmable



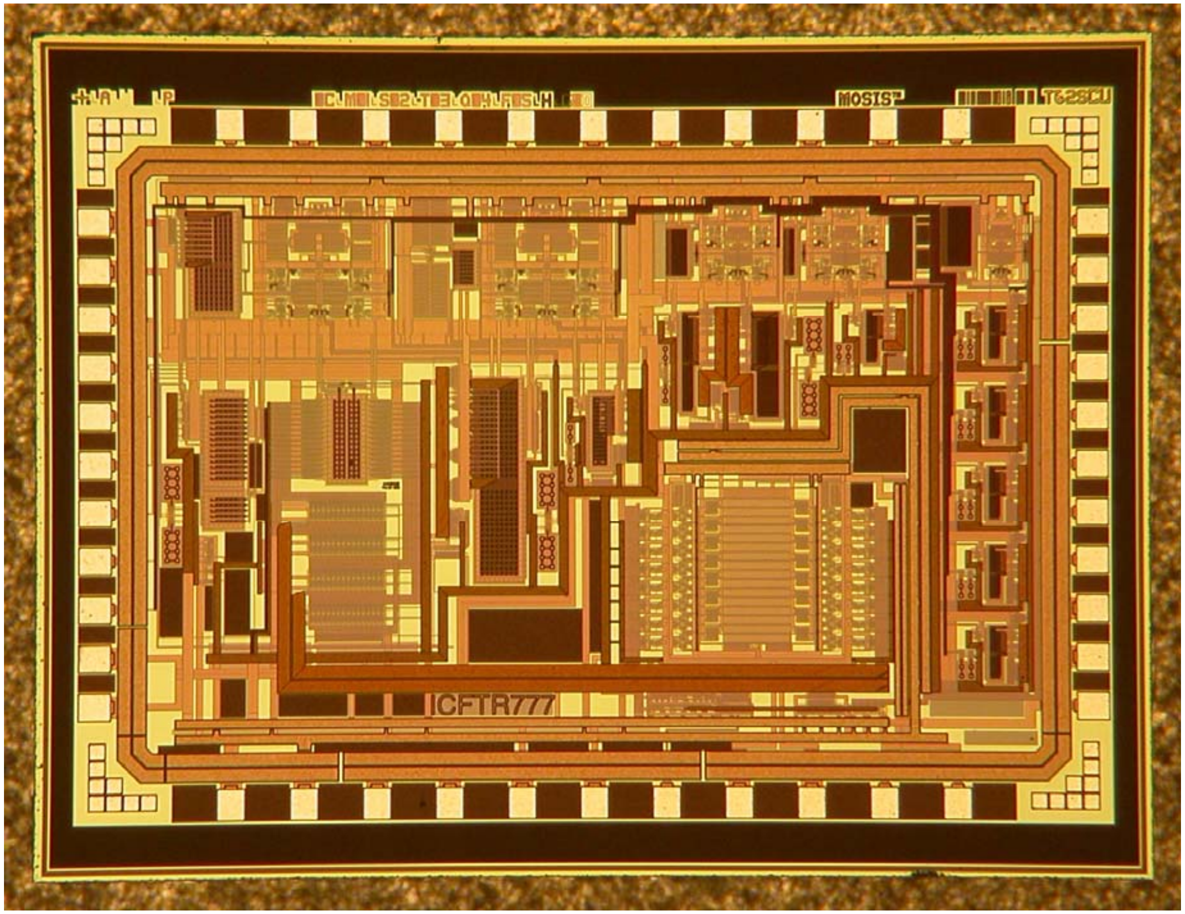
Instead, DAC nonlinearity can be digitally corrected with a lookup table

DAC Calibration



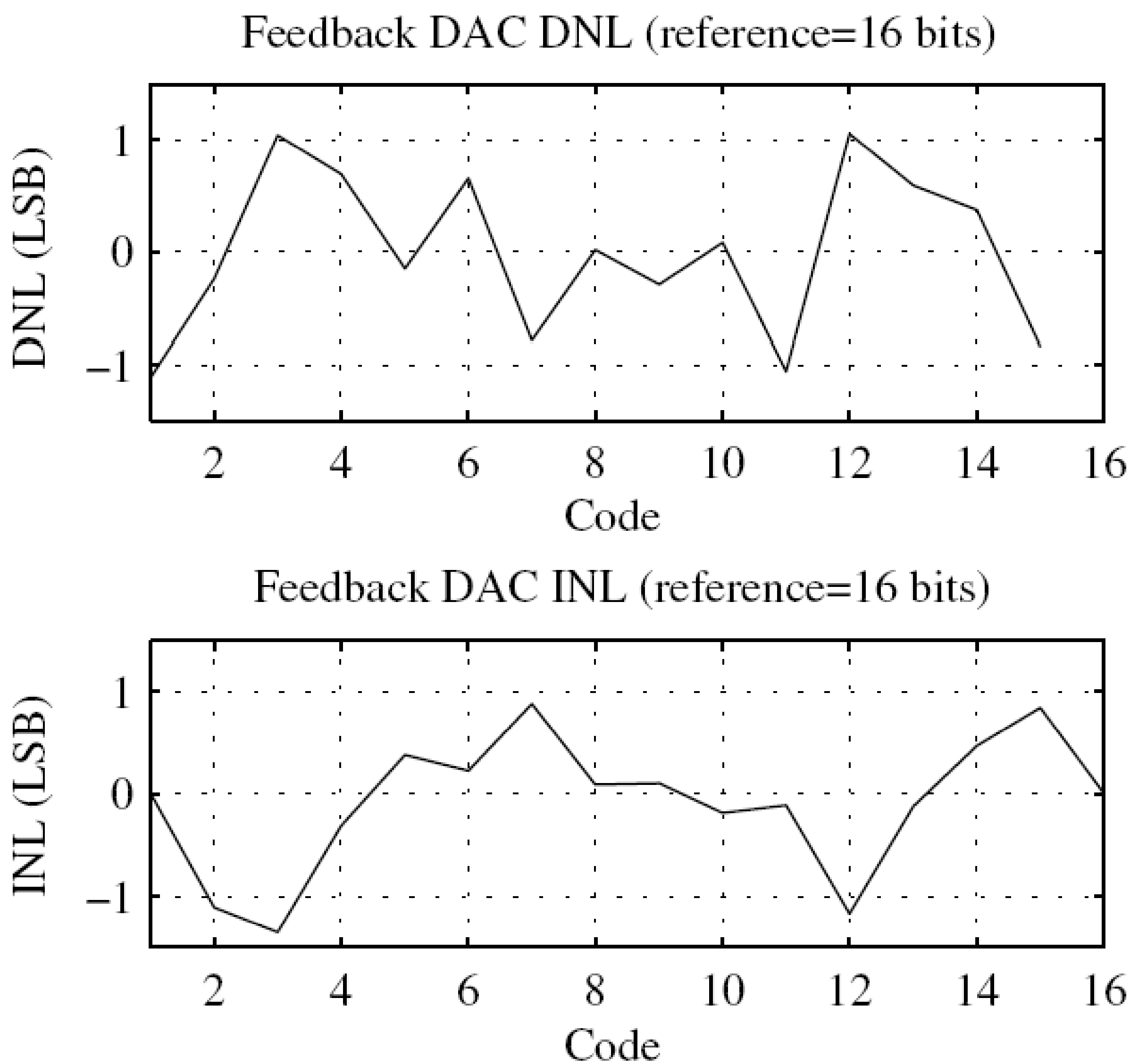
DAC calibration is accommodated taking advantage of the modulator`s programmability with little additional overhead

Die Photo

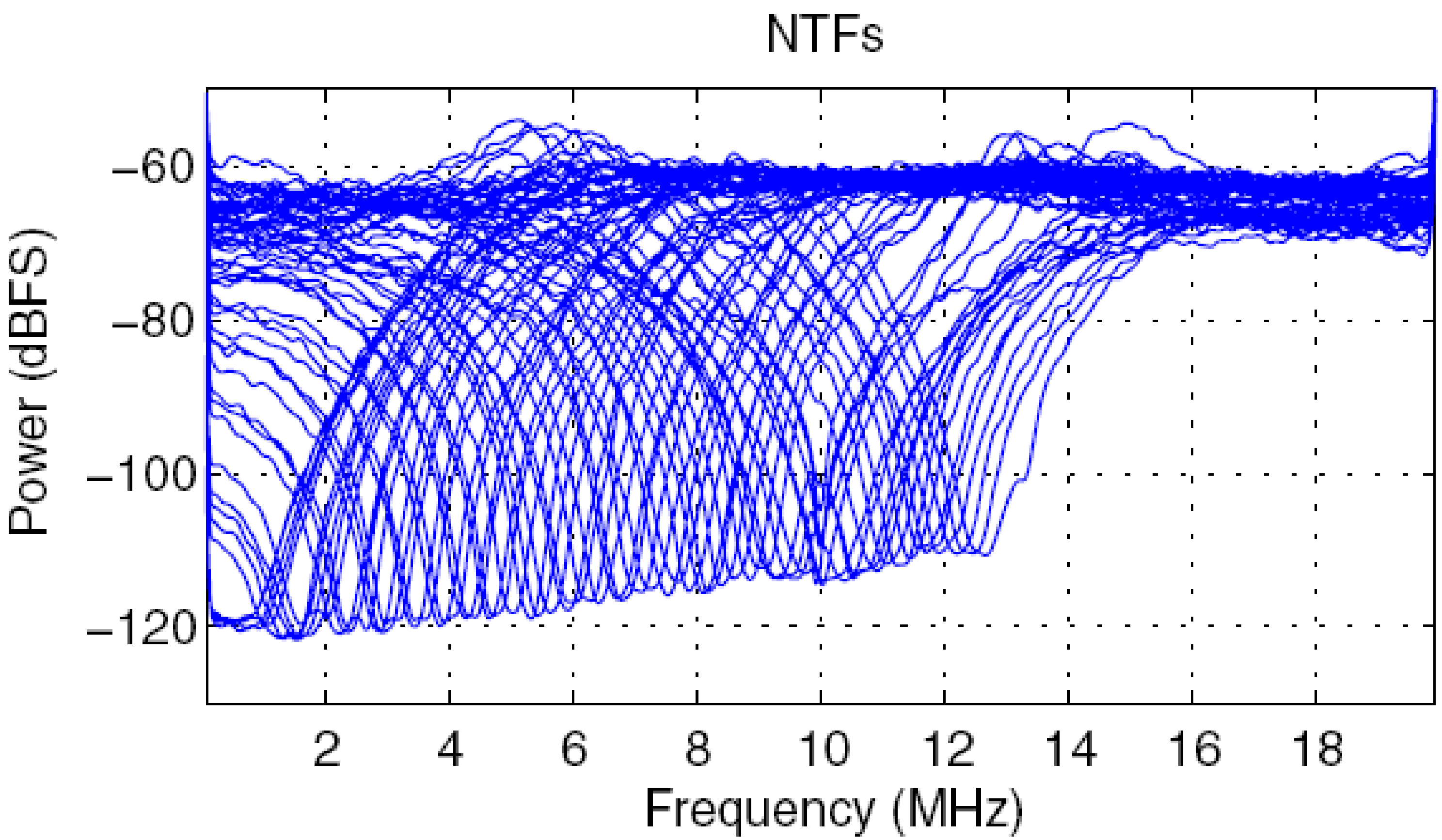


2.5 mm x 2 mm in 0.18-μm CMOS

Measured DAC Nonlinearity



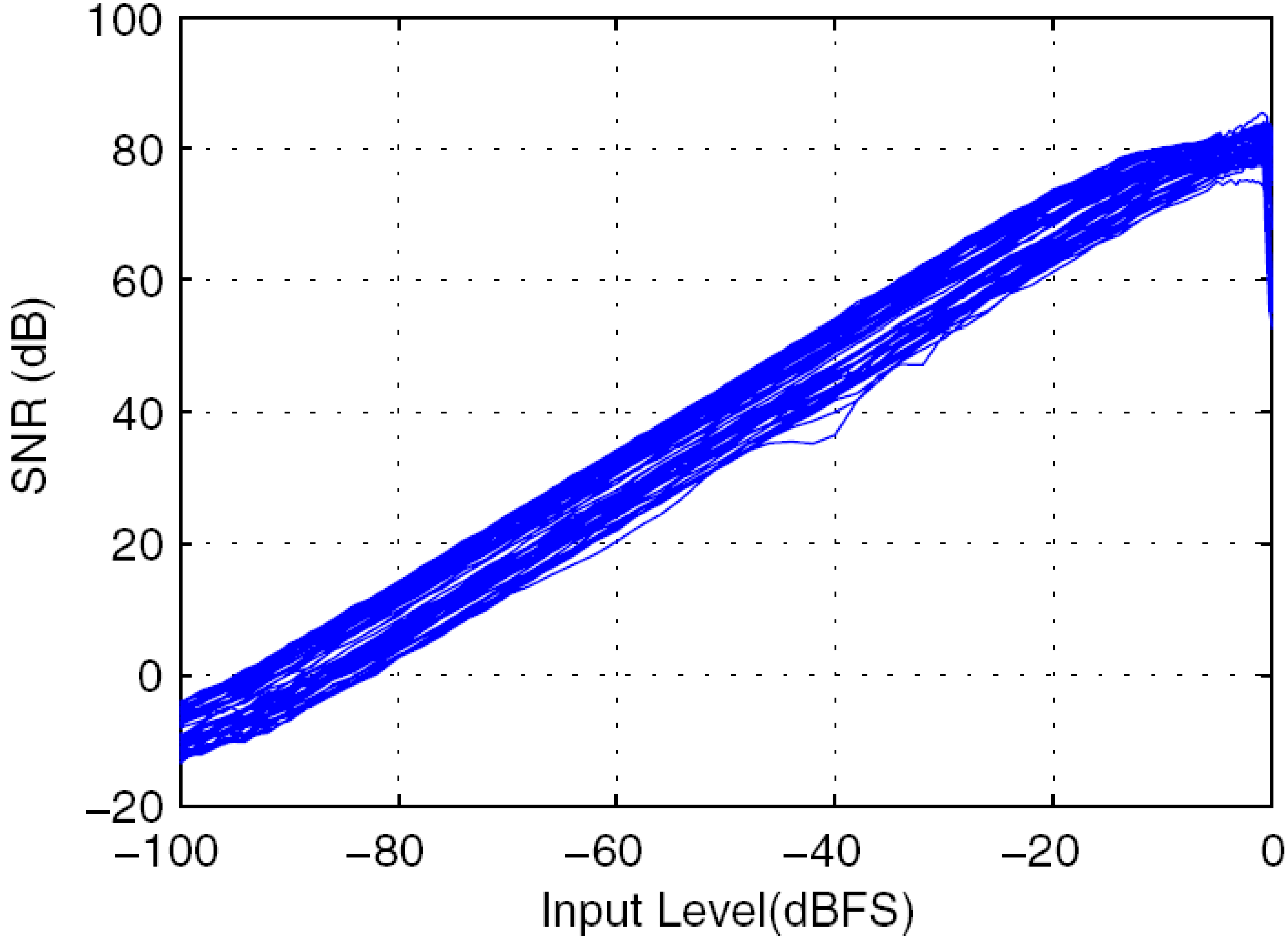
Centre-Frequency Programmability



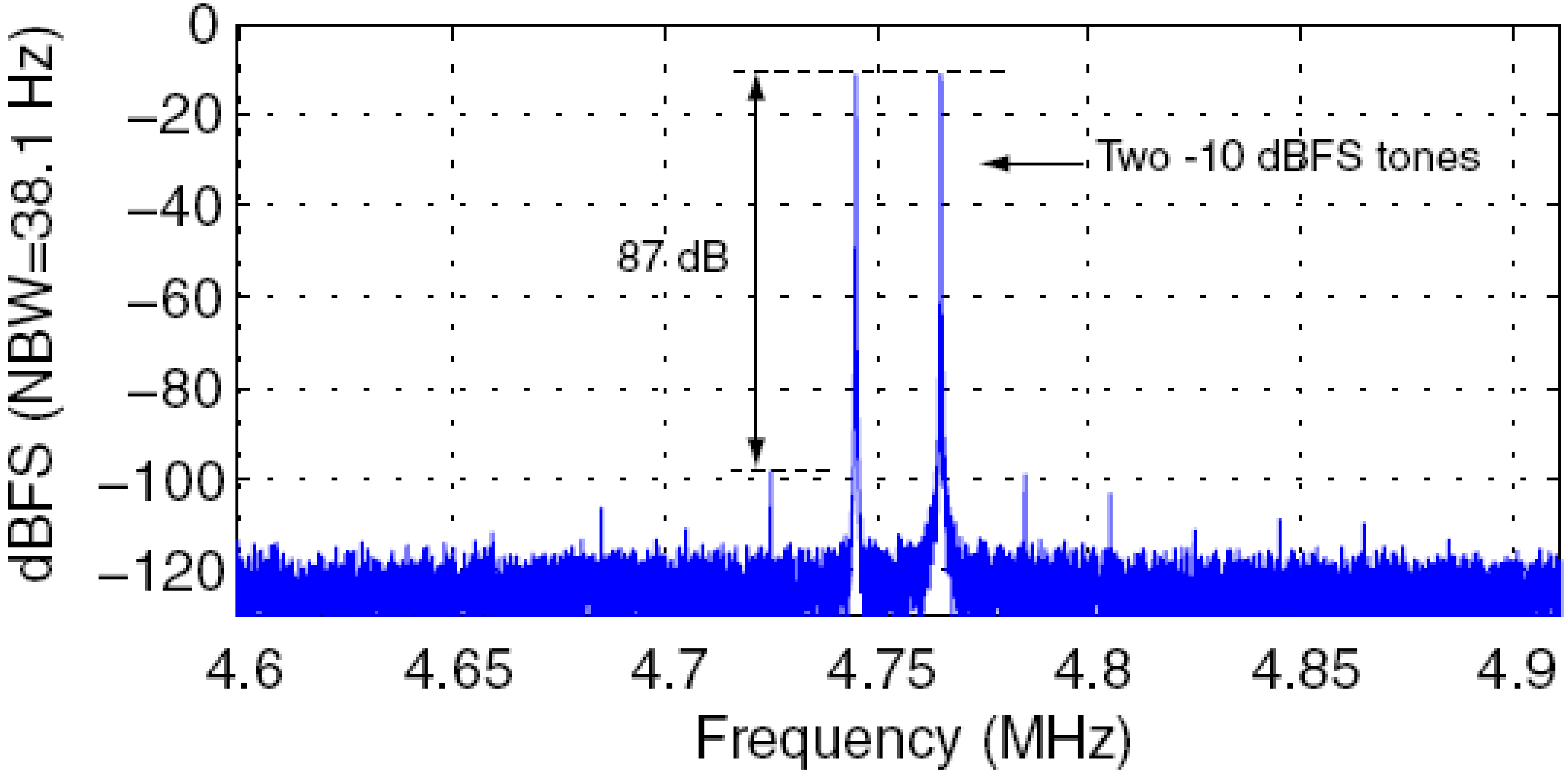
f_s = 40-MHz with bandwidth of 310 kHz (OSR = 64)

Centre frequency swept from dc to 31% of f_s in steps of 0.5% of f_s

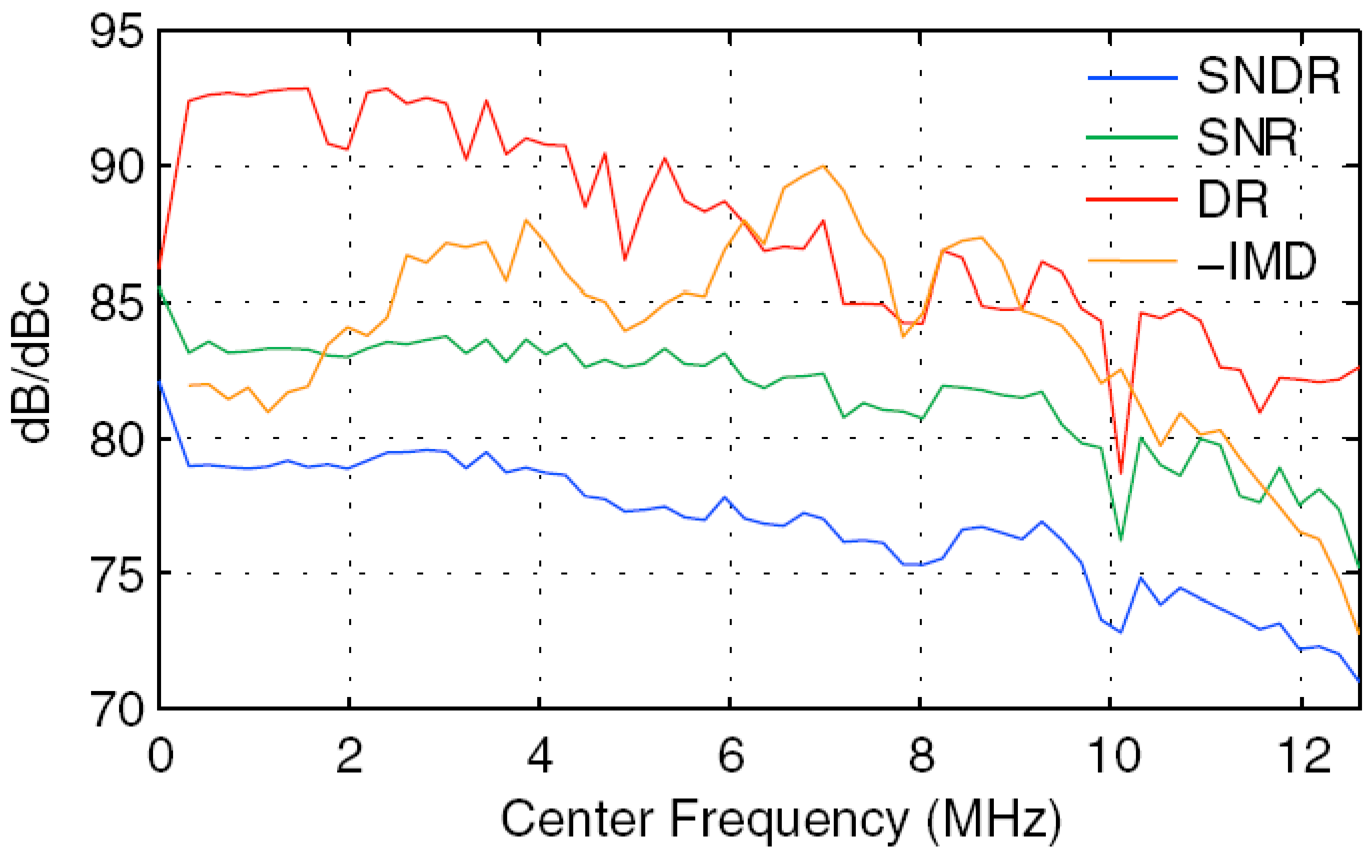
Dynamic Range Testing



Two-Tone Testing



Measurements

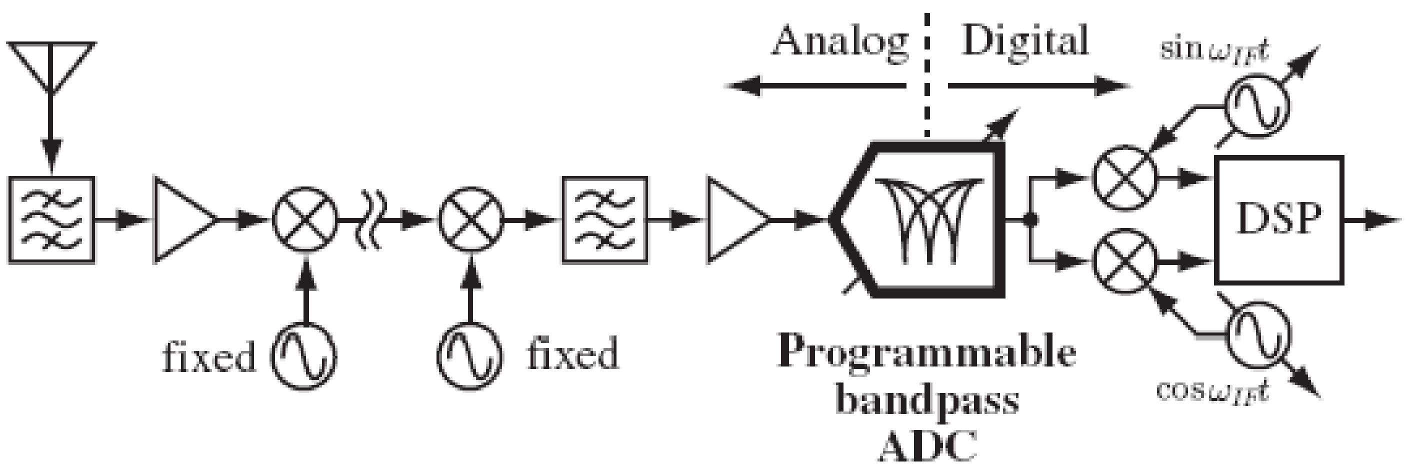


Summary and Comparison

	This work CICC '07	Colonna JSSC '04	Cusinato JSSC '01	Salo JSSC '03
f_s (MHz)	40	37.05	42.8	80
f_c (MHz)	0-12.6	10.7	10.7	20
BW (kHz)	310	200	200	270
SNDR (dB)	82-71	-	61	78
SNR (dB)	86-75	72	-	80
DR (dB)	93-76	78	74	86
-IMD (dB)	-(90-73)	-65	-75	-
P (mW)	115	88	76	24
Area (mm^2)	4.51	1	1	0.52

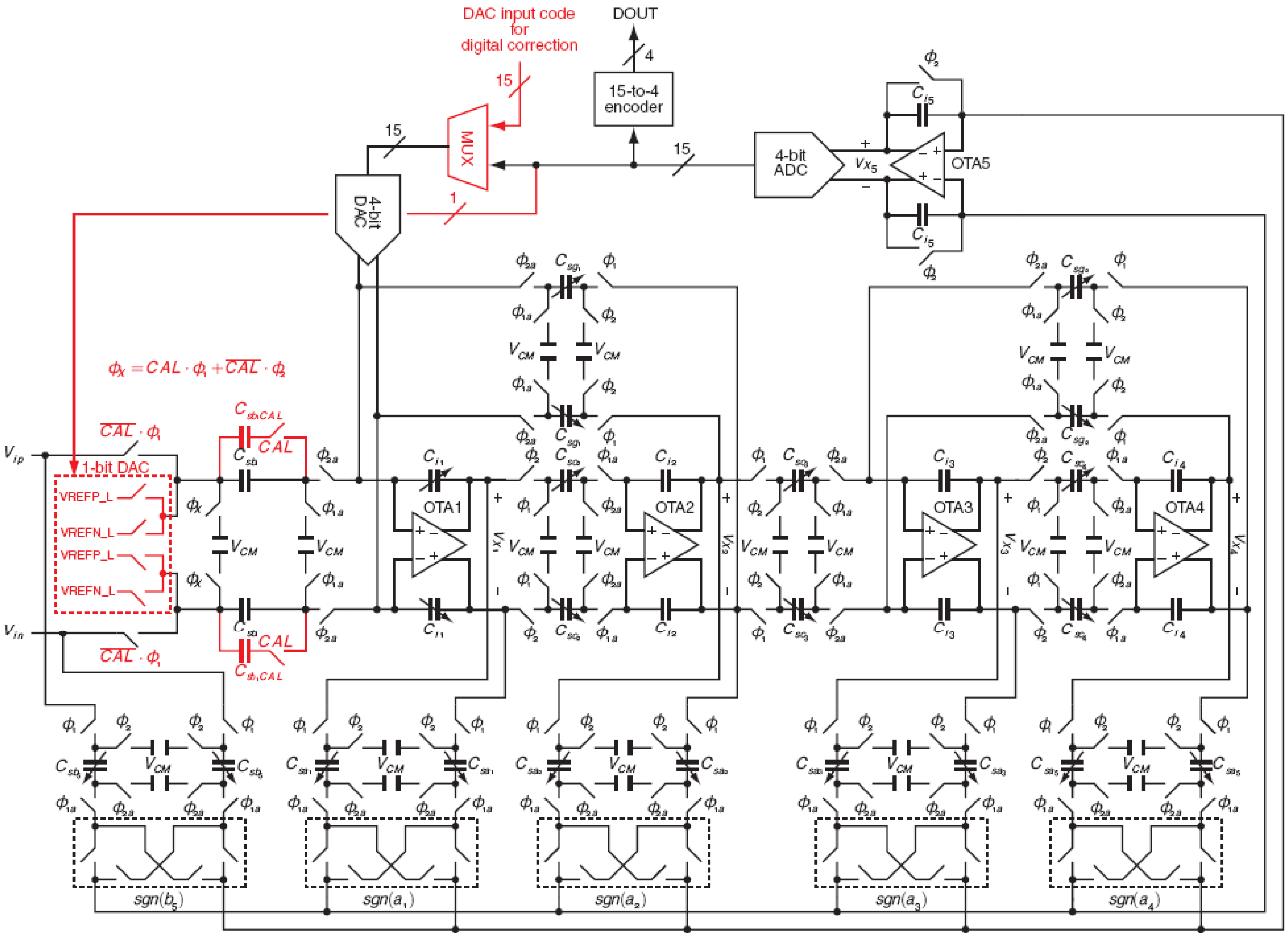
Conclusions

- Performance comparable to state-of-the-art fixed passband modulators was achieved with a programmable centre frequency
- Partly due to the fact that there have been very few multi-bit bandpass $\Delta\Sigma$ modulators reported
- Overhead required to accommodate programmability was minimized
- Future work will look at the other blocks required for flexible IF & baseband processing



Extras

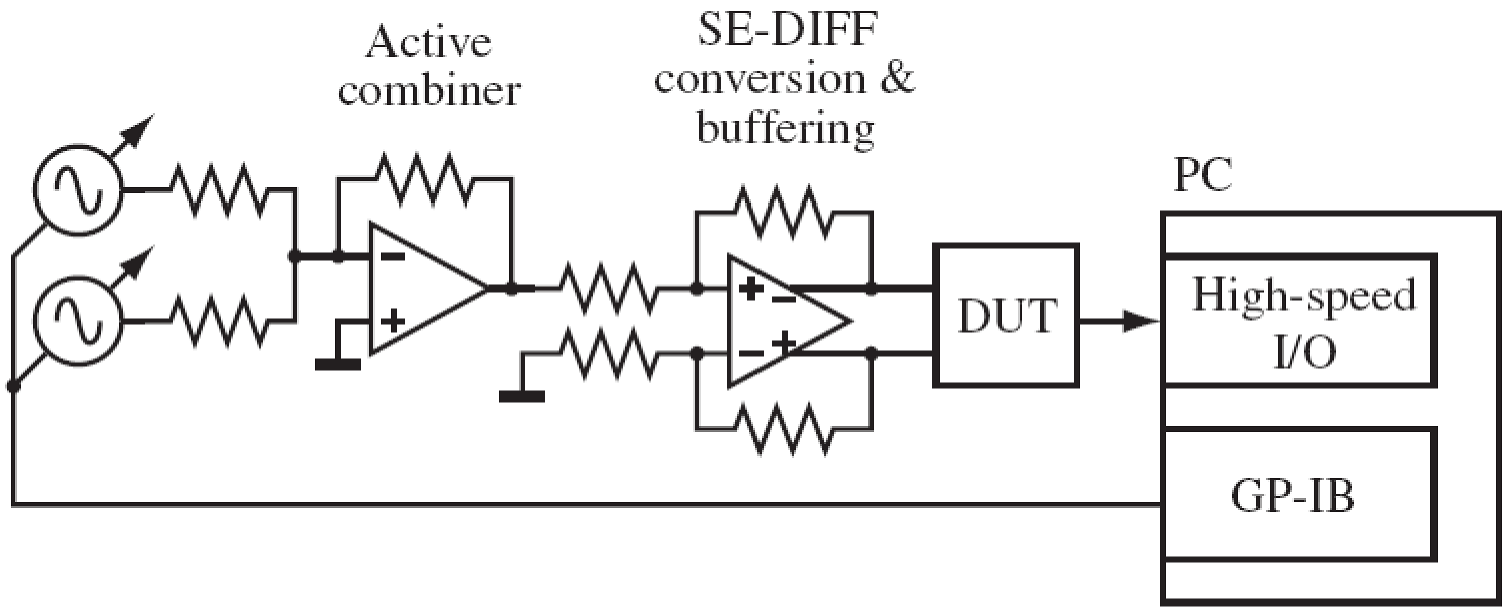
Overall Schematic



Power Breakdown

Supply	Description	Power (mW)
AVDD	OTA1	35.5
	OTA2	35.3
	OTA3	9.32
	OTA4	9.27
	OTA5	7.70
	ADC preamps	2.43
	Others	0.60
	Subtotal	100
BVDD	Bootstrapping	0.936
CVDD	Clock buffers	3.42
DVDD	Clock generator and output buffers	3.24
LVDD	ADC latches	0.234
Total		**108**

Test Setup


Active
combiner
SE-DIFF
conversion &
buffering
PC
DUT
High-speed
I/O
GP-IB