

High Speed D/A Design

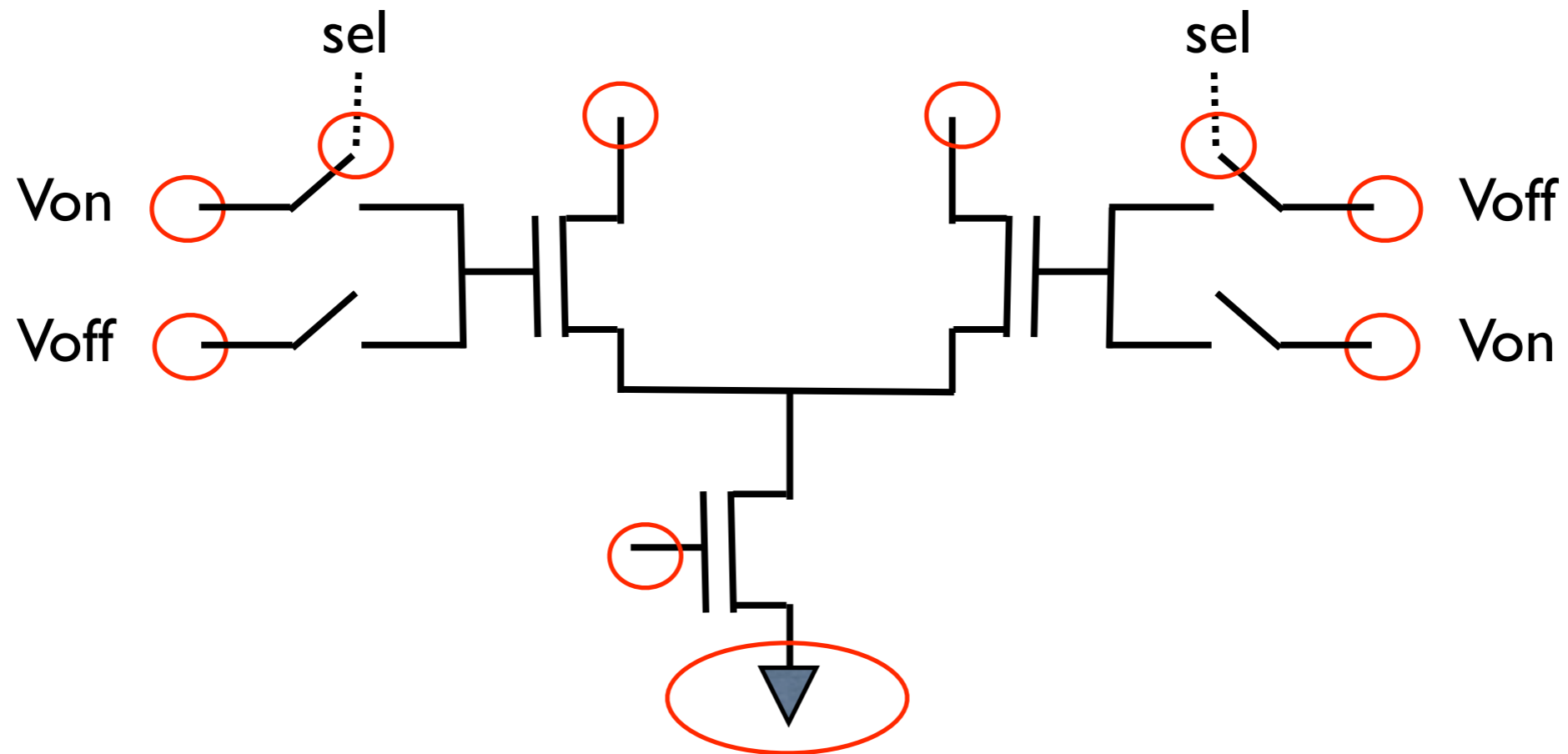
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Topics

- Current steering D/A architectures
- Challenges of high-speed design

Unit current cell



Current Steering D/A

- Current mode vs. CMOS logic
 - + Less digital current
 - More DC current
- Matrix vs. array
 - + Averaging over large area
 - More overhead/parasitics
- Unary-unary vs. unary-binary segmentation

Segmentation

- Unary LSB's

	l_1	l_2	l_3	l_4
3	1	1	1	0
4	1	1	1	1

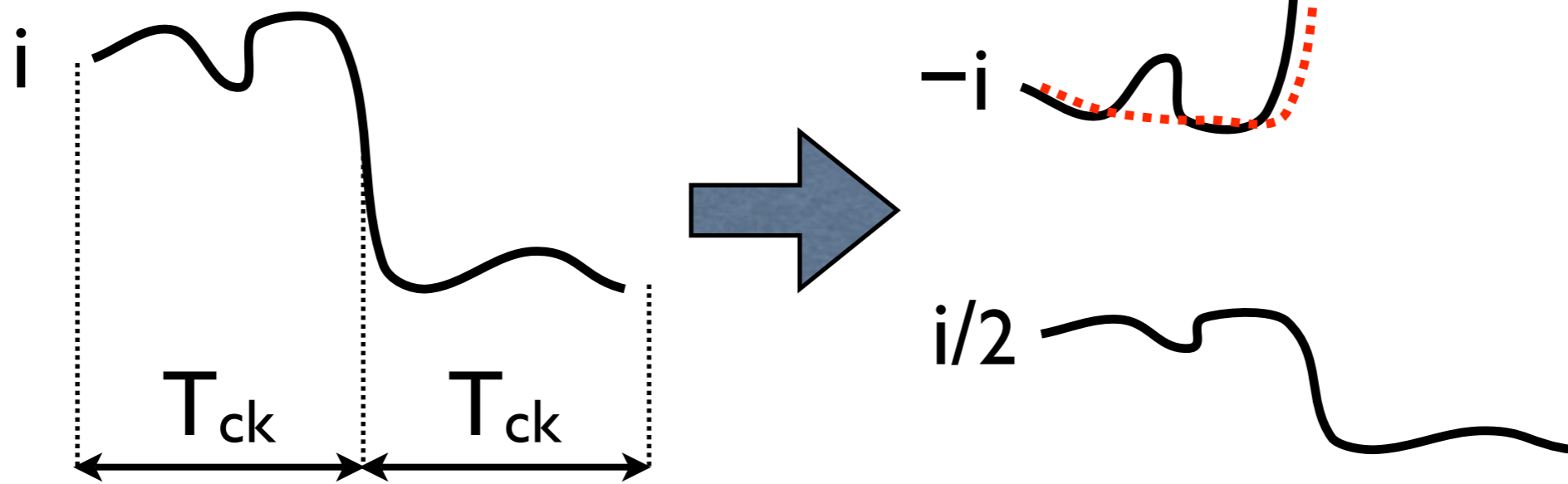
- Binary LSB's

3	1	2	0	0
4	0	0	4	0

– Scaling is not guaranteed by design but viable for low number of binary bits.

Linearity criteria

unit current waveform

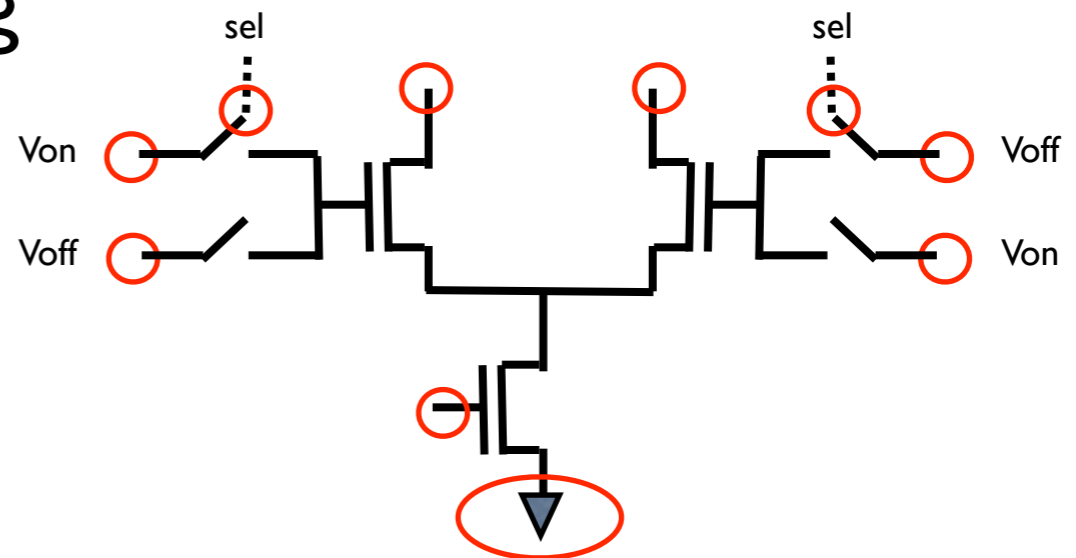


- Waveform glitch is acceptable
- But glitch mismatch is not

Variations over time

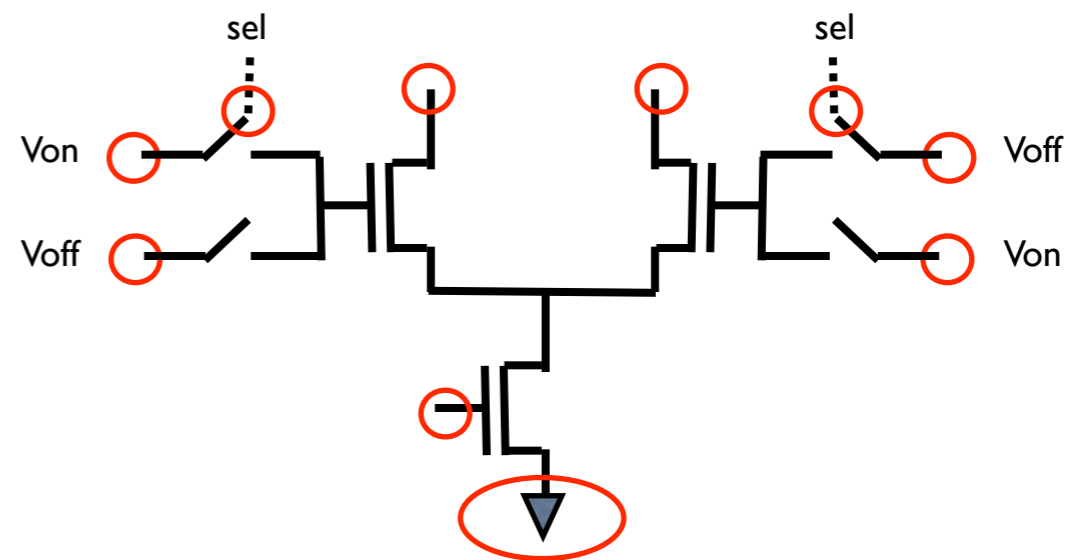
Non-cyclostationay variations due to:

- Finite r_o
- Jitter
- Asymmetric switching
- Von noise
- Supply noise
- Thermal noise

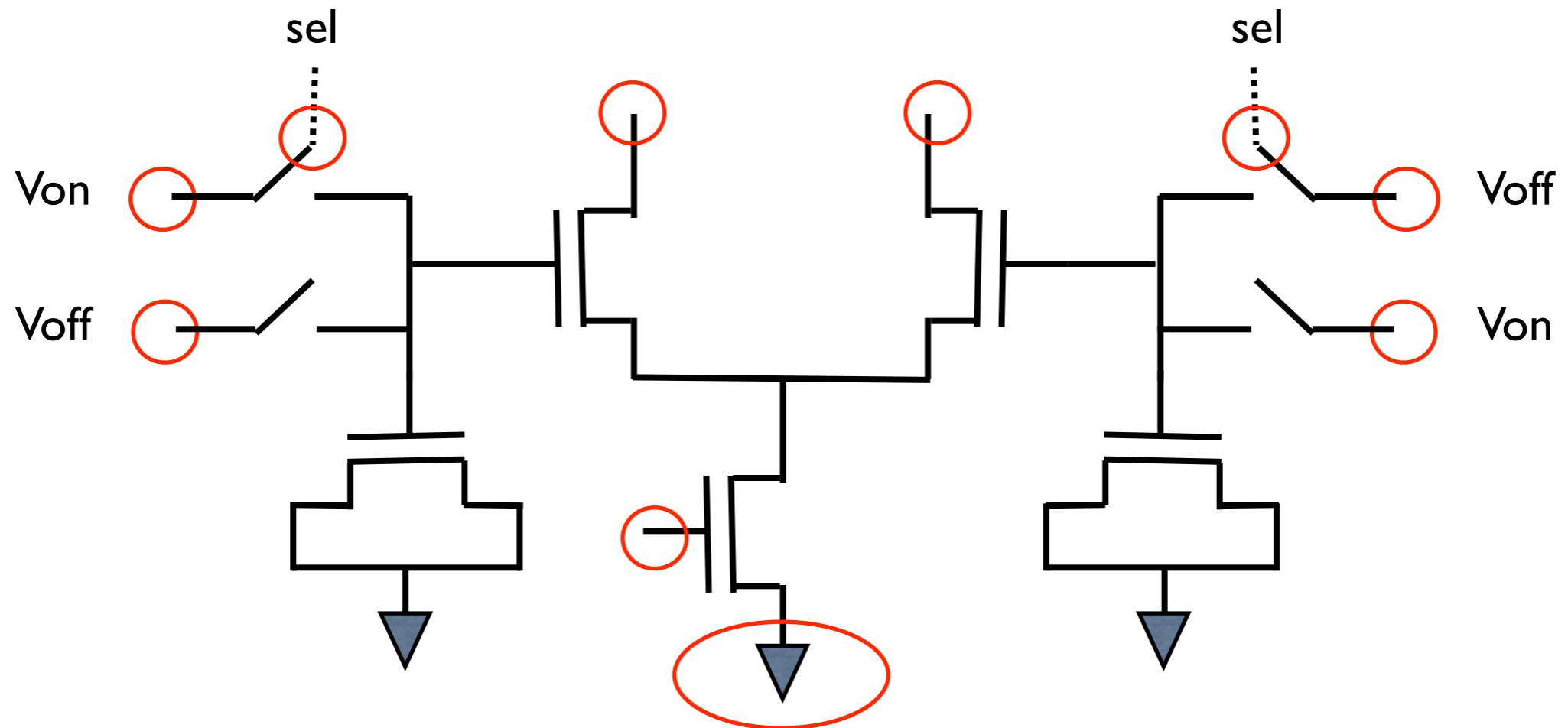


Variations over location

- Supply/gnd gradient
- Von gradient
- Clock/output skew
- Stochastic mismatch
- Temperature gradient



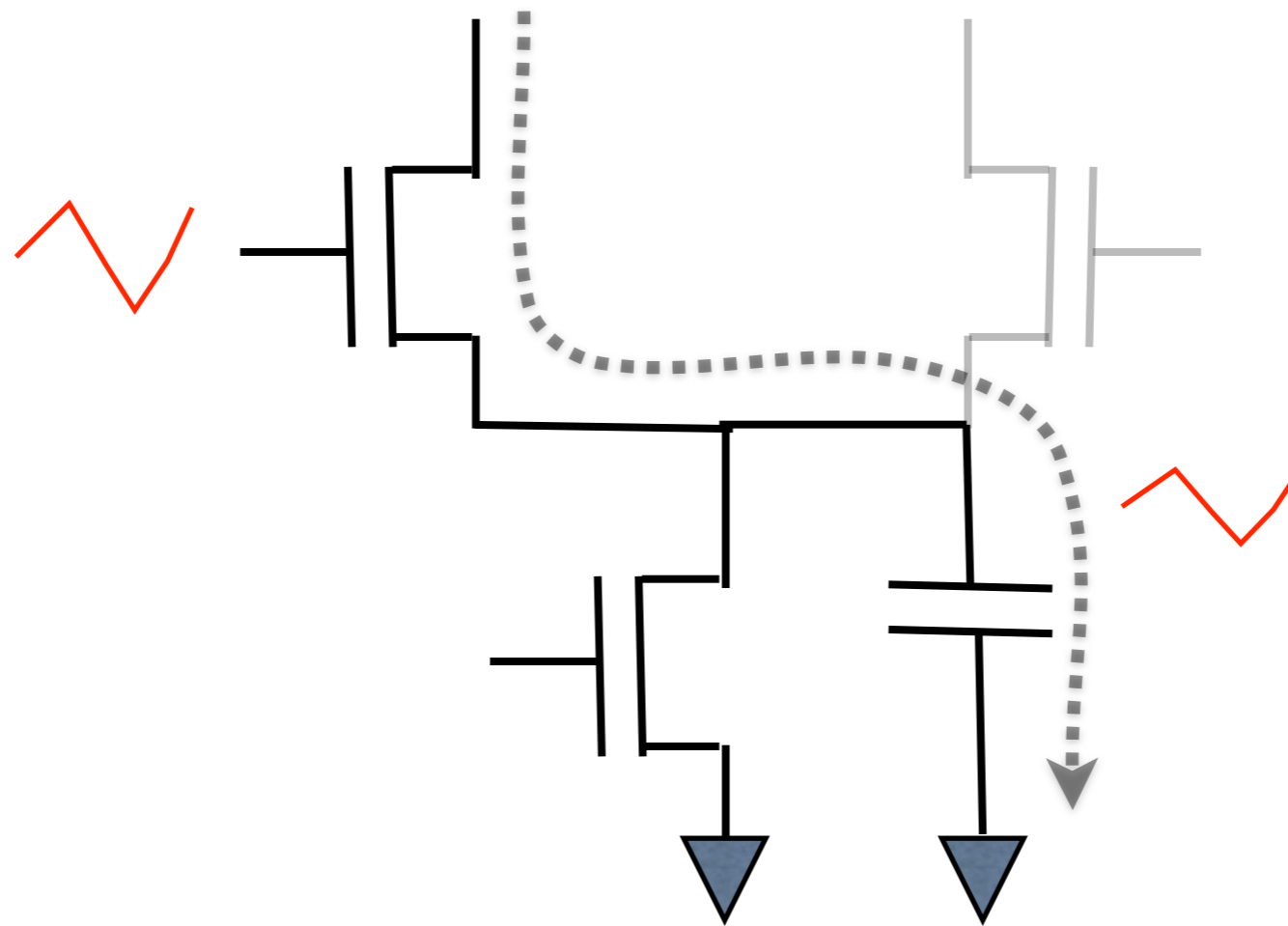
Scaling error (dynamic)



- LSB cell is ideally a perfect scaled version of MSB

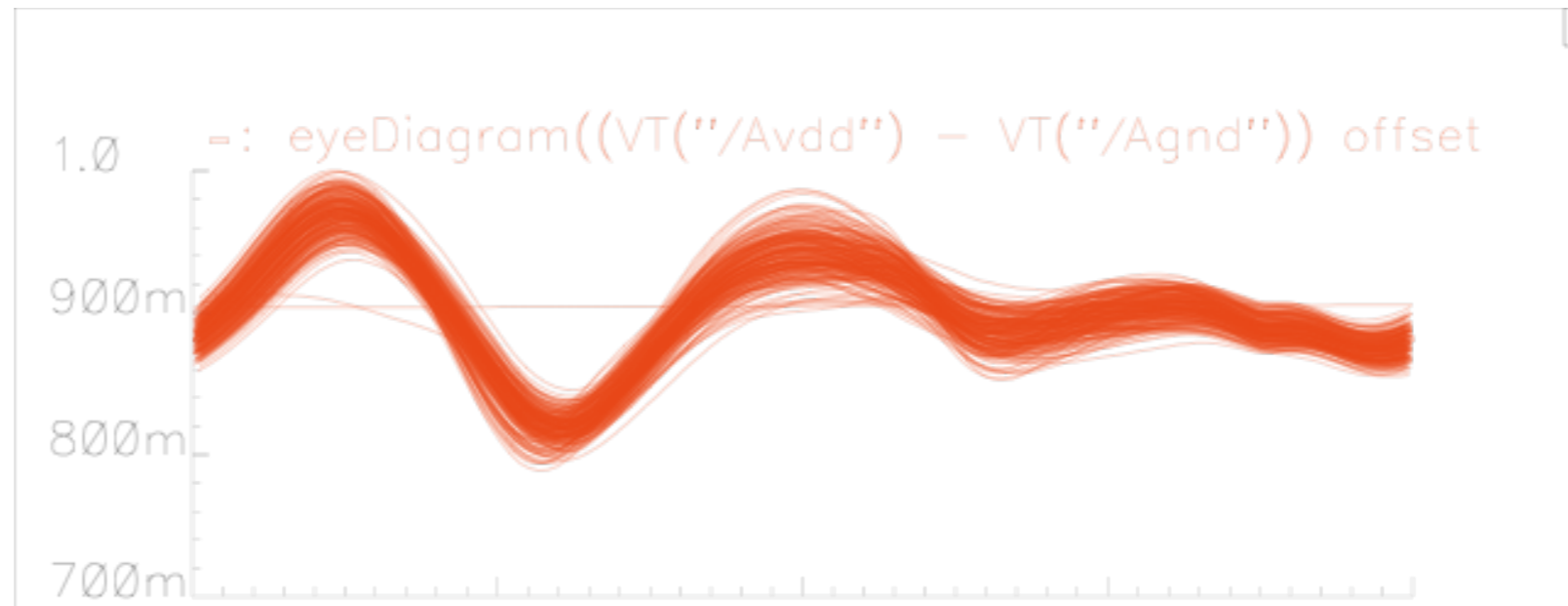
Supply noise

turns to capacitive current:

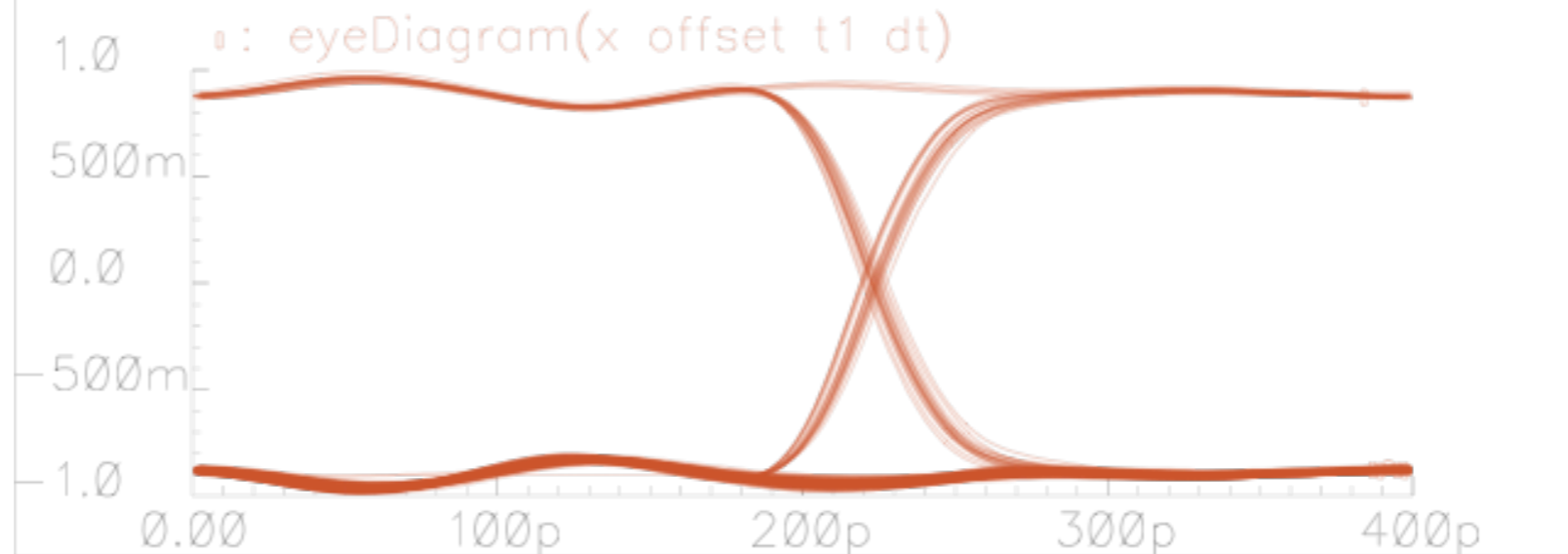


Supply induced jitter

Analog Vdd

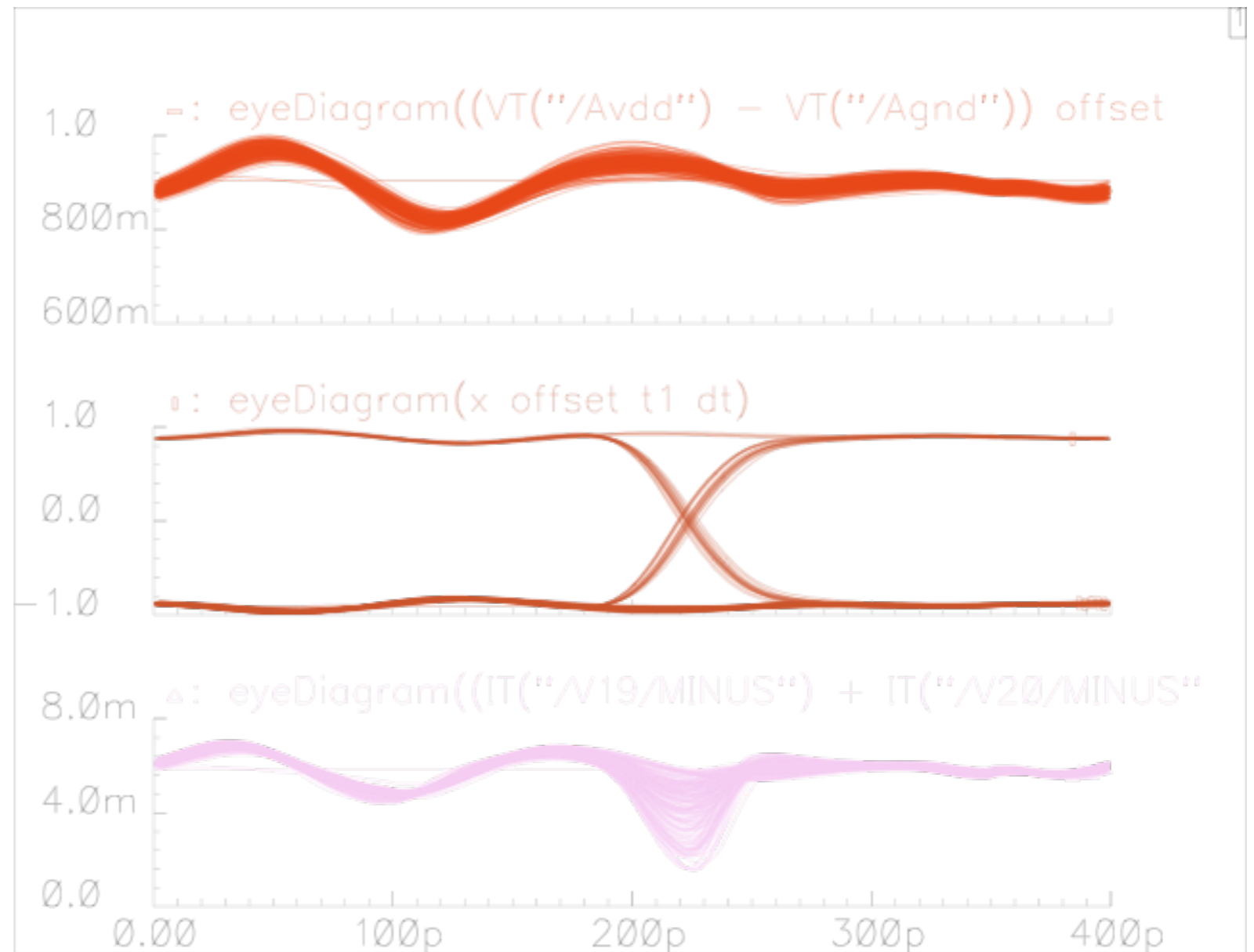


Switching voltage



Tail current modulation

Analog Vdd



Switching voltage

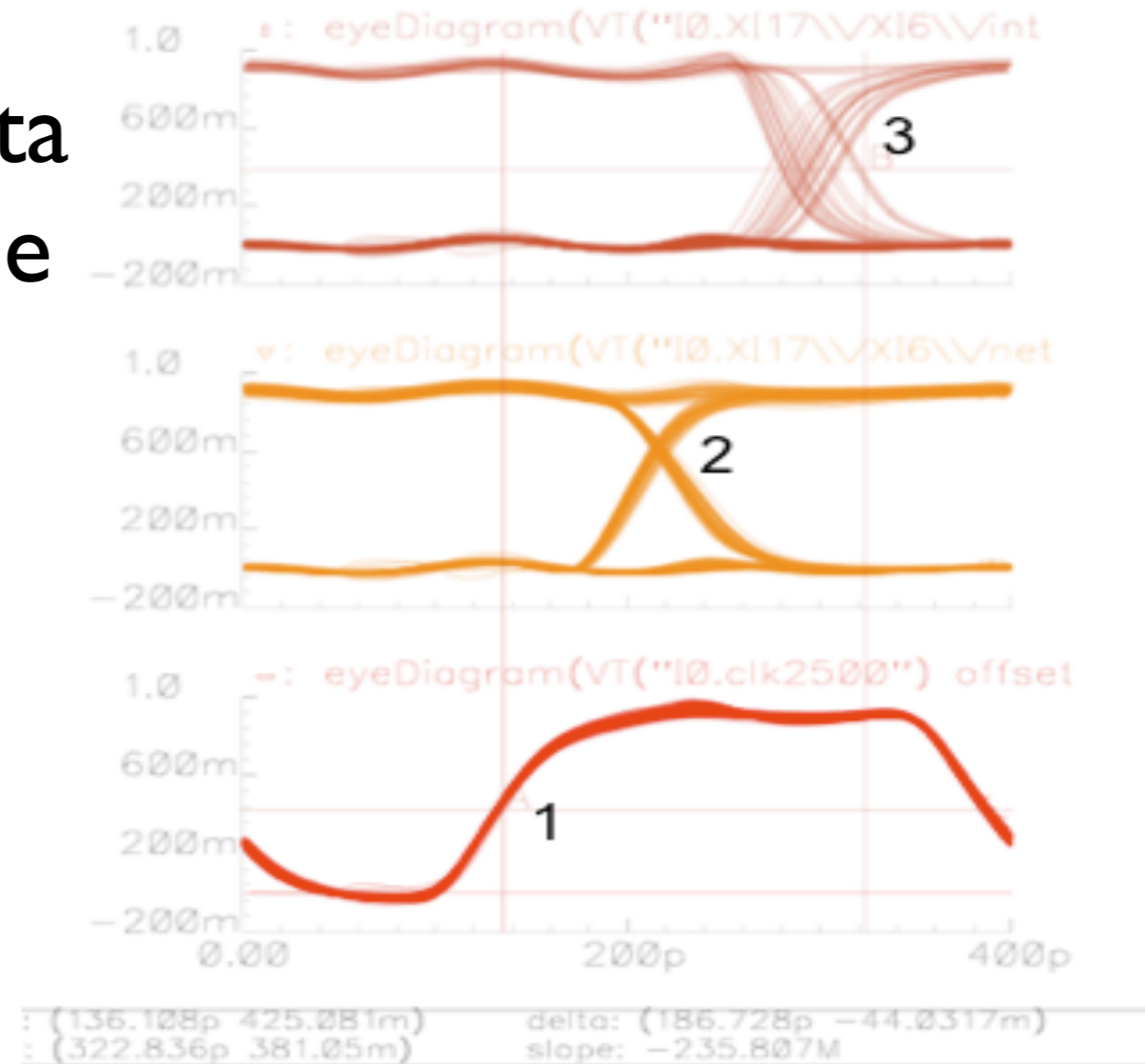
Common-mode
current

Supply noise mitigation

- Low impedance supplies
- Separate analog/digital supplies
- Dummy cells
- Buffered Von

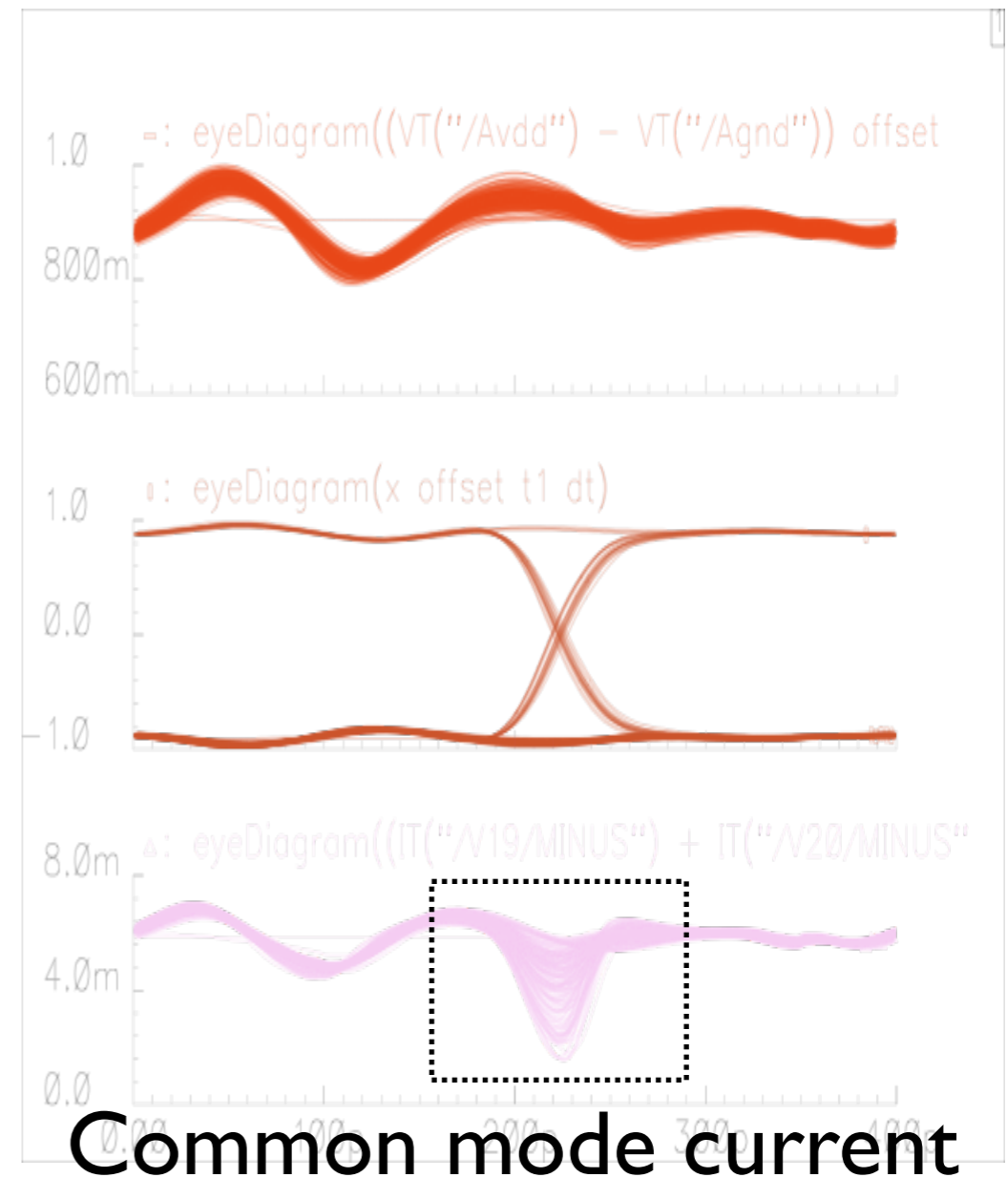
Data propagation time

- Variations of data propagation time is potentially another source of error
- Add another latch?



Common mode current

- CM variation is not necessarily a linearity issue, however ...
- CM to DIFF conversion results in differential error
- Need less parasitics, low energy glitches



SNDR vs. Time

- Dynamic errors can be avoided at the “right” sampling time
- Output filter helps otherwise

