# Design Challenges for CMOS RF-to-DIGITAL Interfaces for Multi-Service Wireless Communication Systems

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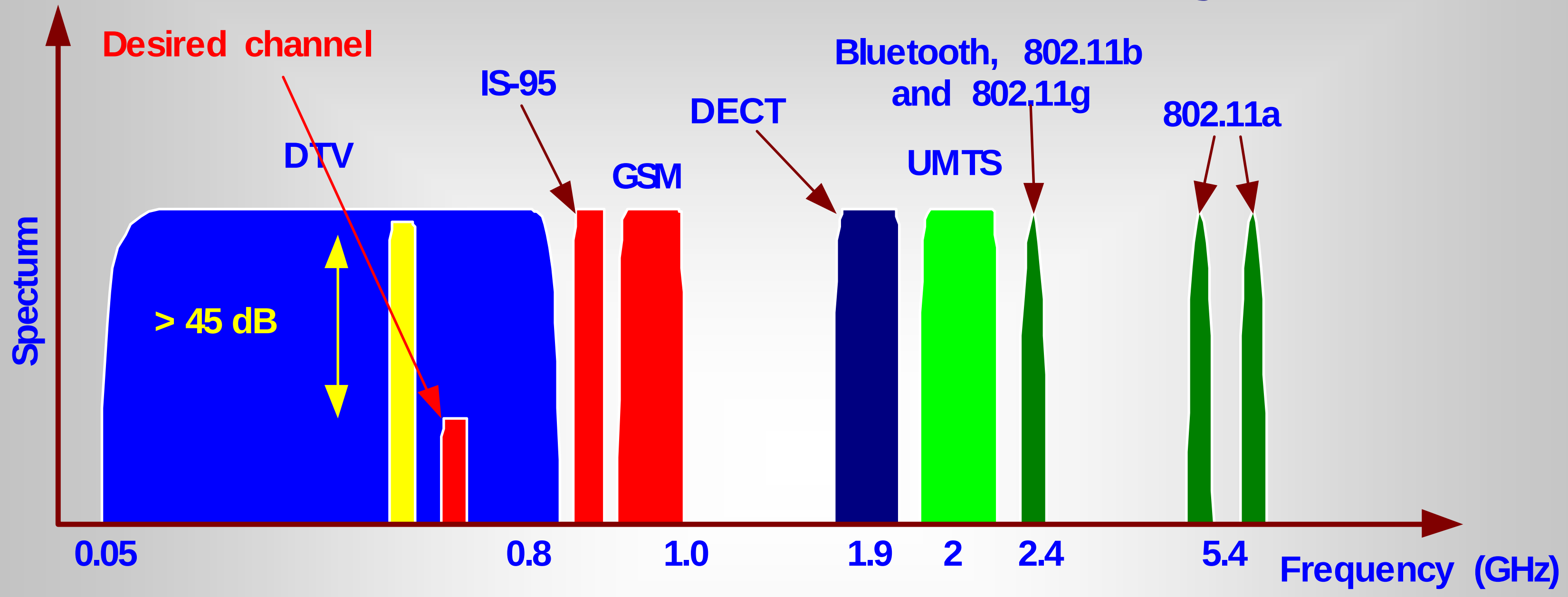
# Introduction

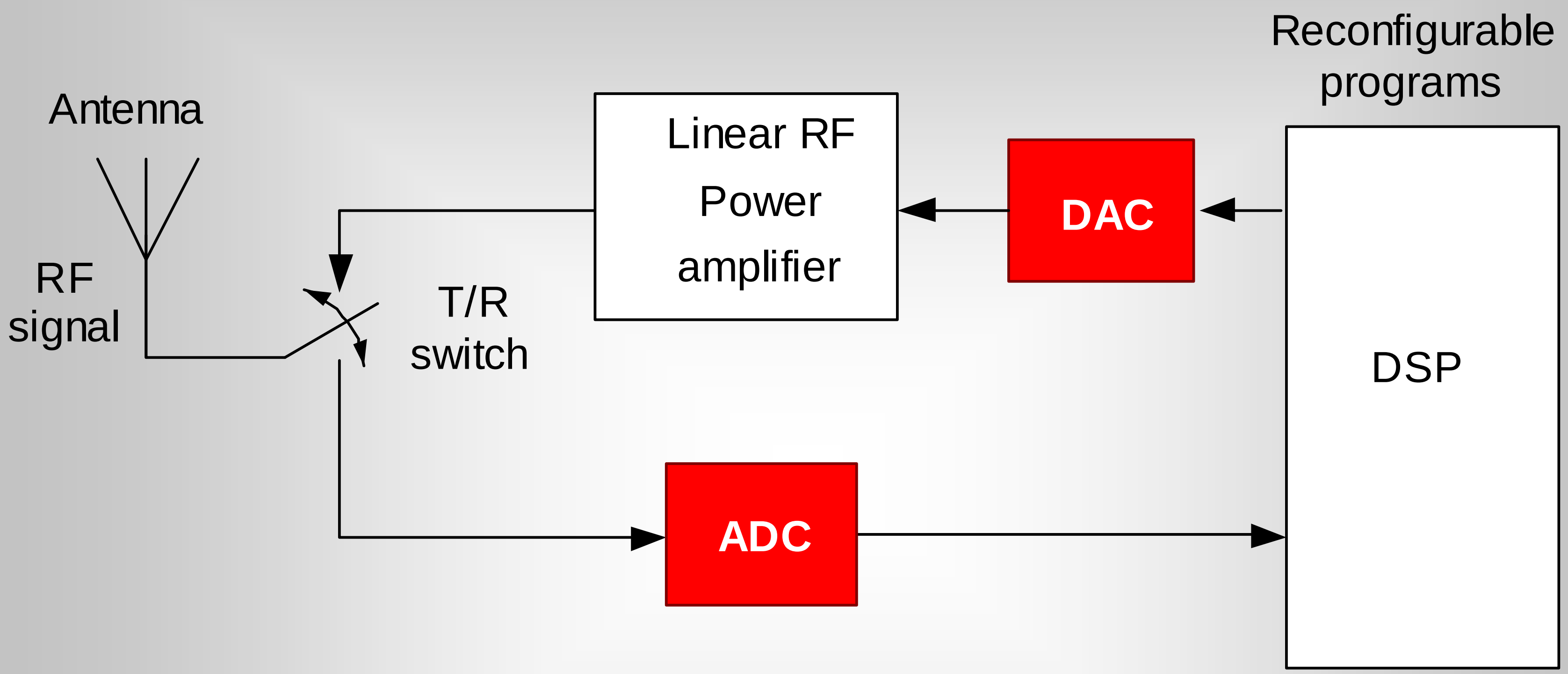
- Number of wireless standards has increased at a tremendous pace in the past decade
  - Cellphones (GSM, EDGE, CDMA, W-CDMA,UMTS etc), communication networks (802.11 a/b/g, bluetooth, WiMax, UWB etc), satellite services (GPS)
- Next generation receivers require support for multiple standards on same chip
- RF and analog front ends use different technologies – CMOS, BiCMOS, III-IV Compounds (GaAs, InP, etc.) **BUT**
- Strong push for CMOS only system-on-chip solution – 90% digital baseband + 10 % RF/analog
- Most receivers use a variation of the superheterodyne architecture

# What’s the problem?
# Noise Bandwidth and Linearity issues



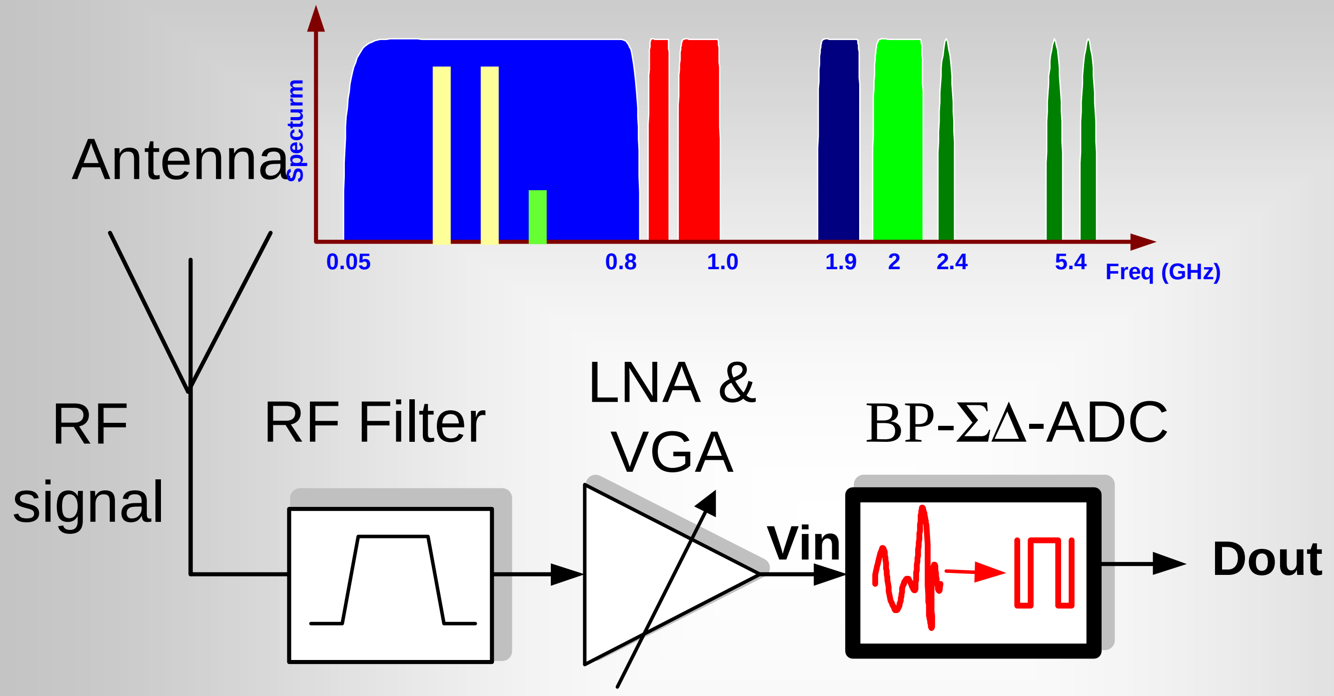
- ➢ Geographic location (**Blockers**)
- ➢ Bandwidth and number of channels
- ➢ Specifications for minimum signal power and SNR

# Ideal software radio transceiver: Why not?



- Software radio concept introduced in 1991 by Joe Mitola
- RF front end + reconfigurable software platform/algorithms in DSP
- Receiver implementation as shown requires >130 dB DR ADC operating at RF: **Not possible in any available technology**

# Software radio receiver: Design Challenges



Is it possible to have a multi-standard solution based on this architecture?

**Bandwidth and linearity required?**

**Dynamic range required?**

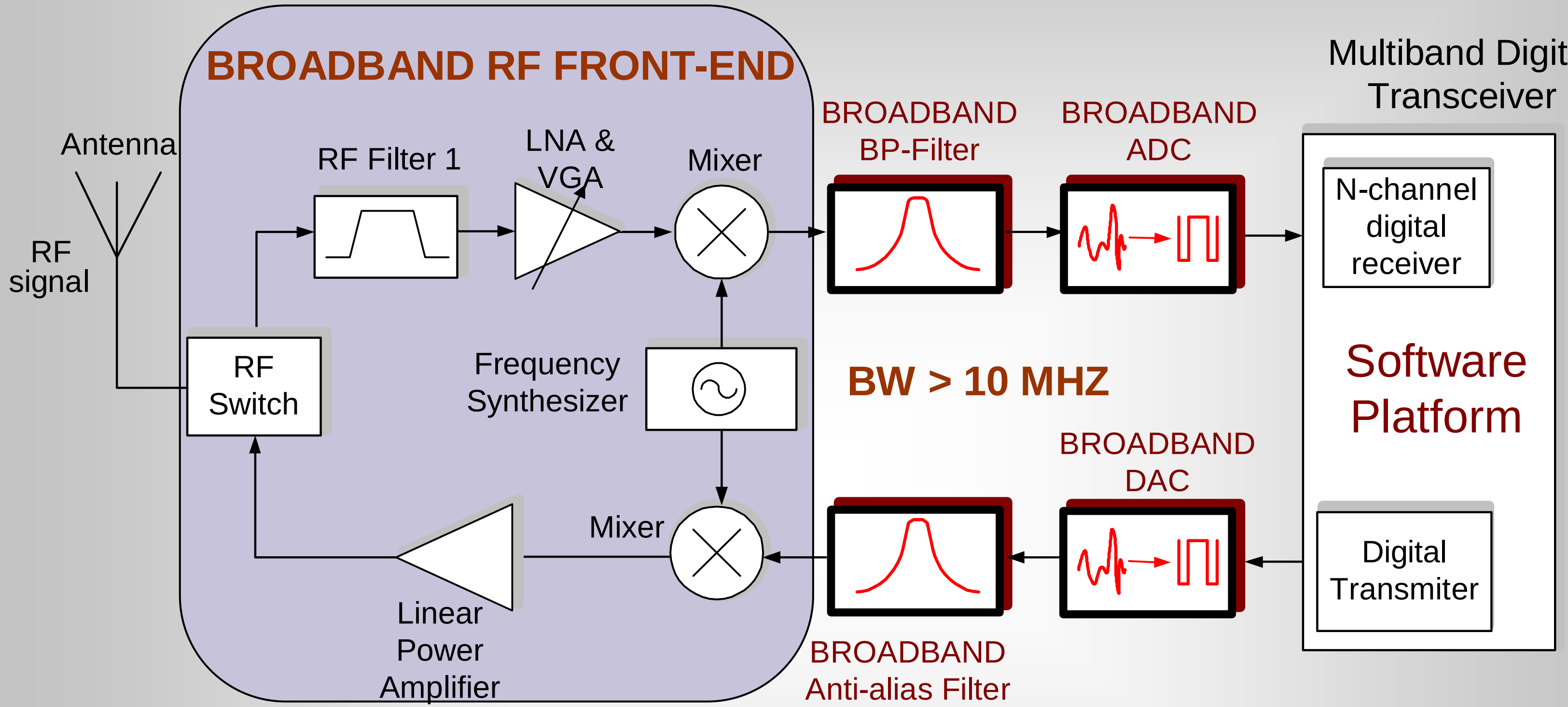
**DTV ➔ SNR signal=25 dB; Blockers > 45 dB; Crest factor > 20 dB**

**LNA+VGA+ADC resolution over 90 dB ; IIP2 and IIP3 over 30 dBm!**

**Power required?**

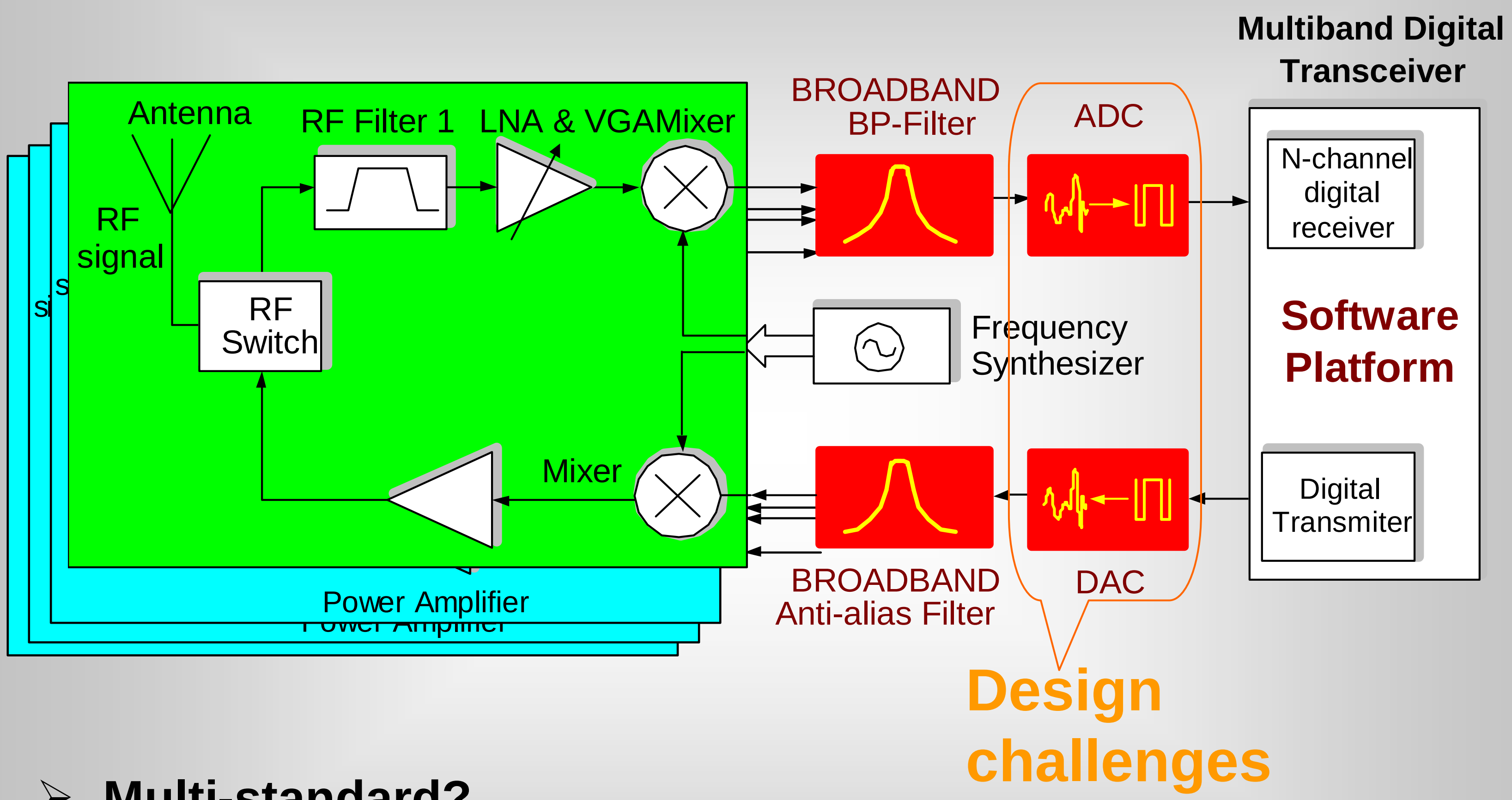
**Can you use tracking filters? (back to the past)**

# Narrow-Band Bandpass Radio Transceiver



- **Minimize analog hardware: BW > 10 MHz to accommodate Video Applications**
- **Flicker noise is not an issue**
- **Best IF frequency? Around 1 GHz (LC networks) or ~ 200 MHz (Active solution)**

# Software Defined Radio Receiver



- **Multi-standard?**
- **MIMO Solution: Multiple Input Multiple Output Antennas**
- **Off-chip SAW filters are used**

# Literature Survey

| Ref | Type | $f_0$ (GHz) | Clock (GHz) | SNR @ BW=1 MHz | Power (mW) | Technology |
|---|---|---|---|---|---|---|
| [1] | 4th order CT BP Σ Δ | 1.3 | 4.3 | 62 dB | 6200 | InP HBT |
| [2] | 4th order CT BP Σ Δ | 1 | 4 | 59 dB | 350 | 0.5 µm SiGe |
| [3] | 4th order CT BP Σ Δ | 1 | 4 | 50 dB | 450 | 0.5 µm SiGe |
| [4] | 2nd order LP-Σ Δ & mixer | 0.9 | 0.1 | 25 dB | 30 | **0.25 µm CMOS** |
| [5] | 4th order CT BP Σ Δ | 0.8 | 3.2 | 55 dB | 1800 | GaAs |
| [6] | 4th order CT BP Σ Δ | 0.2 | 4 | 78 dB | 3500 | InP HBT |
| [7] | 4th order CT BP Σ Δ | 0.2 | 0.8 | 61 dB | 64 | SiGe Bipolar |
| [8] | 4th order CT BP Σ Δ | 0.18 | 4 | 76 dB | 3200 | GaInAs HBT |
| [9] | 4th order CT/DT BP Σ Δ with mixer | 0.1 | 0.4 | 47 dB | 330 | **0.35 µm CMOS** |
| [10] | 10th order CT BP Σ Δ | 0.09 | 2.5 | 87 dB | 6000 | InP HBT |
| [11] | 4th order CT BP Σ Δ | 0.9 | 3.8 | **59 dB** | **75** | 0.25 µm SiGe |
| [12] | 4th order CT BP Σ Δ | 2 | 40 | **72 dB** | **1600** | 0.13 µm SiGe |

# Literature Survey

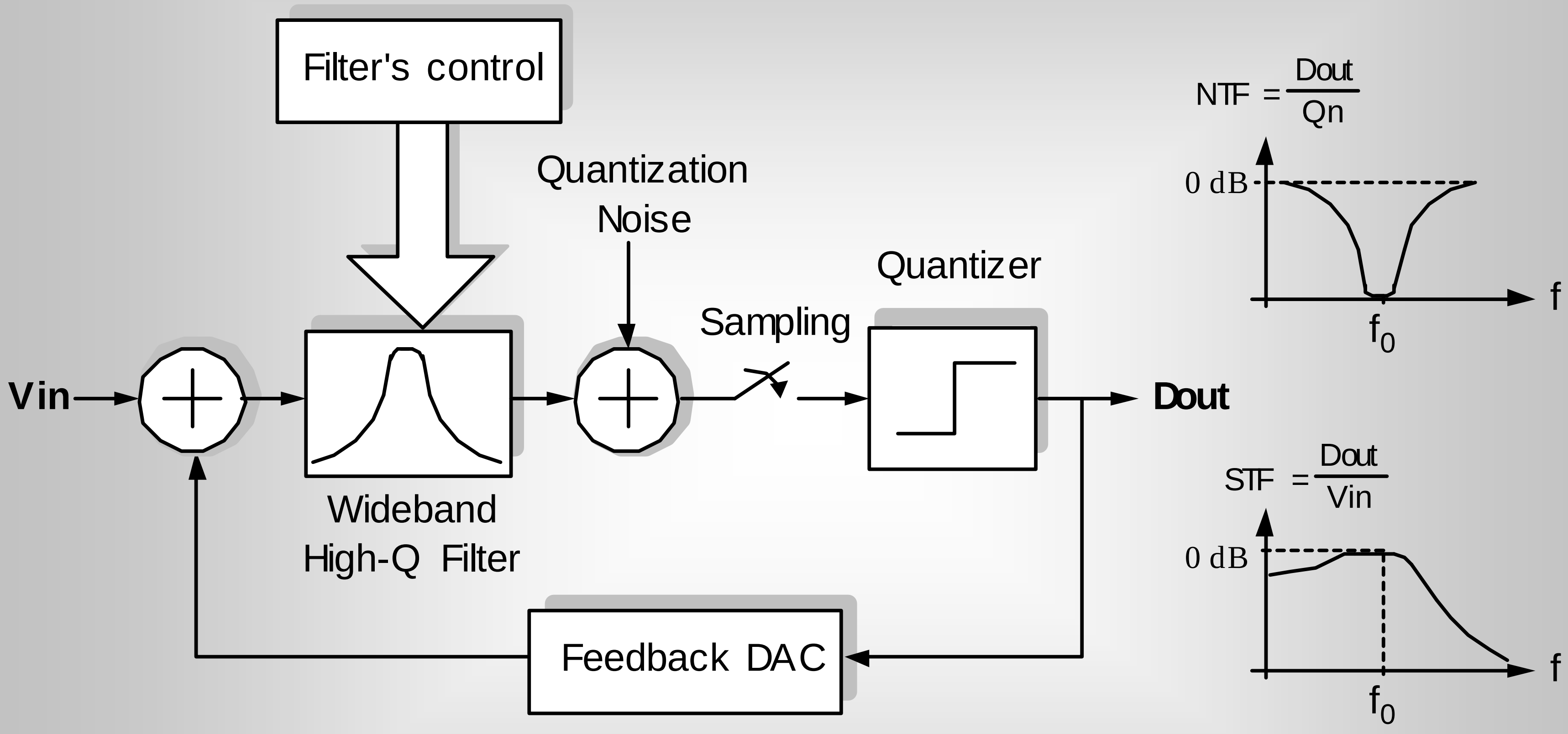
- High resolution CMOS pipeline ADC’s are suitable only for “low” IF A/D conversion, not for RF conversion

- **Best choice of architecture for high resolution RF CMOS A/D conversion is continuous time BP ΣΔ ADC, but has significant design challenges**

- Reported implementation are predominantly in SiGe BiCMOS and non-silicon technologies like GaAs, InP etc

- Most direct sampling frequencies have power in the watt range – big disadvantage for handsets

# CT BP ΣΔ ADC for Broadband applications



- ✓ High frequency of operation
- ✓ Relaxed specifications for anti-alias filter
- ✓ Modest power consumption
- ✓ Good linearity, but must be improved (open issue)

# Design parameters for BP ΣΔ ADC

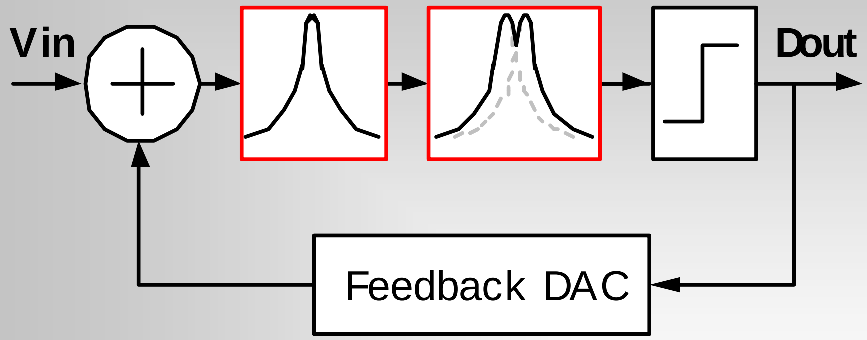
$$SNR\,(dB) = 10 * \log_{10}\left[\frac{3}{2}\frac{(N+1) * OSR^{N+1}}{\pi^{N}}\right] + 6.02 * (B-1)$$

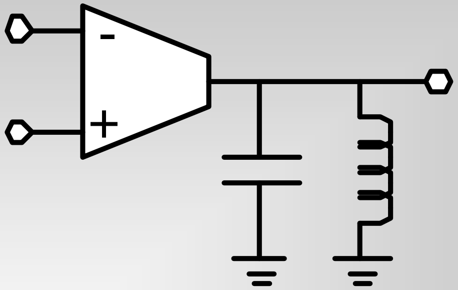
$$N \rightarrow order\ of\ \ filter, OSR \rightarrow oversampling\ ratio$$

$$B \rightarrow number\ of\ \ bits\ in\ comparator$$

- SNR ↑ with higher N
  - Loop stability becomes a problem (for practical implementation N=<6)
- SNR ↑ with higher OSR
  - Highest Fs is determined by comparator and DACs
- SNR ↑ with multi-bit quantizer and DACs.
  - Design complexity of Multi-bit comparator and multi-bit DAC.
  - B in the range 1-3; hard to handle at RF

# Distortion

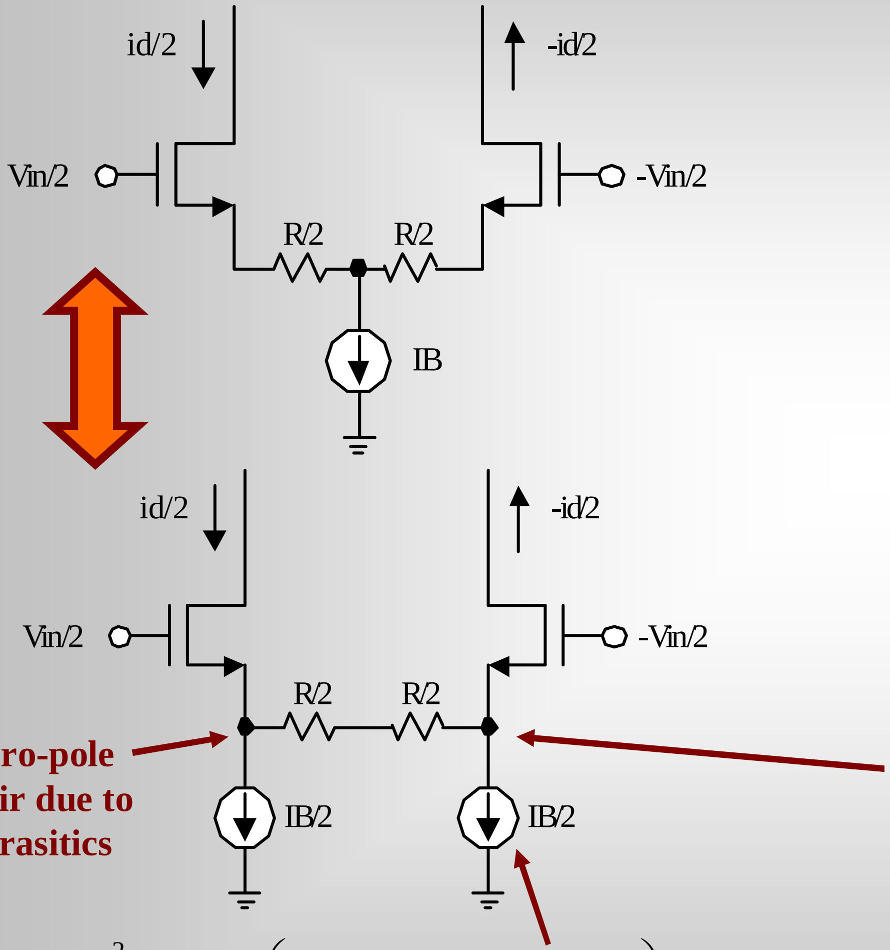




- Linearity of the first filter stage is the most critical one in the ADC
- Many linearization schemes (cross-coupling, negative feedback etc) which work well at IF do not necessarily scale at RF
- Mobility degradation is a big issue
- Non-linearity due to parasitic capacitances becomes a significant factor as device sizes become larger
- Transistor output resistance is quite non-linear as well
- Source degeneration offers good dynamic range (distortion + input noise) for RF signals among existing linearization schemes

# Differential Pair: Improved linearity

**Noise? Frequency response? HD3?**



**Zero-pole pair due to parasitics**

$$\frac{v_{no}^2}{Hz}=\frac{4kT}{G_{m1}}\left(\gamma+N_r+2N_r^2\gamma\frac{g_{m2}}{G_{m1}}\right)$$

$$i_d \cong g_m v_{in}\sqrt{1-\left(\frac{v_{in}}{2n\left(V_{GS}-V_T\right)}\right)^2}$$

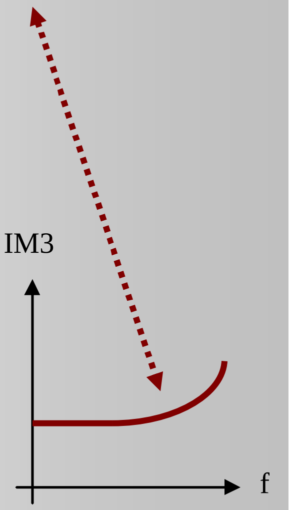
$$n=1+g_m R/2$$

**Decreases at HF due to the parasitic capacitors**

$$g_m \cong \sqrt{\beta_1 I_B}$$

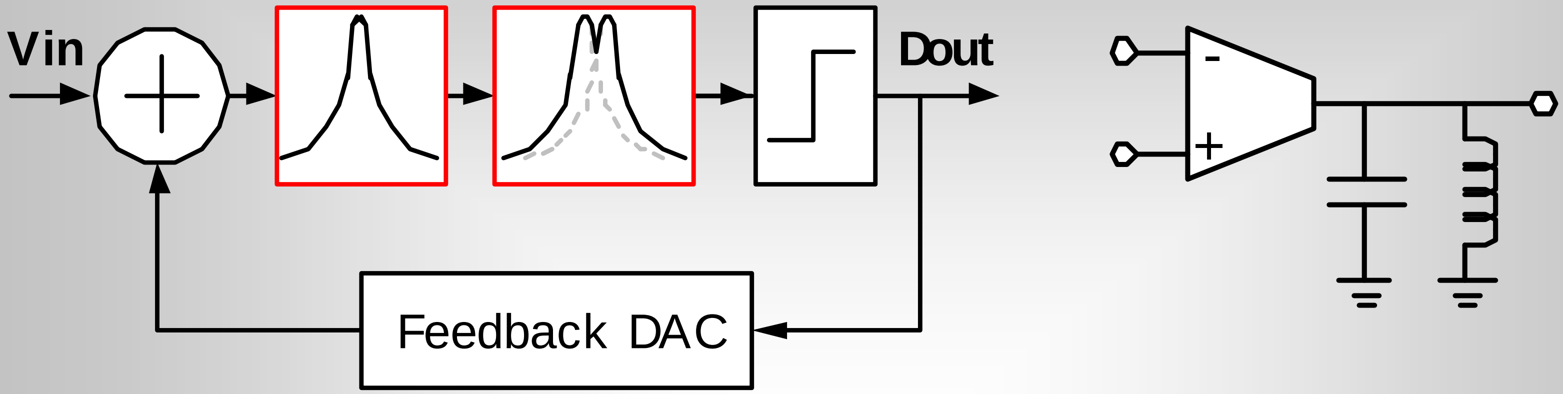
$$HD2=0 \quad \text{(Ideally)}$$

$$HD3 \cong \frac{1}{32n^2}\left(\frac{v_{in}}{\left(V_{GS}-V_T\right)}\right)^2$$



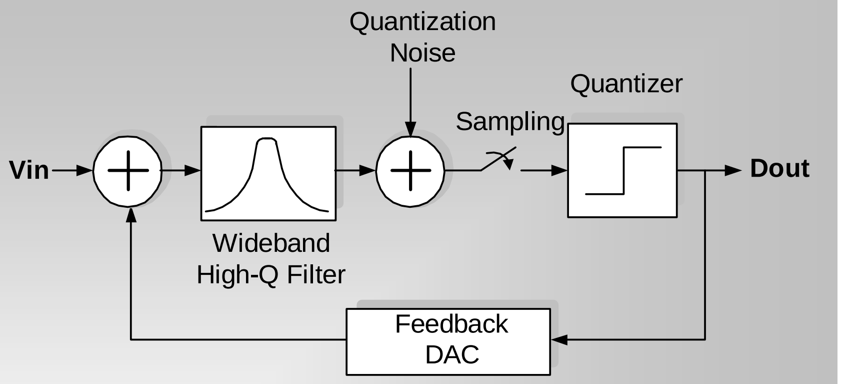
**Non-linear transistor output resistance and junction capacitors are the ultimate linearity limitation**

# Noise



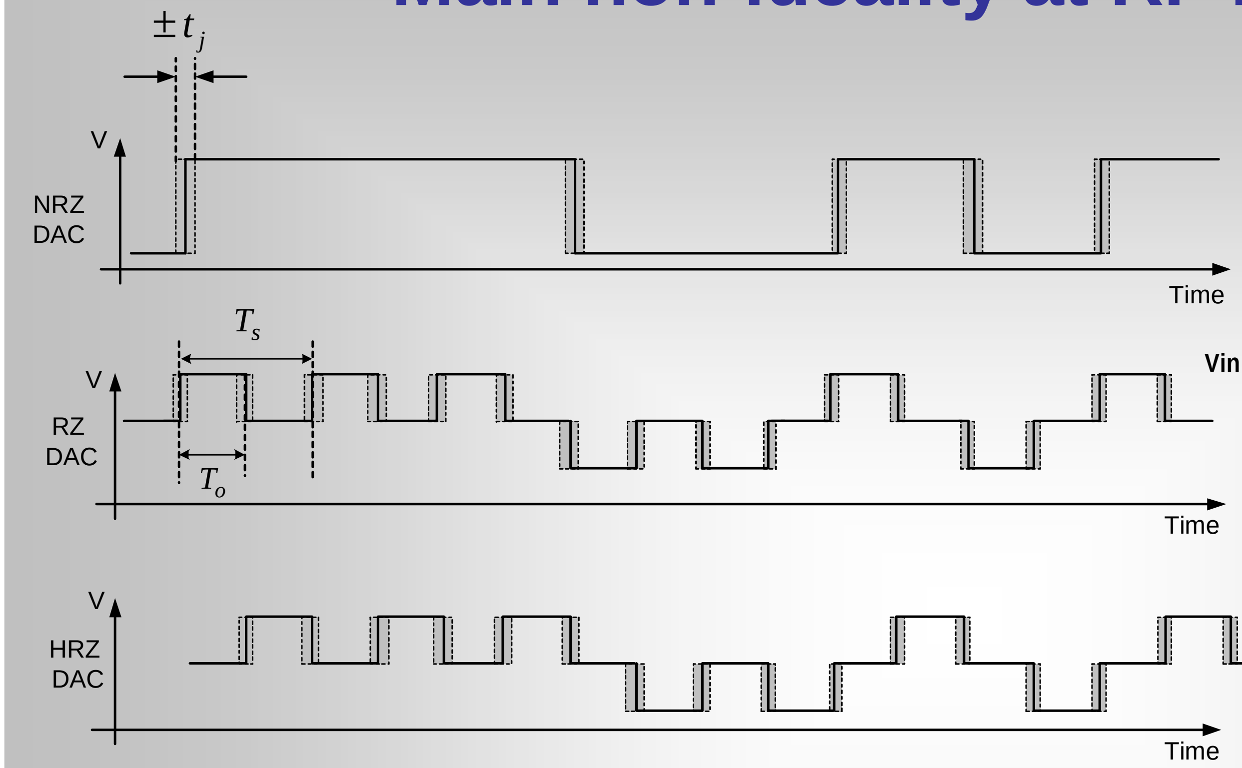
- Thermal noise of drain current is the dominant source for input referred noise of active devices
- Flicker noise does not significantly affect the ADC performance
- Usually gate noise (due to AC gate current) becomes significant only at high frequencies (> 3 GHz)
- Input referred thermal noise of filter + DAC should be well below the theoretical predicted quantization noise floor

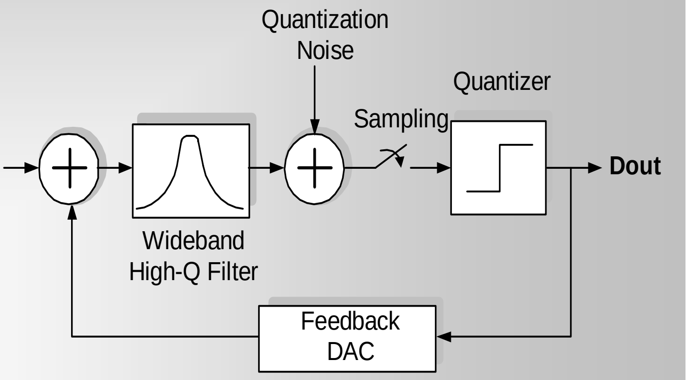
# DAC implementation



- A simple MOS differential pair is a single-bit DAC
- Linearity of DAC also determines overall IM3 of ADC
- Single-bit DAC is inherently linear
- Multi-bit DAC implementations suffer from linearity issues
- DEM techniques to improve DAC linearity work well at IF but they are not very efficient at RF (open problem)
- DEM techniques increases excess loop delay and results in lower SNR (pulse response is affected)

# Main non-ideality at RF is clock jitter



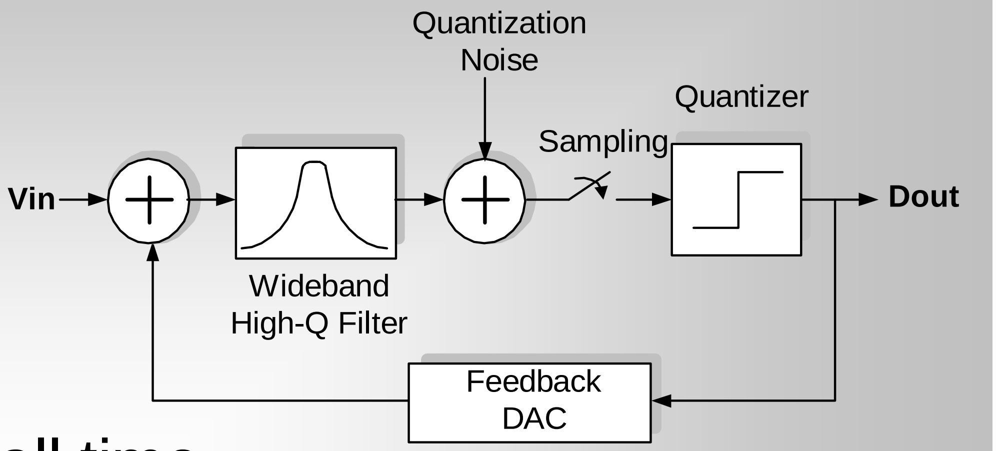


▯ → Error due to clock jitter every clock edge $\quad \sigma_j$ → RMS value of clock jitter

$$SNR_{NRZ} = 10\log_{10}\left(\frac{OSR * V_{in}^2 * \text{sinc}^2\left(\frac{\omega_o T_s}{2}\right)}{4\left(\frac{\sigma_j}{T_s}\right)^2}\right) \qquad SNR_{RZ/HRZ} = 10\log_{10}\left(\frac{OSR * V_{in}^2 * \text{sinc}^2\left(\frac{\omega_o T_o}{2}\right)}{4\left(\frac{T_s}{T_o}\right)^2\left(\frac{\sigma_j}{T_s}\right)^2}\right)$$

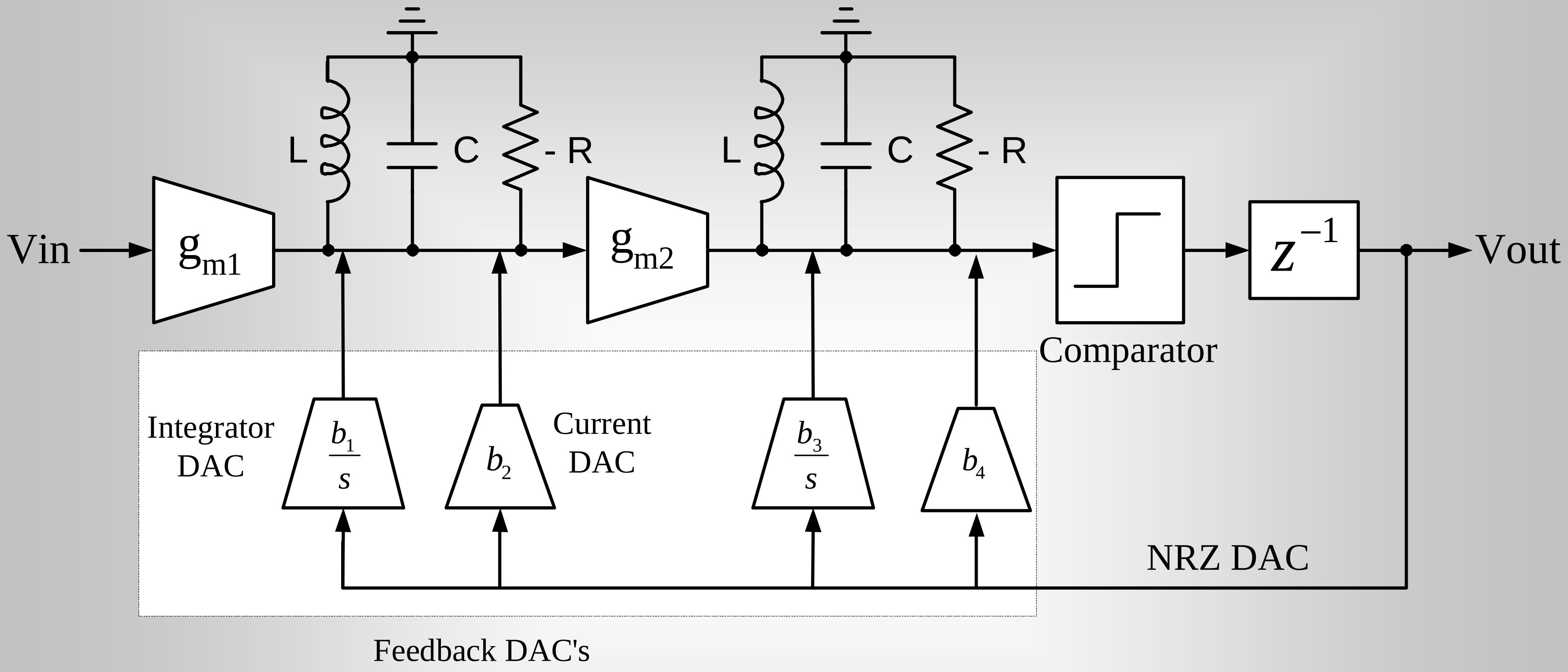
- $\text{SNR}_{\text{NRZ}} \approx (6\text{ -}12)\ \text{dB} + \text{SNR}_{\text{RZ/HRZ}}$

# Other non-idealities



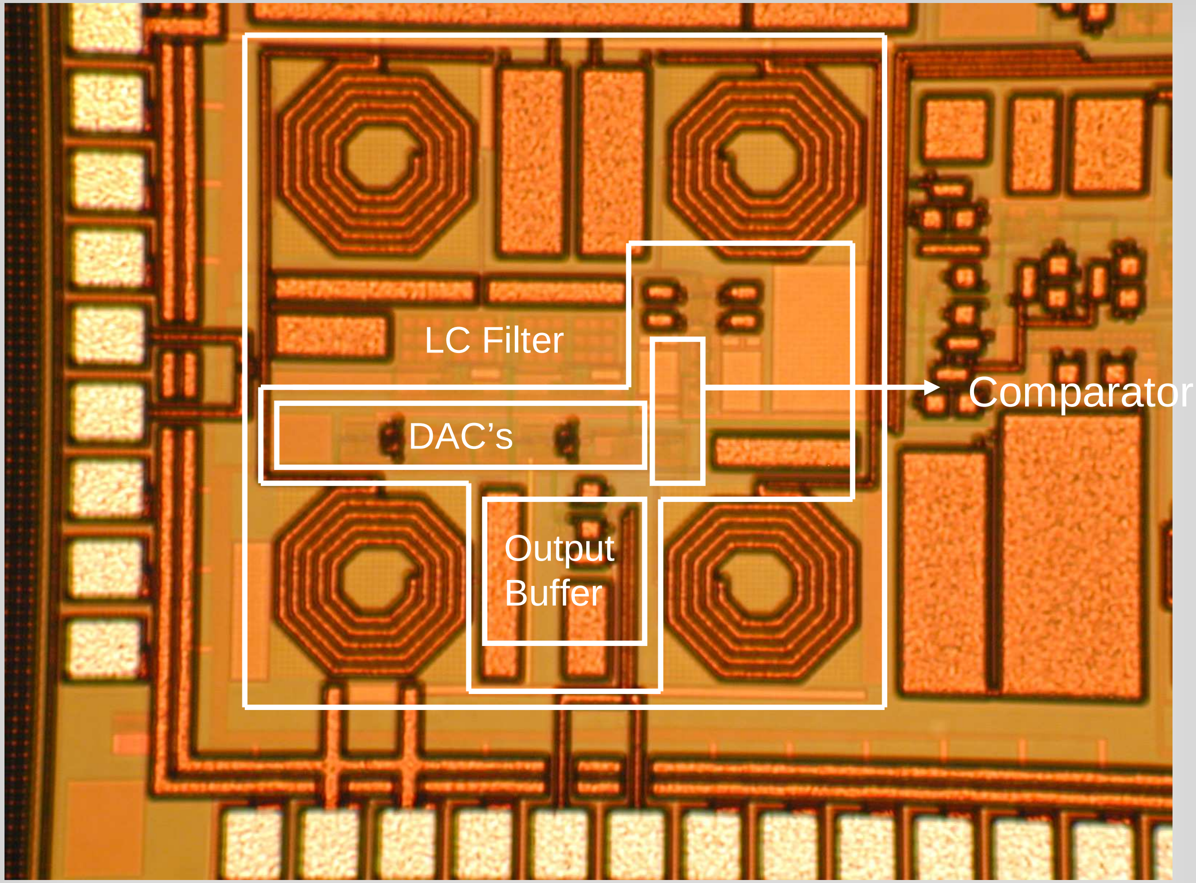
- Excess loop delay
- Quantizer metastability
  - Quantizer-DAC delay ($z^{-1}$)
- Unequal DAC pulse rise/fall time
  - Use fully differential RZ DAC (Current Steering)
  - Overall performance – use NRZ DAC
- Adjust for optimal loop performance to get best SNR
  - (PVT variations ~ 20%)
- Automatic tuning loop for best possible noise transfer function: **Global Tuning Strategy**

# LC Filter Architecture



- ✓ NRZ DAC – improved jitter performance
- ✓ Control of open loop transfer function coefficients
- ✓ $Z^{-1}$ delay

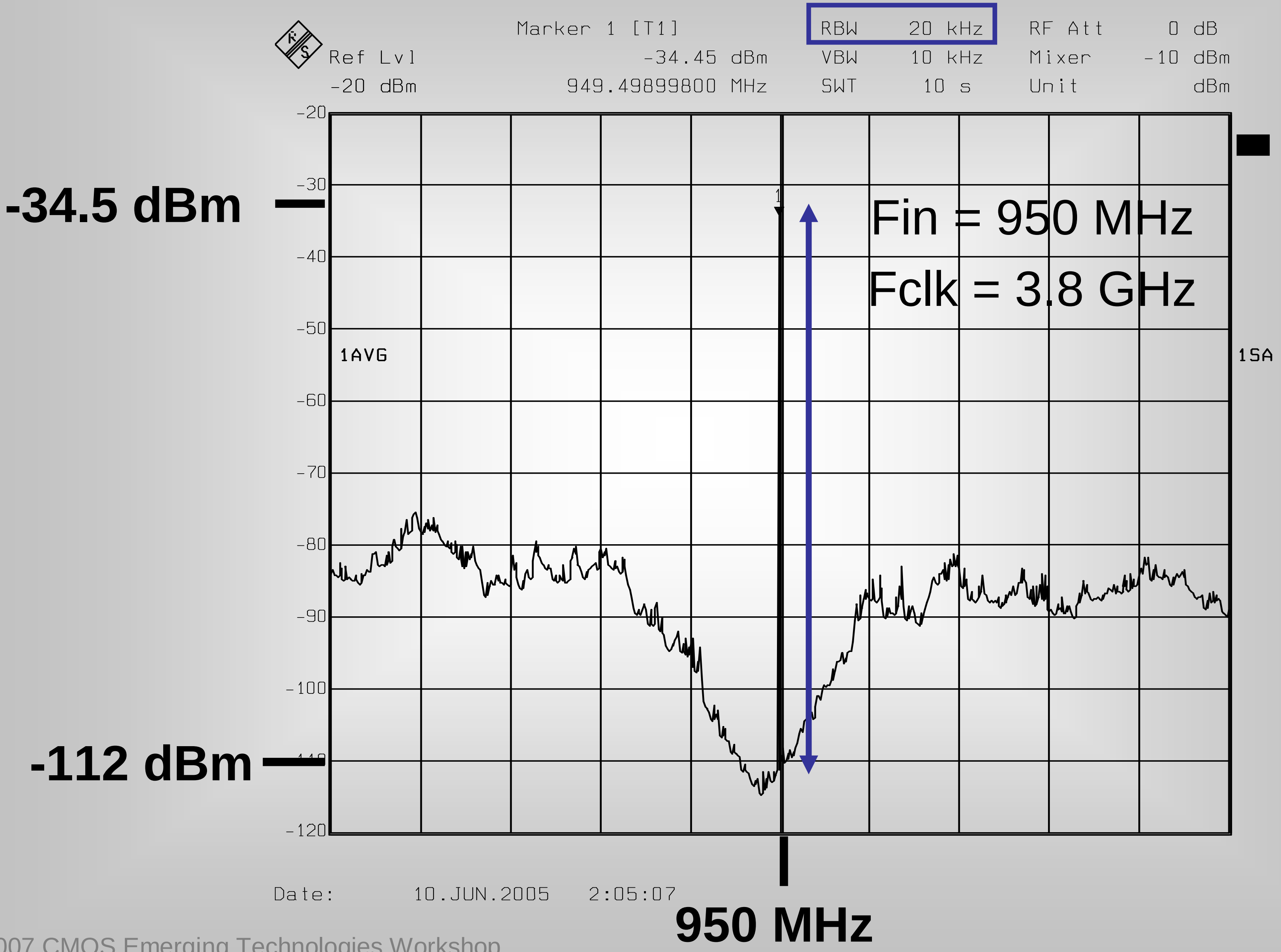
# Design Example: Chip microphotograph



Area = 1.08 mm$^2$ IBM 0.25 μm SiGe BiCMOS

**Bharath Kumar Thandri and Jose Silva-Martinez, "A 63 dB SNR, 75 mW bandpass RF ΣΔ ADC at 950 MHz using 3.8 GHz clock in 0.25 μm SiGe BiCMOS technology," *February 2007, IEEE Journal of Solid-State Circuits*.**

# Measured output spectrum of ADC



Marker 1 [T1]
-34.45 dBm
949.49899800 MHz

Ref Lvl
-20 dBm

RBW 20 kHz
VBW 10 kHz
SWT 10 s

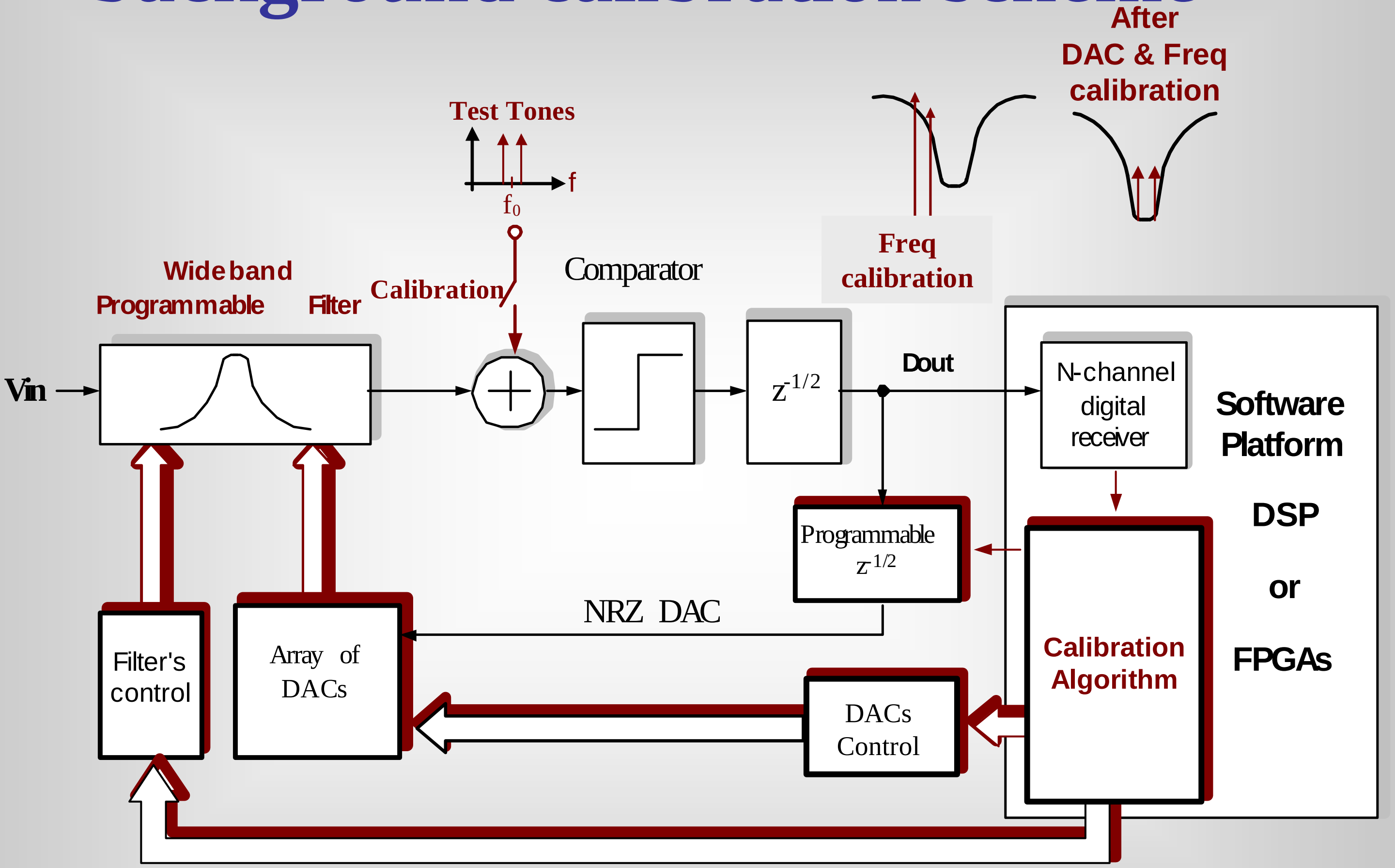
RF Att 0 dB
Mixer -10 dBm
Unit dBm

Date: 10.JUN.2005 2:05:07

Fin = 950 MHz

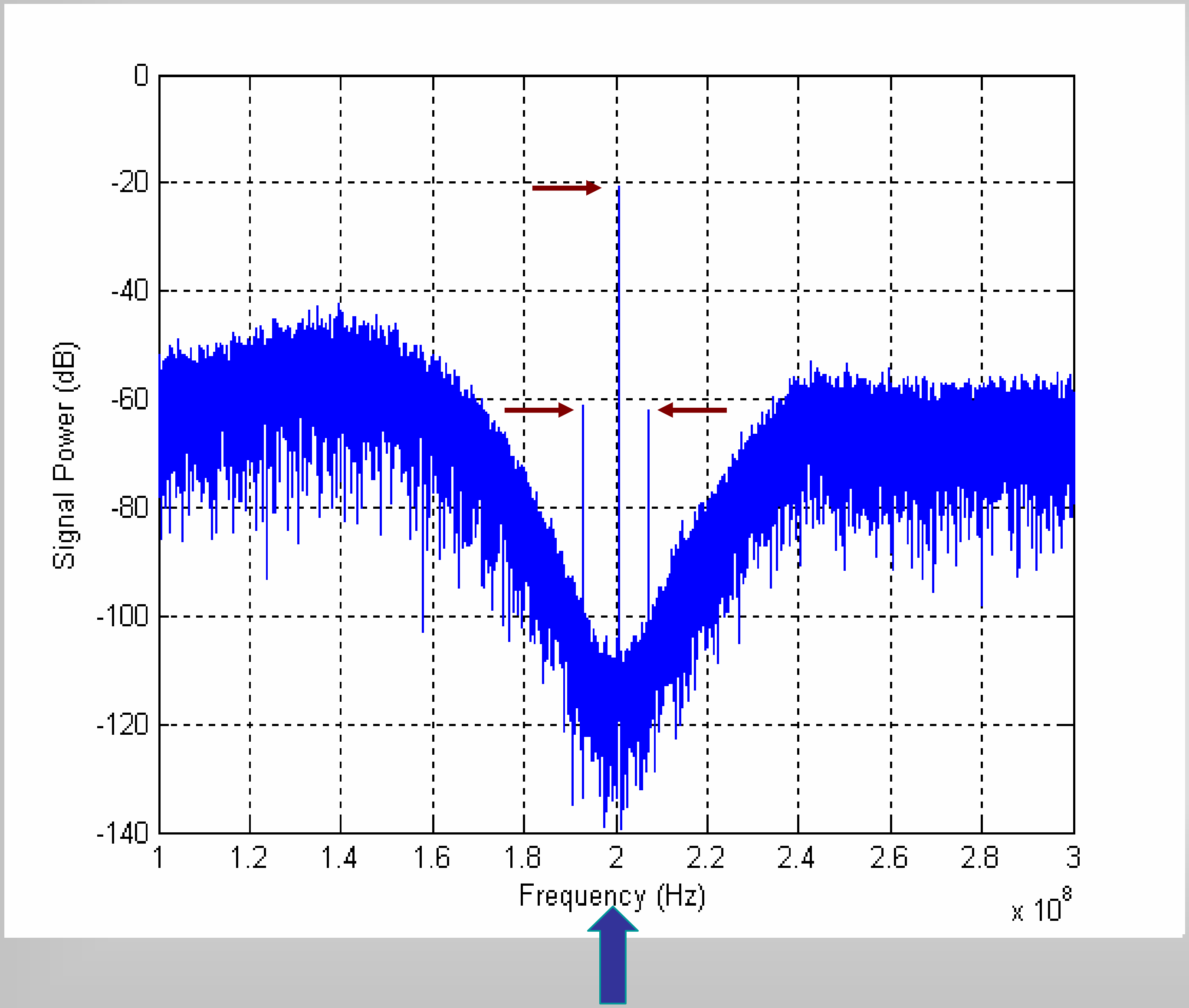
Fclk = 3.8 GHz

# Broadband BP-ADC with a digital based background calibration scheme



**Target (in progress)**: **A fully calibrated BW=10 MHz 13-Bit resolution (in a bandwidth of 1 MHz) 200 MHz ADC**

# SNR (after calibration) = 80 dB for 1MHz



- **Frequency tuning using an Adaptive LMS algorithm**
- **Scheme based on a two-tone test signal**
- **Digital based**

# Conclusion

- ADC → main component for software radio architectures
- RF ADC architecture uses CT filters with only NRZ DAC's => effects of clock jitter ↓
  - Reduced power (passive inductors)
  - Less noise (passive inductors)
  - Passive Inductors ➔ RF frequencies ➔ **Clock Jitter + Loop Delay issues**
- Currently demonstrated SNR>60 dB in a 1 MHz bandwidth with decent power consumption.
  - **Not in pure CMOS yet!**
- System level background calibration scheme to obtain maximum SNR is still a pending issue.
- Significant design challenges for CMOS direct RF ADC's

# References

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[11] B.K. Thandri and J. Silva-Martinez, “A 63 dB 75 mW bandpass ΣΔ RF ADC at 950 MHz using 3.8 GHz clock in 0.25 μm SiGe BiCMOS technology”, *IEEE Journal of Solid-State Circuit*s, vol. 42,no 2, pp.269-279, Feb 2007.
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