

---

# Circuits for high accuracy broadband ADC's

Sandeep Gupta  
Teranetics, Santa Clara, CA

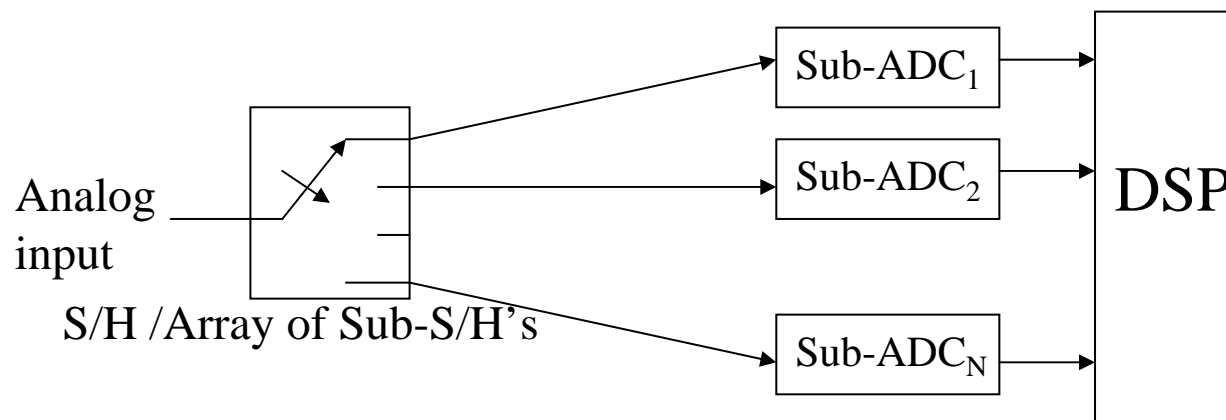
# Outline

---

- Introduction to time-interleaved architectures.
- Conventional Sampling architectures and their application space:
  - High accuracy ( $>7$ ENOB) for relatively lower sampling speeds ( $<1$ GS/s)
  - High sampling speeds,  $>1$ GS/s, up-to 20GS/s, lower accuracy ( $<7$  ENOB)
- Proposed architecture (ISSCC 2006) for broader application space.
- Measured results for a 1GS/s 11 bit ADC based on the proposed architecture.

# Time-interleaved architectures

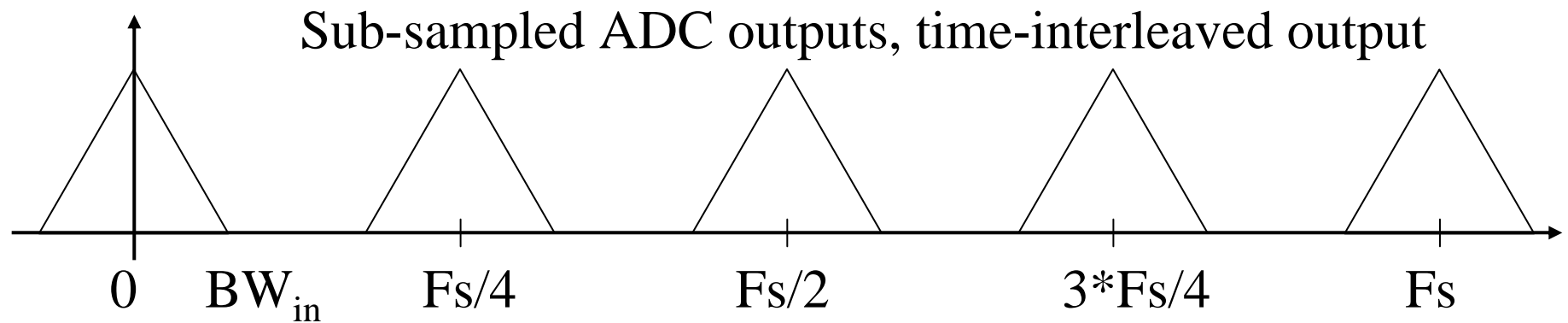
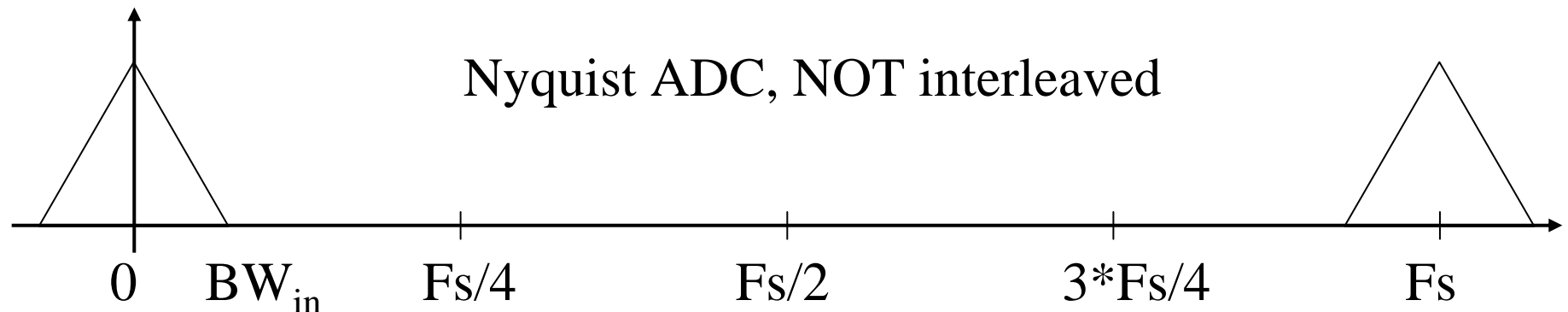
---



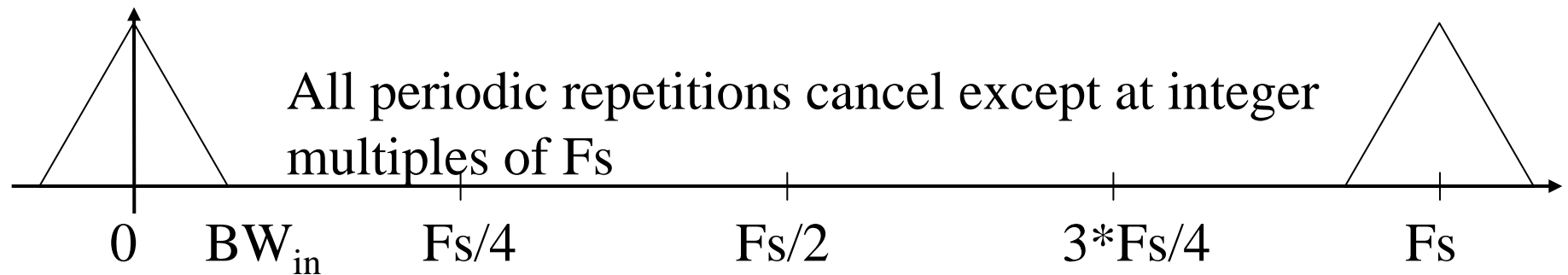
- Time interleaved architectures:
  - Efficient architectures for achieving accuracy at high speed.
- Caveats: SNR limitations due to
  - Gain & Offset mismatches: Present in all time-interleaved architectures.
  - Phase & bandwidth mismatch: Dominant only in some time-interleaved architectures

# Mismatch errors: Intuitive reasoning

---

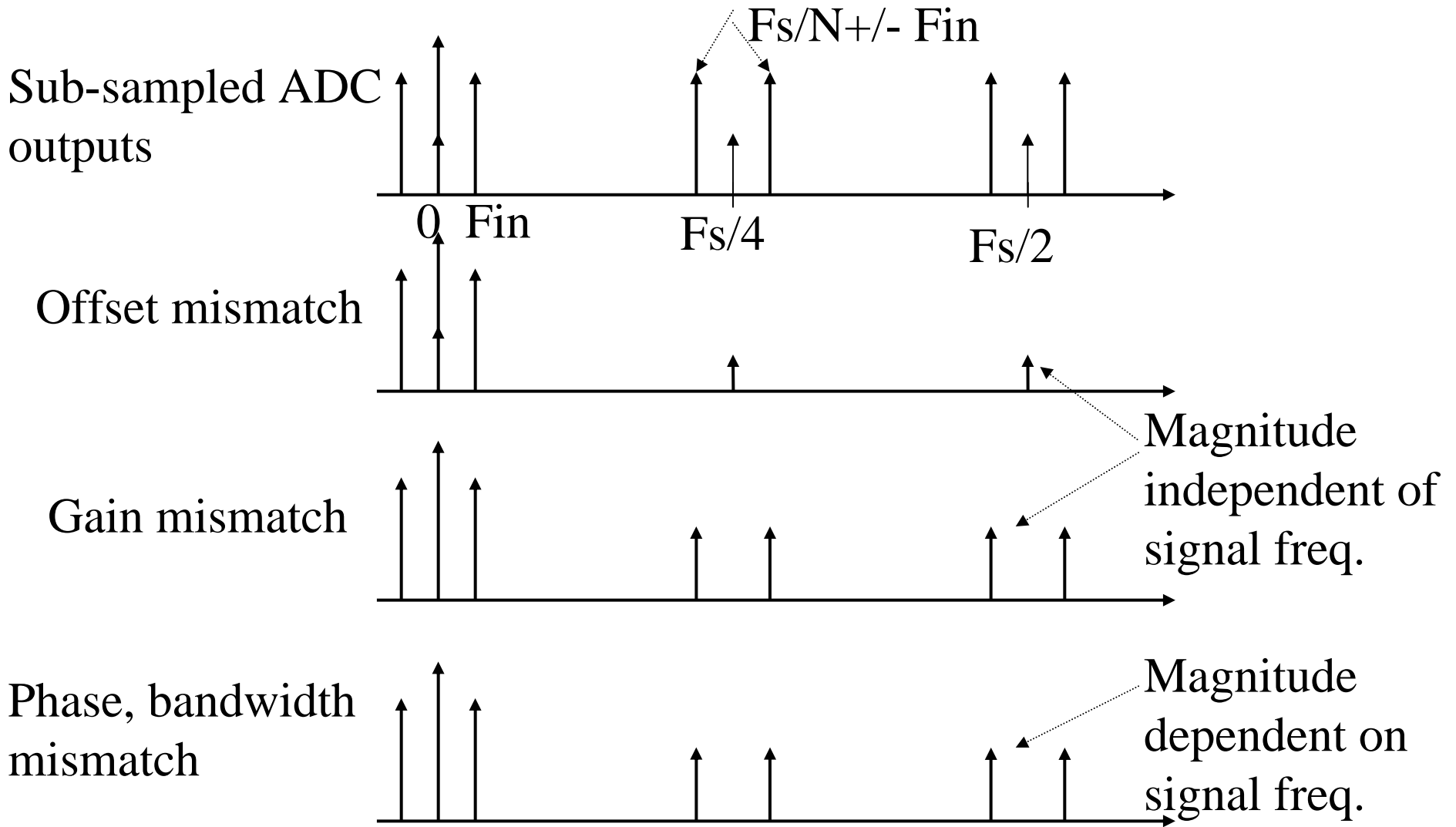


Sub-sampled ADC outputs recombined with perfectly matched array



# Offset, gain, Phase Skew and bandwidth mismatch

---



# Phase and bandwidth mismatches

---

- Phase mismatch:
  - Systematic mismatches in clocks
    - Layout  $\Delta RC$  effects
    - generation of sub-sampled clocks
  - Random mismatch in clocks
    - Jitter
- Sampling bandwidth mismatches
  - Primarily due to mismatch in switch resistance, layout  $\Delta RC$  effects.
  - Dominant mechanism the phase shift caused by different sampling bandwidths.

# SNDR vs. phase/bandwidth mismatch

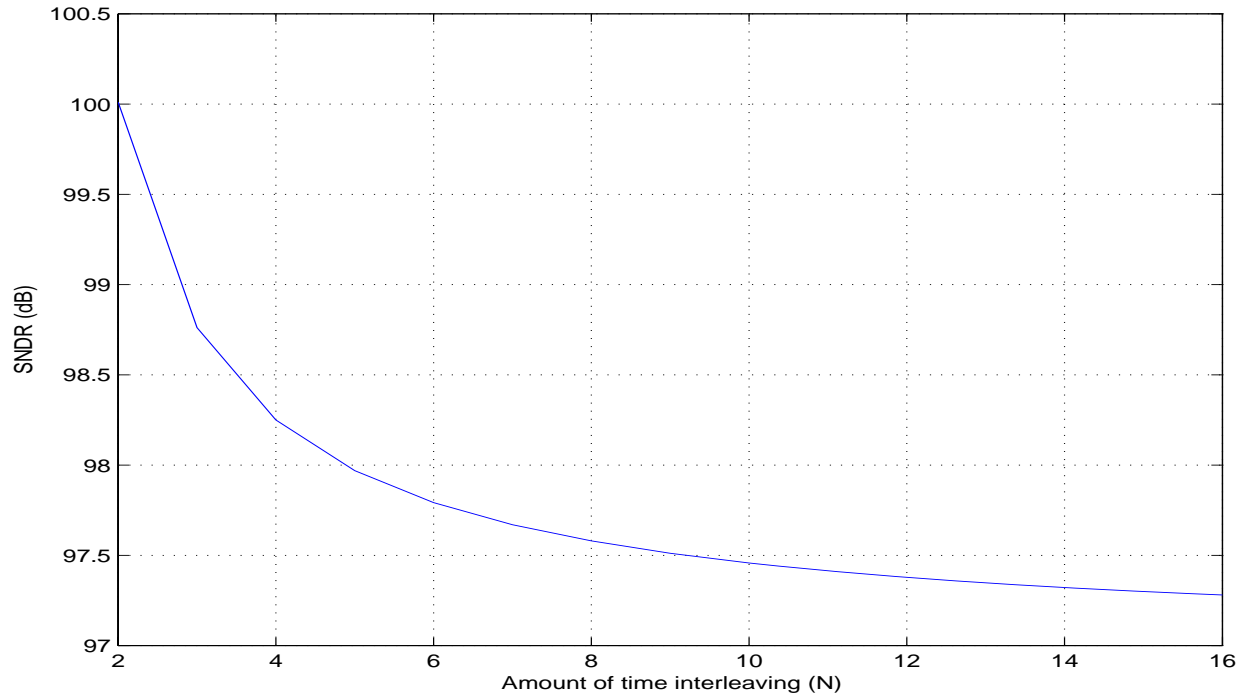
---

- SNDR  $\sim \alpha -20 \cdot \log_{10}(\text{phase error})$
- Phase error (jitter/skews) =  $2\pi \cdot f_{in} \cdot (\sigma_j / f_s)$ 
  - Wherein,  $\sigma_j$  is the RMS jitter OR the standard deviation of the clock skew
  - $f_s$ , the sampling clock frequency
- Phase error due to sampling bandwidth mismatch =  $2\pi \cdot f_{in} \cdot \sigma_N / f_{BW}$ 
  - Wherein  $f_{bw}$  is the sampling bandwidth of a normalized sub-channel.
  - Wherein  $\sigma_N$  is the standard deviation of the bandwidth mismatch between sub-channels.

# SNDR vs. interleaving factor

---

- SNDR  $\propto -10 \cdot \log_{10}[1 - 1/N]$ , mismatch  $\sigma$  being constant. (Ref: Seng Pan U et. al., IEEE trans. Inst. and measurement, Aug. 2004.)

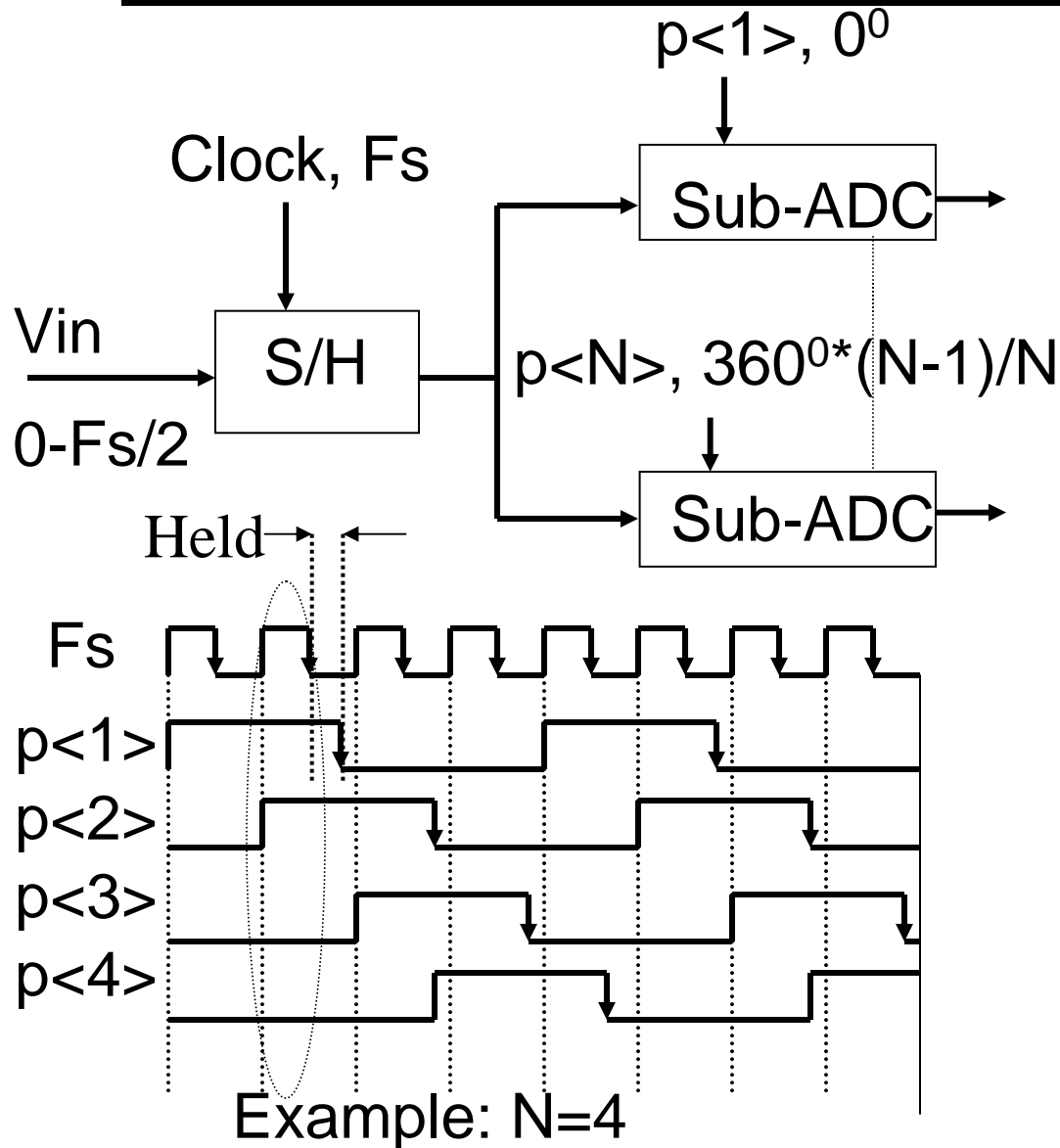


- However, physically mismatches (systematic/random) can increase with N (not taken in account in graph above)

---

# Conventional Architectures and their application landscape

# Conventional architecture 1



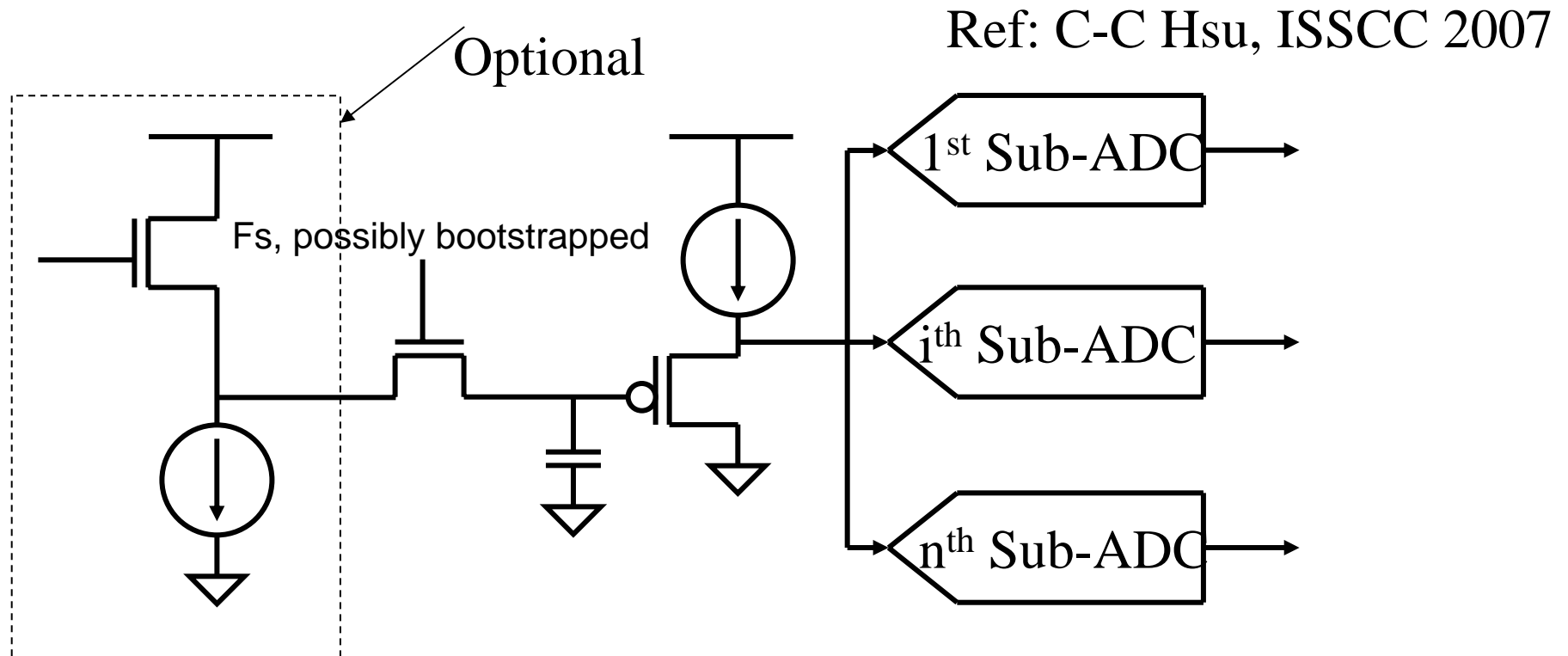
Advantage:

1. Phase skews in  $p\langle i \rangle$ , Bandwidth mismatch errors, not much loss of accuracy.

Disadvantages:

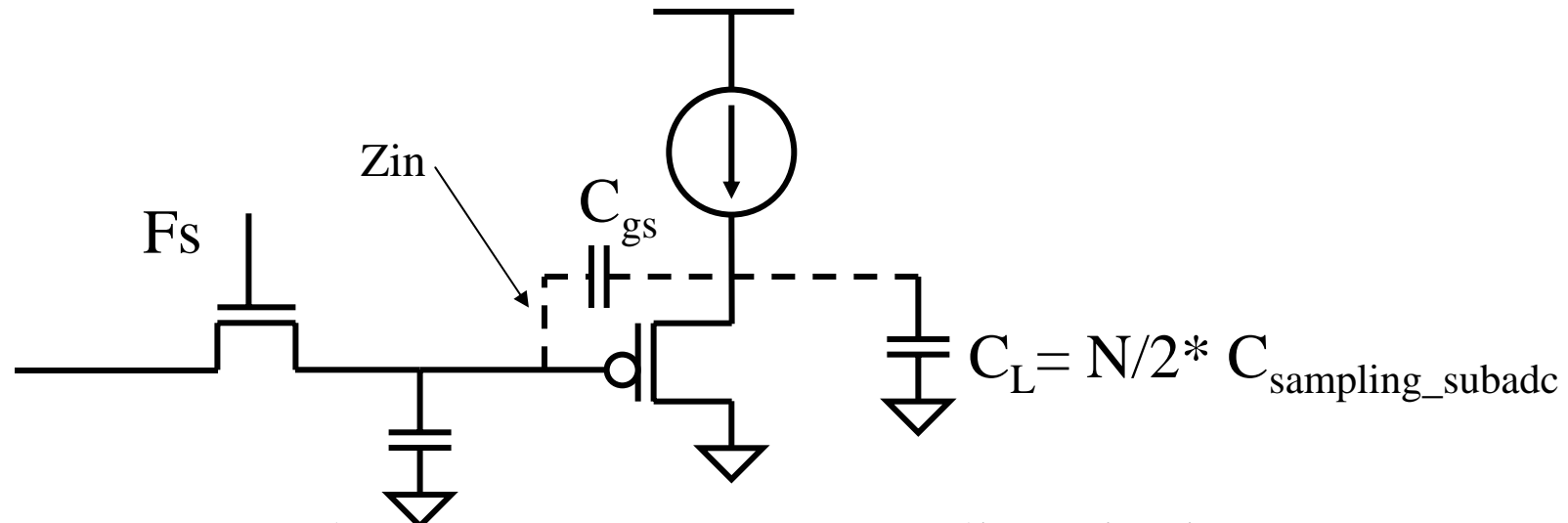
1.  $N/2$  Sub-ADCs loading on first sampler limits its BW, performance,
  - Sub-ADC sampling speed still high, if  $N$  kept low.
2. Sub-ADC input signal held only for short time  $<(T/2=1/2F_s)$

# Possible implementation



- Full speed operation=> bottom plate sampling scheme not feasible
- Charge injection, tracking distortion in the switch
- Additionally in the source follower driving the Sub-ADC's ...

# Source follower buffer for Sub-ADC's



- $C_L \propto N/2$  sub-ADC caps, power/non-linearity increases as  $N$  increases for a given Sub-ADC speed to achieve high  $F_s$ .
- If  $\omega C_L \gg (g_{mb} + g_{ds})$ ,  $Z_{in} = 1/sC_{gs} + 1/sC_L - g_m/\omega^2 C_{gs} C_L$
- As  $C_L$  increases, negative impedance becomes worse in value, that too at lower frequencies.
  - Transfer function ripple in the ADC increases.
  - Further restricts value of  $N$ , and therefore  $F_s$

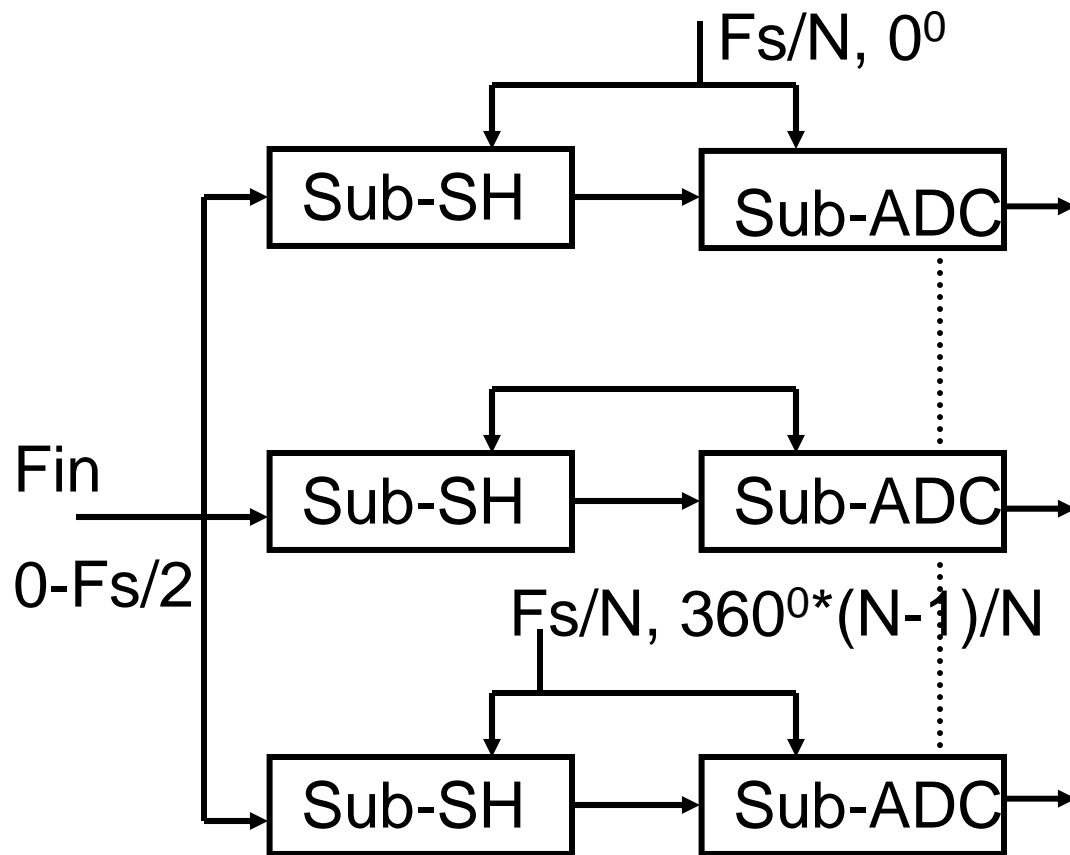
# Applications for conventional architecture 1

---

- Based on
  - a) no accuracy loss due to phase/bandwidth mismatch
  - b) Restriction on value of N for a given speed, accuracy and choice of architecture of sub-ADC,
- Optimally applied for
  - Relatively lower speed time-interleaving (<1GS/s), medium to high accuracy (~7-9 ENOB)

# Conventional architecture 2

---



Advantages:

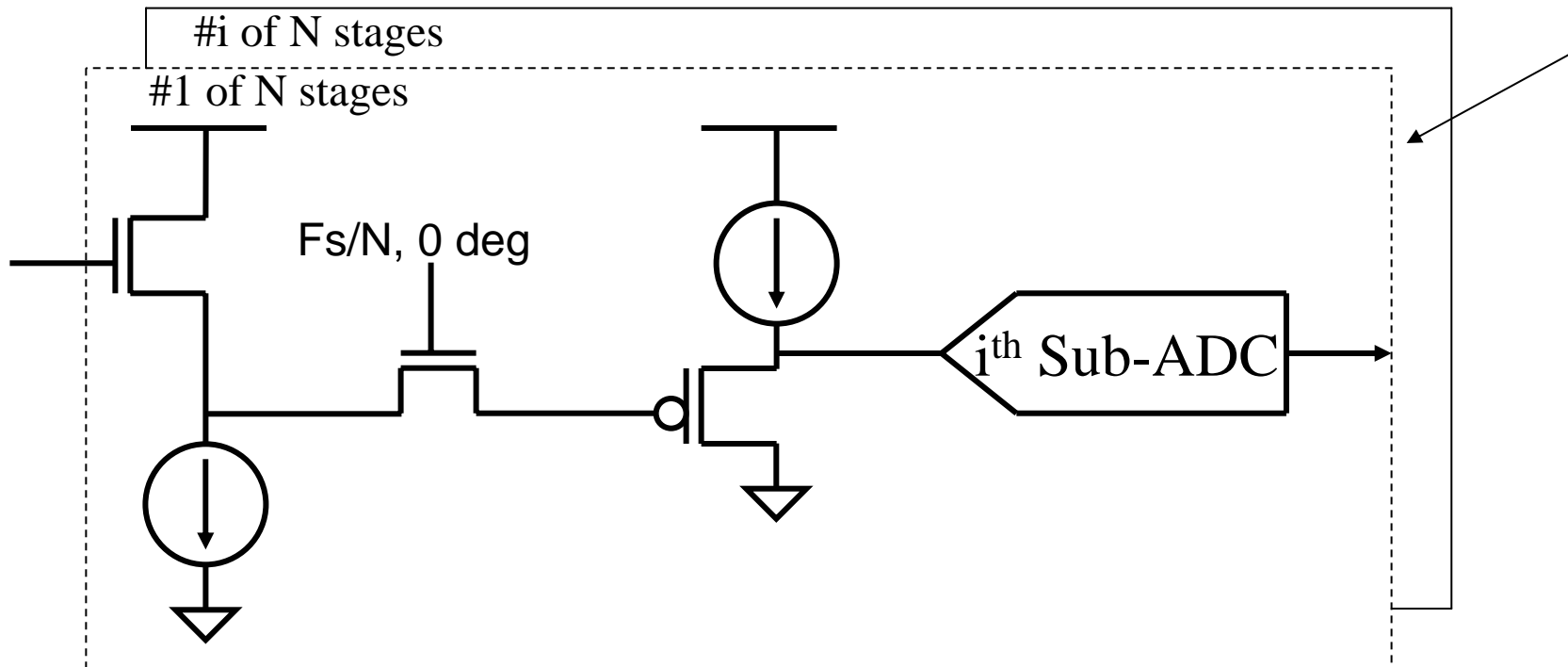
1. Scalable, high speed operation.
2. No need for  $F_s$  rate clock, fully sub-sampled

Disadvantage:

Complex DSP for phase & bandwidth mismatch

-residual errors degrade SNR, worse at high  $N$  and high  $F_{in}$

# Possible implementation



- Source follower/sub-channel performance independent of  $N$ .
- Phase/bandwidth mismatch increases severely as  $N$  increases, limits accuracy.

# Applications for conventional architecture 2

---

- Based on
  - a) Value of N not restricted for realizing BW/high accuracy in the sub-channel circuits
  - b) Phase/bandwidth mismatch of channels limiting accuracy of the time-interleaved output, worst at high N.
- Optimally applied for
  - Relatively higher sampling speeds ( $\sim 1\text{GS/s} < F_s < \sim 20\text{GS/s}$ ), low to medium accuracy ( $\sim < 7$  ENOB)

---

Proposed architecture (ISSCC 2006)  
for broader applications.

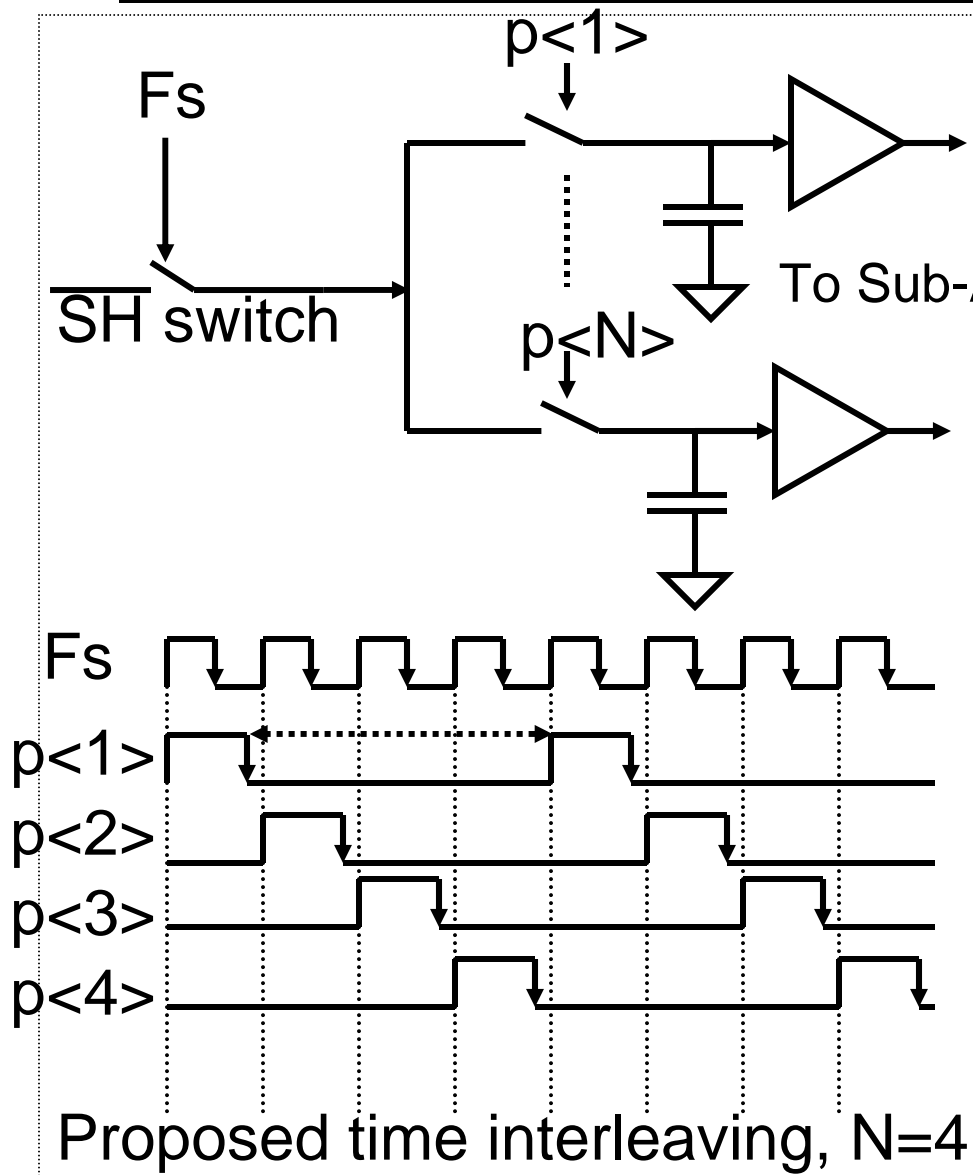
# Need for newer architecture

---

- Need to
  - Cover the landscape of high speed (  $\sim \geq 1\text{GS/s}$ ) time-interleaved ADC's with a considerable higher accuracy.
  - AND/OR
  - Possibly realize at lower speeds ( $< 1\text{GS/s}$ )
    - for the same power higher accuracy ( $> 9\text{ ENOB}$ )
    - OR for the same accuracy lower power

Compared to conventional architecture 1.
- Based on adopting the advantages of each of the conventional architectures mentioned before, and mitigating the disadvantages.
  - Ref: S. Gupta. Et. al., ISSCC 2006
  - The target application here was  $1\text{GS/s}$ ,  $\sim 9\text{ENOB}$  at very low power, in relatively older CMOS  $0.13\mu\text{m}$  technology.

# Architecture development: Step 1

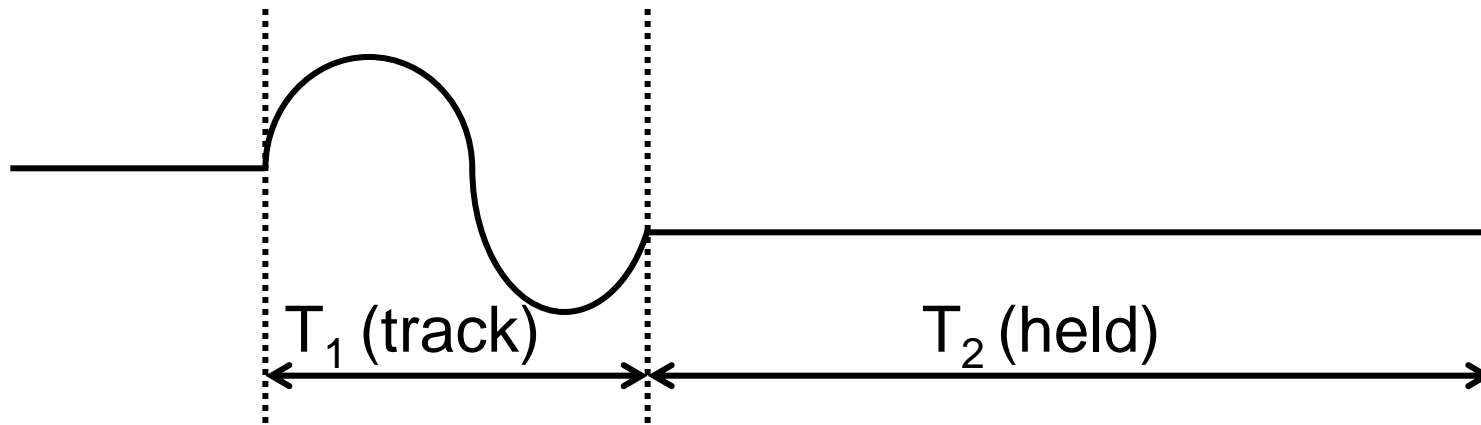


- $p\langle i \rangle$  duty cycle  $< 1/N$
- **1 sub-sampler loads the S/H switch at any time.**
- BW, performance independent of  $N$ , scalable to high speed.
- $p\langle i \rangle$  turnoff when  $F_s$  is off
  - Phase skews do not contribute to loss of SNR.
- Sub-ADC input held longer.

# Desirables for performance/power

---

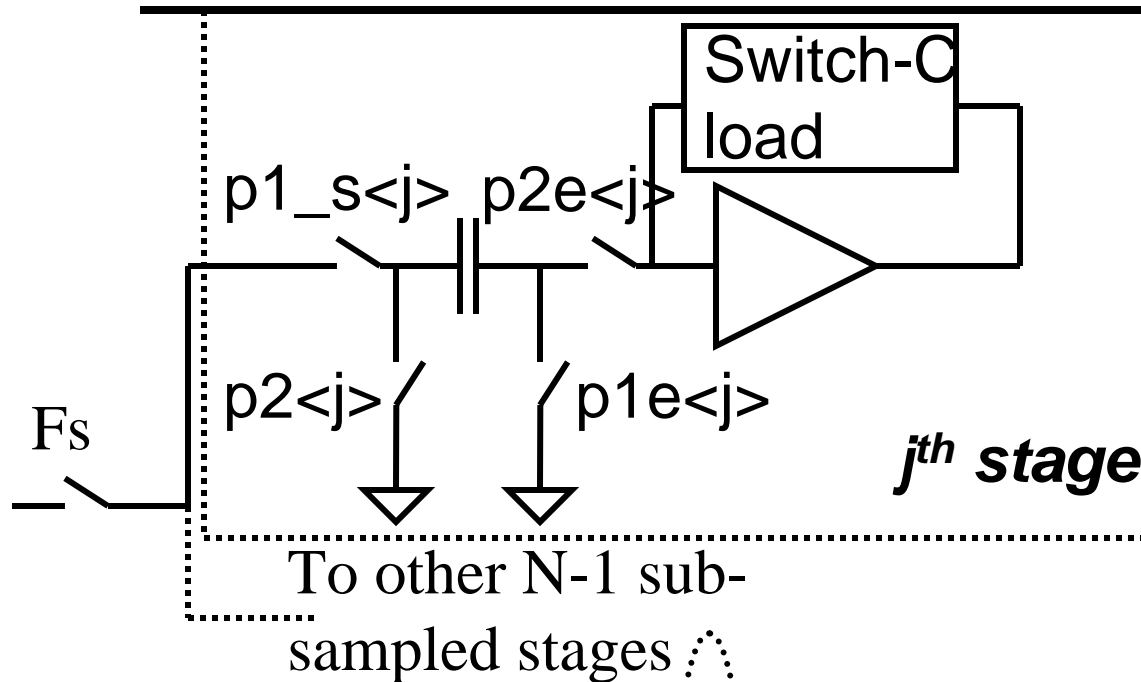
- Sample and hold instead of a track and hold



$$T_1 + T_2 = T_{\text{sub}} = N/F_s, \quad T_1 < (T = 1/F_s)$$

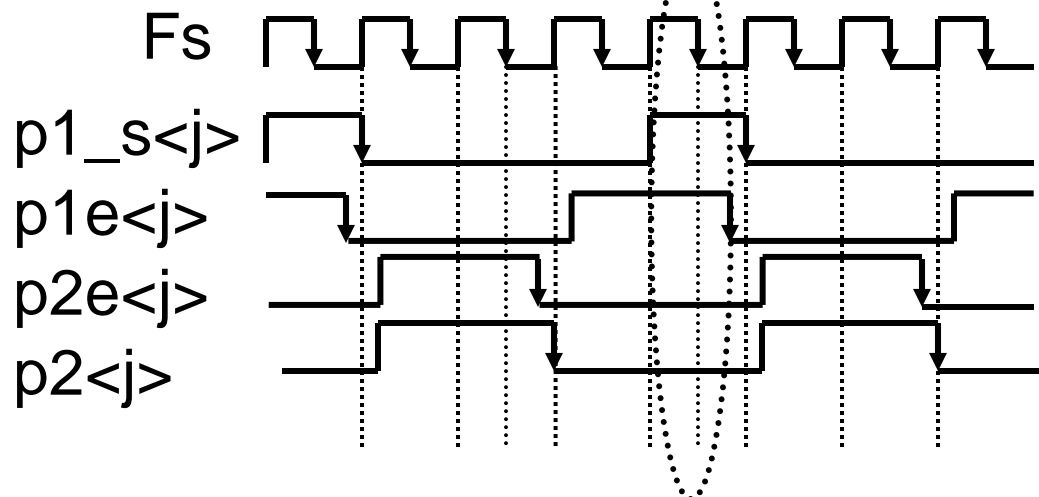
- Use double sampling, for maximal power utilization.
- Buffer faces full swing -- replace with a virtual ground amplifier

# Architecture development: Step 2



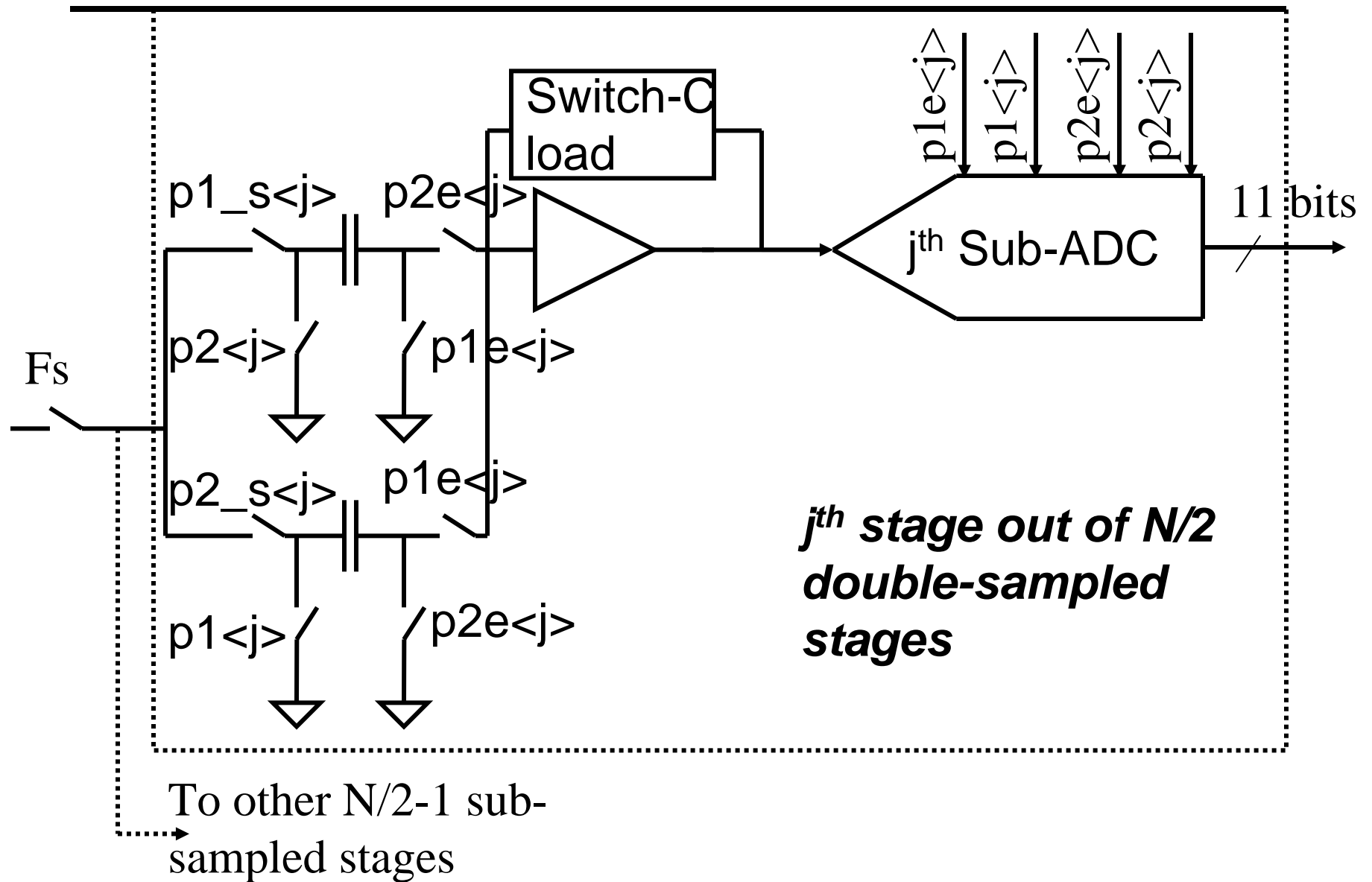
- Adapt structure in step 1 to bottom plate sampling
  - Can achieve all three desirables

Clocking scheme:



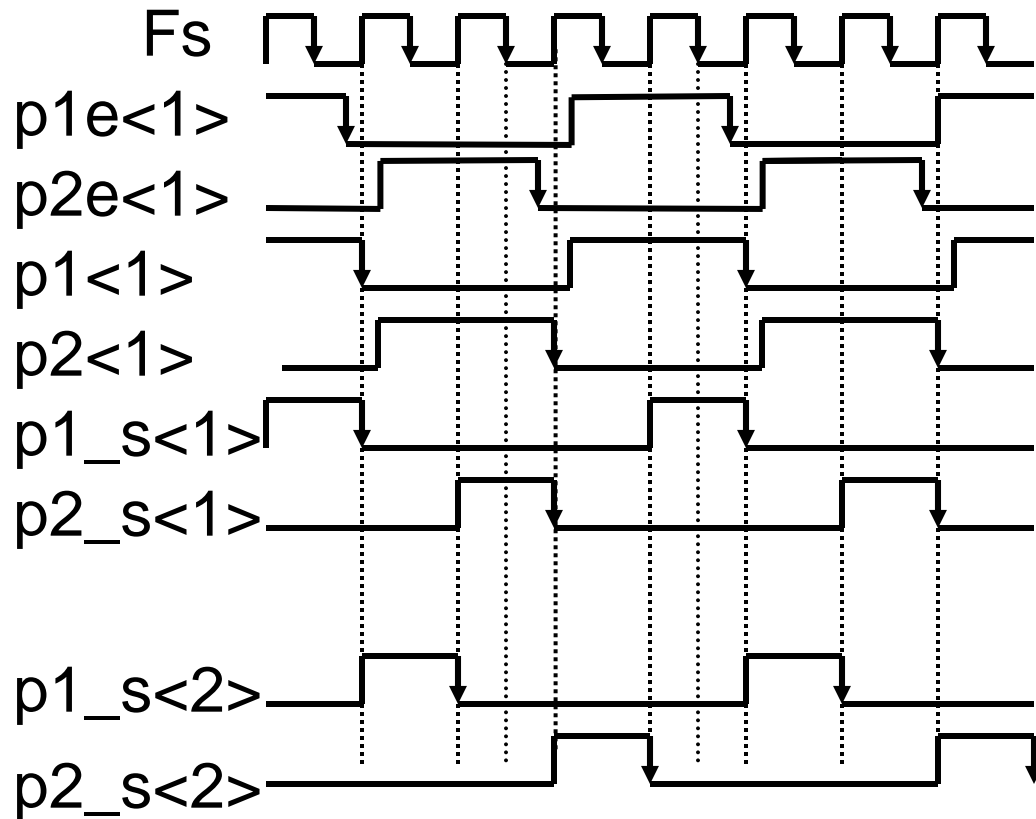
- $p1e$  turns off during the off period of  $F_s$  clock.
- $p1\_s$  is **the**  $1/N$  duty cycle clock.

# Final Time-interleaved Architecture



# Clocks for the Final Architecture

---



- Clocks generated from  $N$  phases,  $360/N^\circ$  apart.
- Sub-sampling track occurs during the on period of  $p1\_s$  AND  $p2\_s$ .

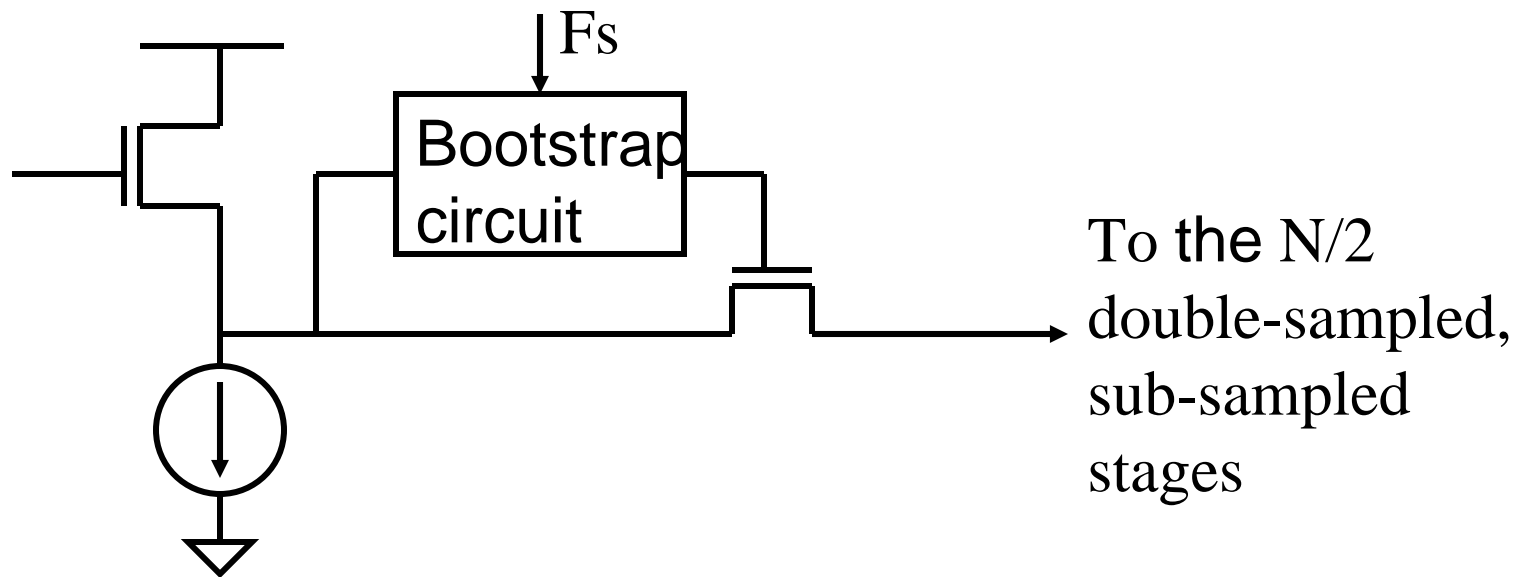
Example clocks for  $N=4$ .

In this design  $N=8$

# ADC linearity

---

- Dominated by the first switch's track mode and charge injection distortion.
  - First switch bootstrapped
    - maintain constant  $V_{GS}$ .
  - First switch driven by a source follower



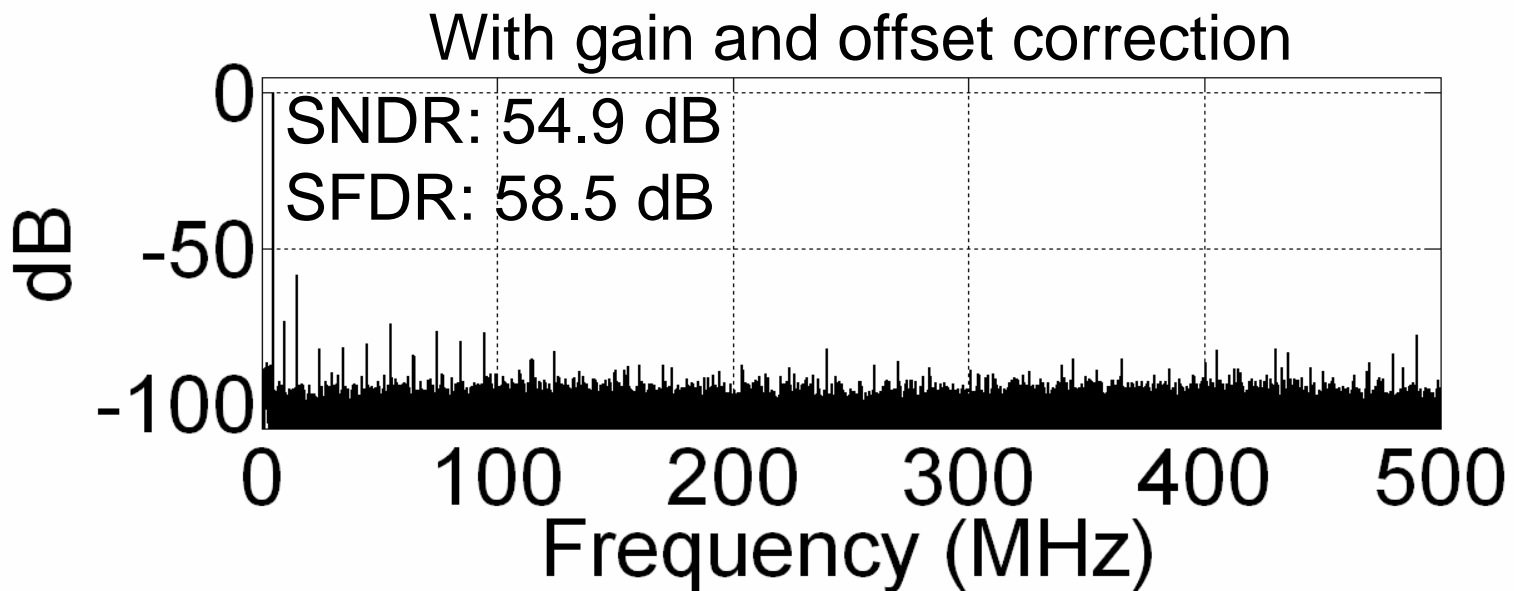
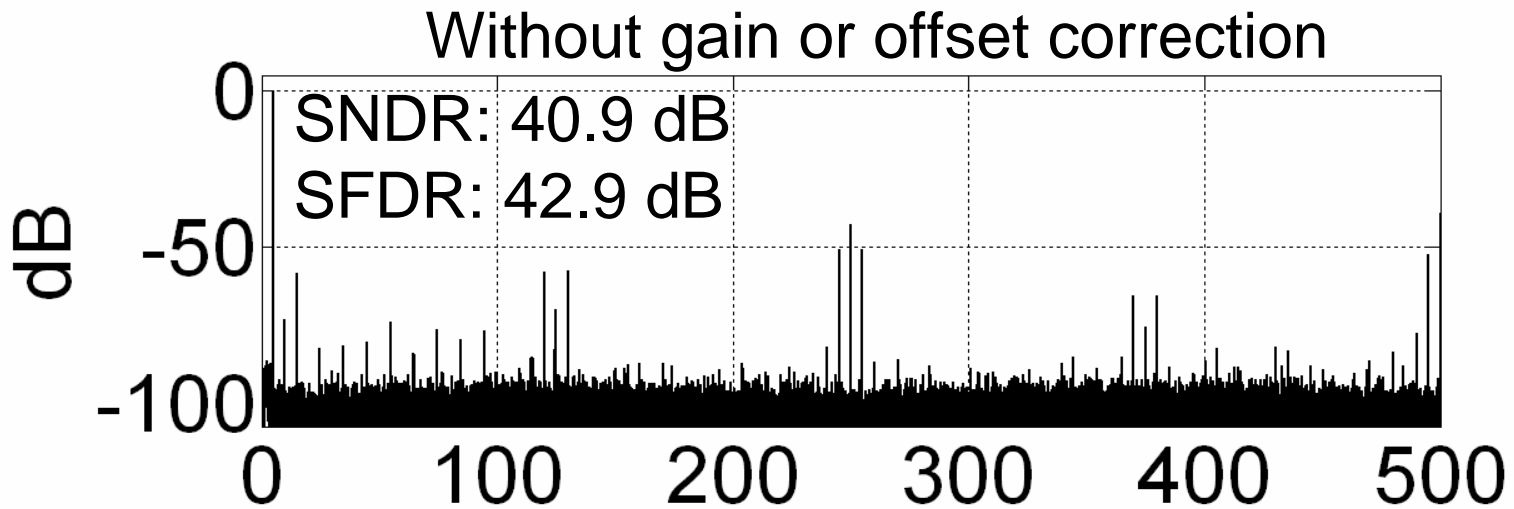


---

# Measured results for the proposed architecture

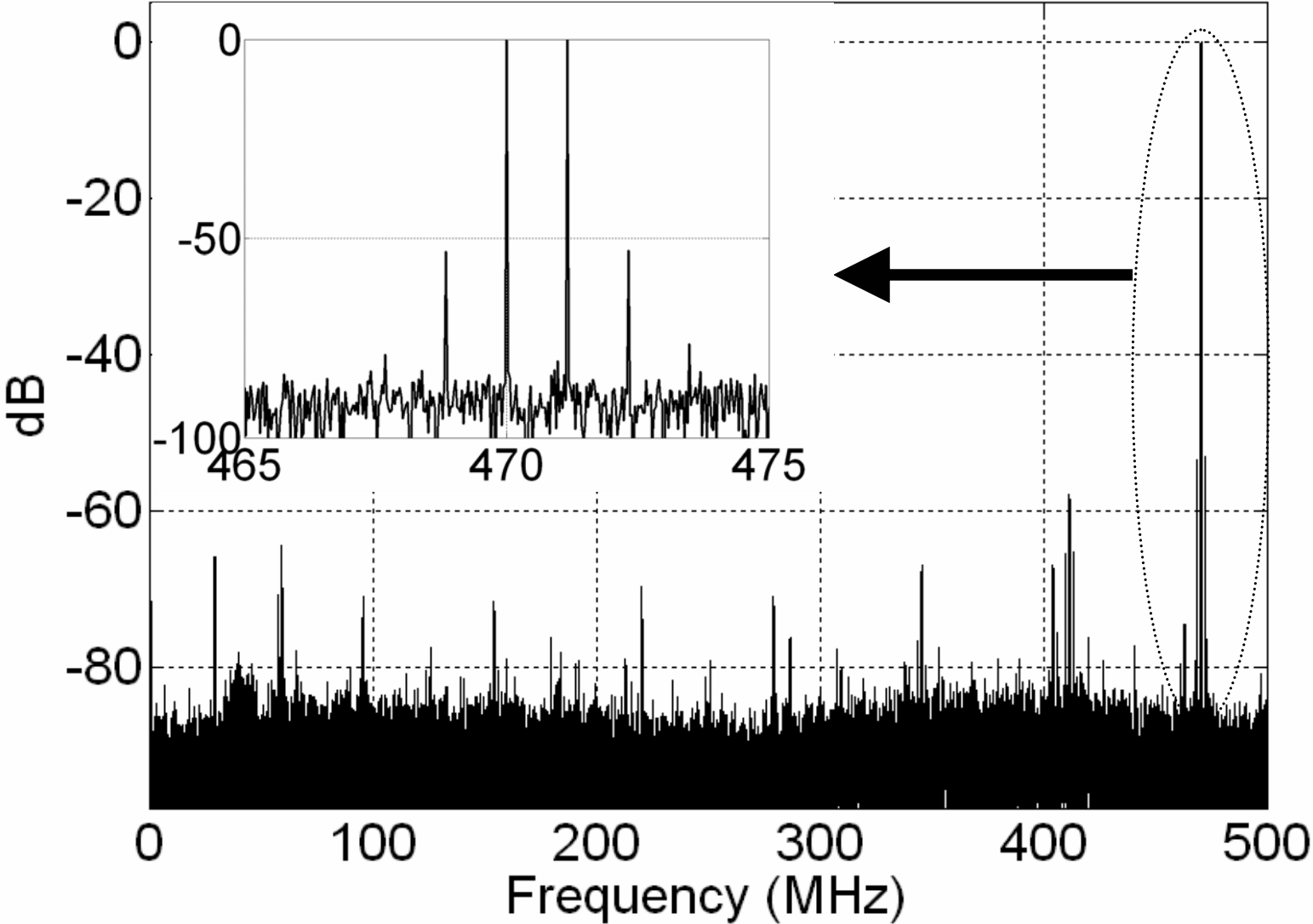
# FFT with & w/o Gain/Offset errors

---



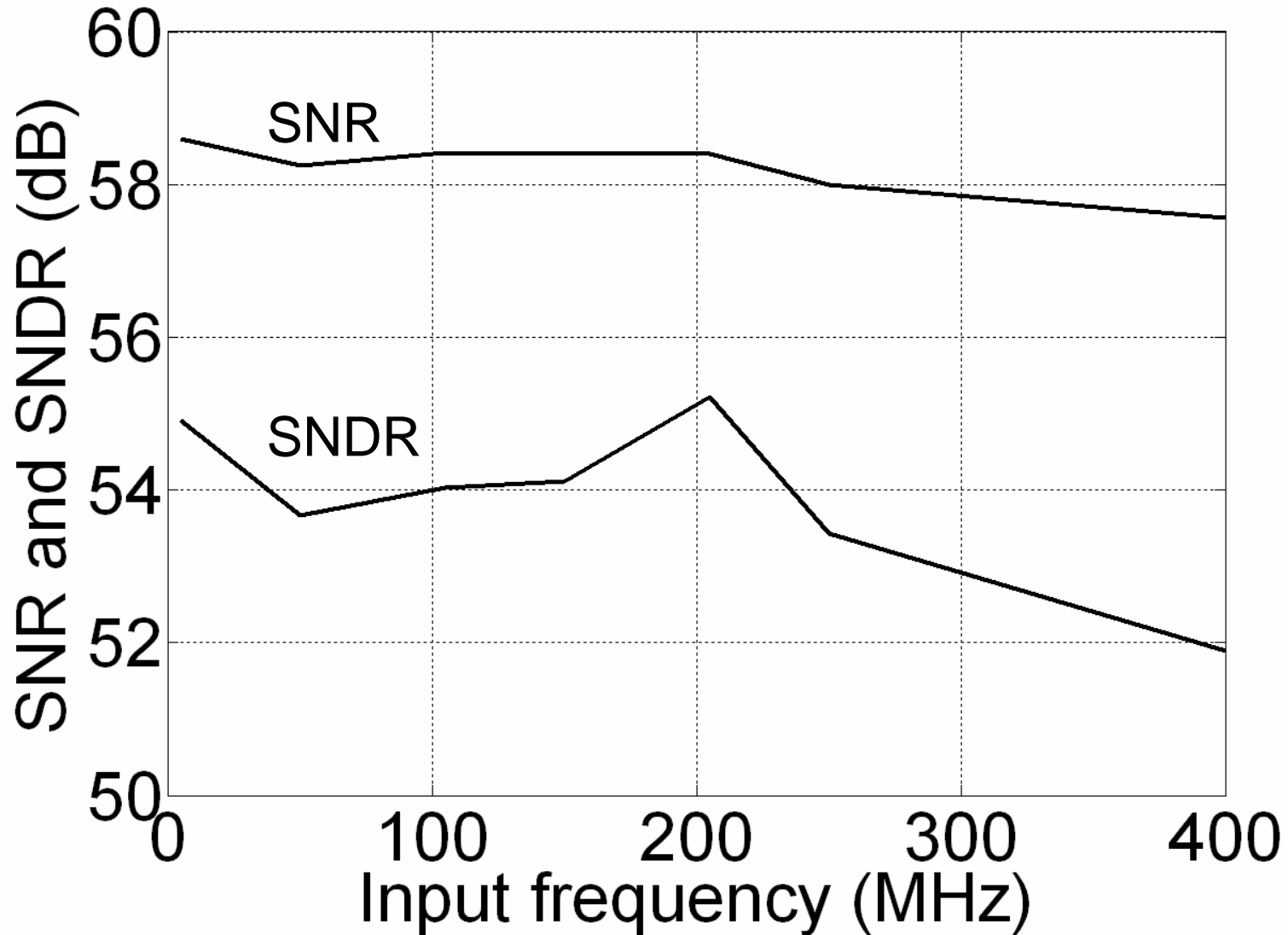
# FFT for 2-tones at high frequency

$f_{in} = 470 \text{ \& } 471 \text{ MHz}$ ,  $SFDR(\text{Signal}/\text{IM3}) = 53.1 \text{ dB}$



# SNDR and SNR vs. frequency

---



# ADC performance summary

Sample rate	1 GS/s
Effective Resolution BW	500MHz
Resolution	11 bits
SNR at 5 MHz	58.6 dB
SNR at 400 MHz	57.6 dB
Peak SNDR	55 dB
2-tone IM3 @ 470 MHz	53 dB
SFDR @ 5MHz	58.5 dB
Power consumption	250 mW
ADC core area	3.5 mm <sup>2</sup>
Technology	0.13 μm digital CMOS
FOM (Power/2 <sup>ENOB</sup> *2*ERBW)	0.5pJ/conversion step

# Talk Summary

---

- Applications landscape of time-interleaved ADC's studied
  - Conventional architecture 1 usable for lower speed, higher accuracy
  - Conventional architecture 2 more optimal for higher speed, lower accuracy.
  - Proposed architecture (ISSCC 2006) covered a broader landscape of ADC's providing at
    - Higher speeds: higher accuracy,
    - Lower speeds:
      - same accuracy at low power
      - higher accuracy at similar power