Variability in Deeply Scaled CMOS and What Can Circuit Designers do About It

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Outline

- What kind of variability matters?
- Test structures for measuring variability in logic
- Analysis of variability measurements in 90nm CMOS
- What to do about variability?

Temporal vs. Spatial Variability

- **Nature of process variability**
  - Within-die (WID), Die-to-die (D2D), Wafer-to-wafer (W2W)
  - Systematic vs. random
- **Spatial variability/correlation**
  - Device parameters (CD, t_{ox}, …)
  - Supply voltage, temperature
- **Temporal variability/correlation**
  - Within-node scaling, Electromigration, Hot-electron effect, NBTI, self-heating, temperature, SOI history effect, supply voltage, crosstalk [Bernstein, IBM J. R&D, July/Sept 2006]

Systematic and Random Device Variations

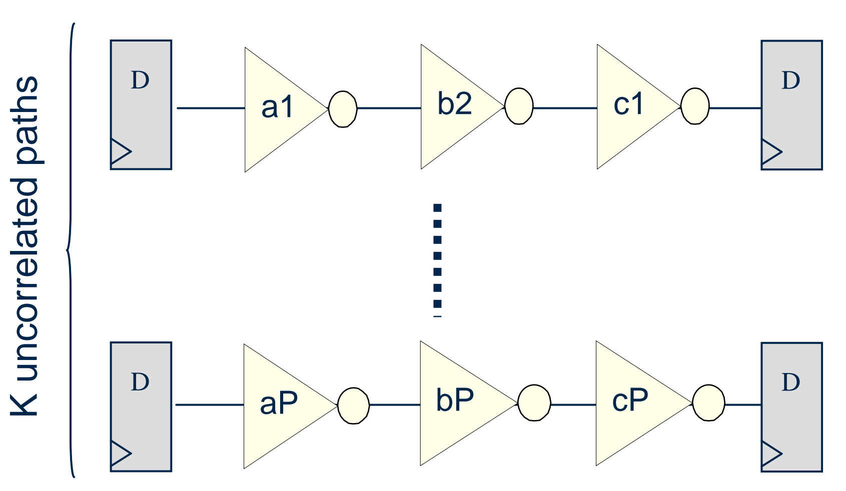
Parameter	Random	Systematic
Channel Dopant Concentration Nch	**Affects Δ_{Vth} [1]**	**Non-uniformity in the process of dopant implantation, dosage, diffusion**
Gate Oxide Thickness Tox	**Si/SiO_2 & SiO_2/Poly-Si interface roughness[2]**	**Non uniformity in the process of oxide growth**
Gate Length L	**Line edge roughness (LER)[3]** 45 nm lines/90 nm pitch	**Lithography:** **Proximity effects, RET, OPC, PSM** **Resist development, etching, etc**

Largest[4]

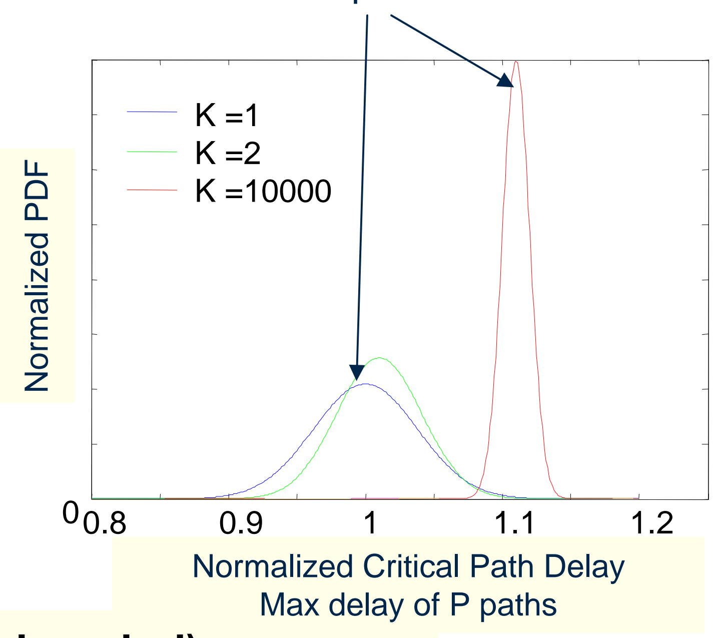
Systematic, lithography-induced variation dominates

[1] D. Frank et al, *VLSI Symposium*, Jun. 1999 .
[2] A. Asenov et al, *IEEE Trans on Electron Devices,* Jan. 2002.
[3] P. Oldiges et al, *SISPAD 2000,* Sept. 2000.
[4] M. Orshansky et al, *IEEE Trans on CAD*, May 2002.

Chip Yield Depends on Inter-Path Correlation



Mean delay increases as K increases for uncorrelated paths

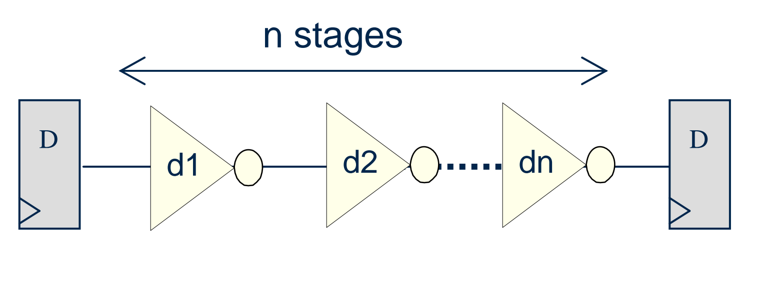


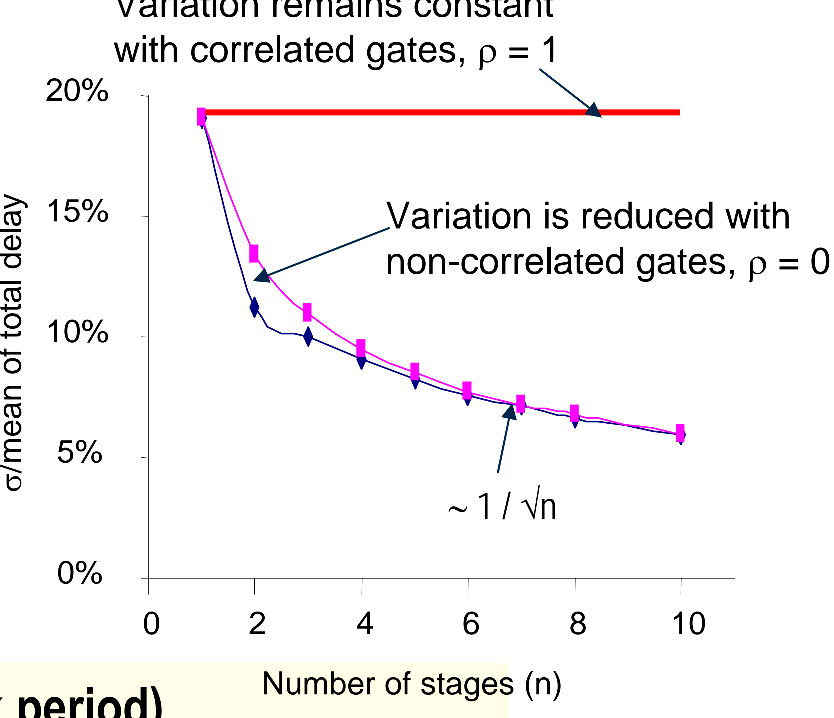
- **Yield = Pr (max delay of K paths < clock period)**
- **K = 1 gives highest yield**

Correlated paths reduce impact of variation

Bowman et al, *JSSC*, Feb 2002 .

Chip Yield Depends on Inter-Gate Correlation

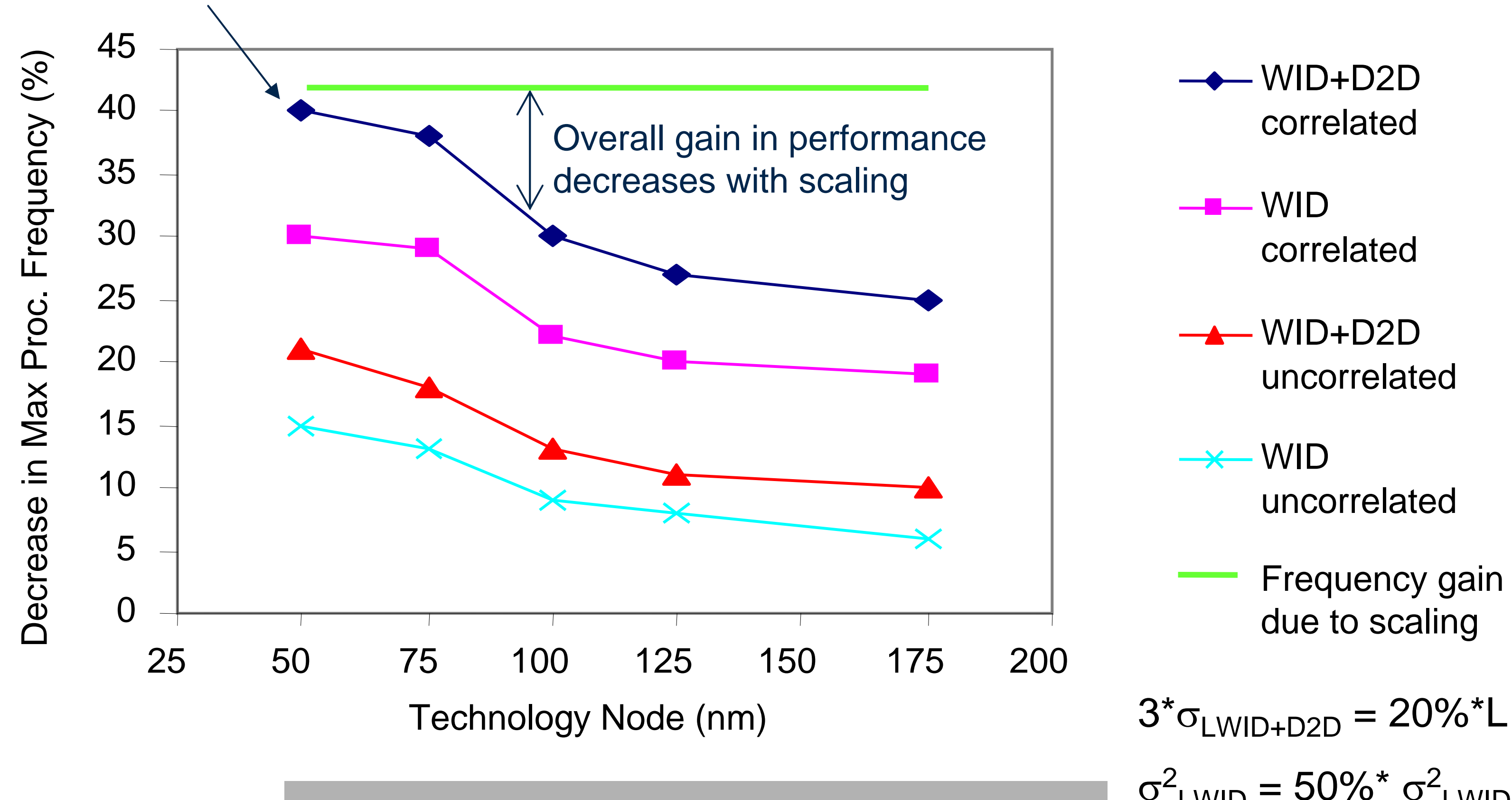




- **Yield = Pr (sum of n delays < clock period)**
- **ρ = 0 gives highest yield through increased averaging**

Non-correlated gates in a path reduce impact of variation

Impact of Variation on Performance Gain



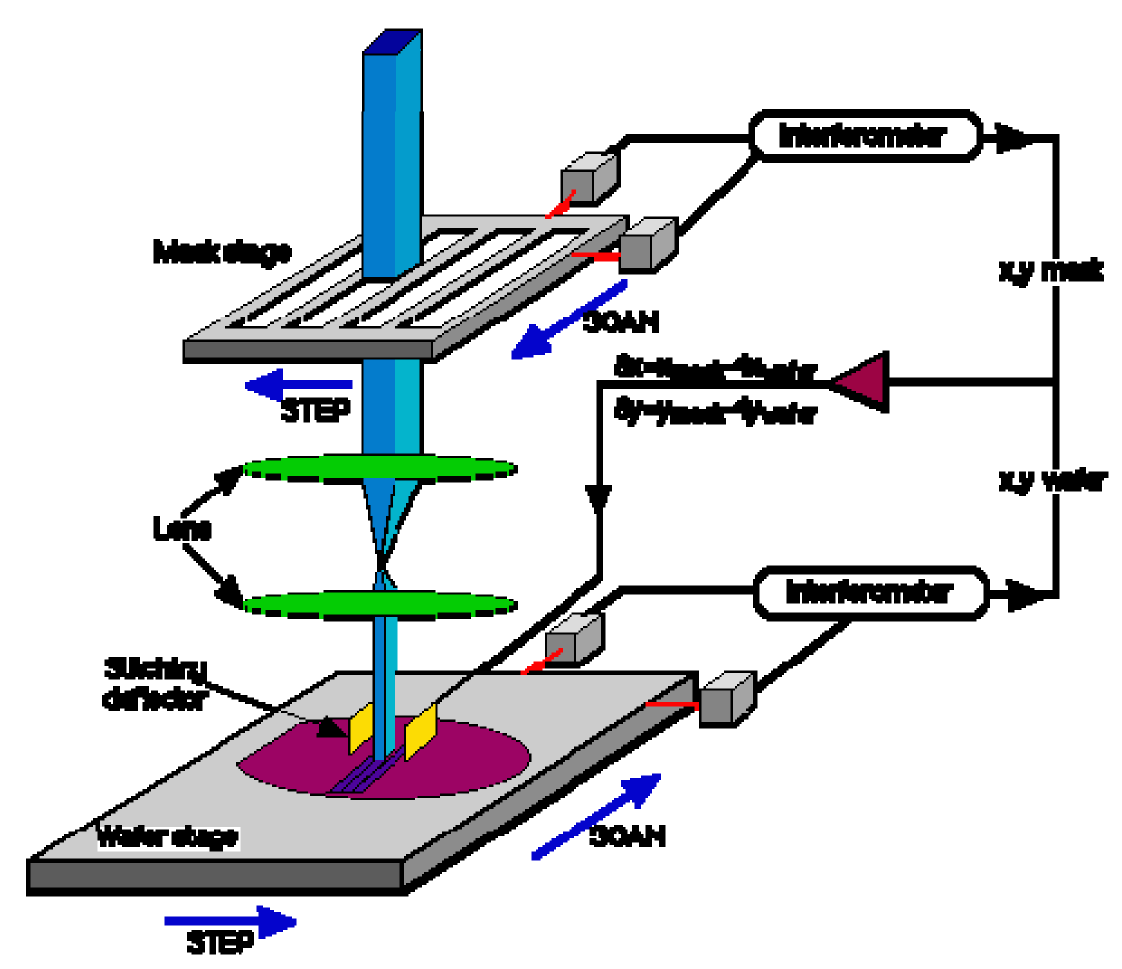
$3^*\sigma_{LWID+D2D} = 20\%^*L$

$\sigma^2_{LWID} = 50\%^* \sigma^2_{LWID+D2D}$

Variations diminish scaling benefits

Bowman et al, *JSSC*, Feb 2002 .

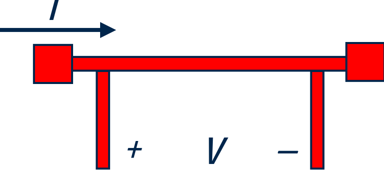
Step-and-Scan Lithography



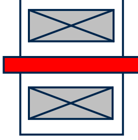
Lithography: Proximity Effects

- **Gate CD is a function of its neighborhood**

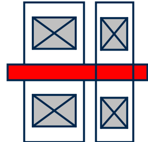
- **Test structures:**
  - Poly line resistance



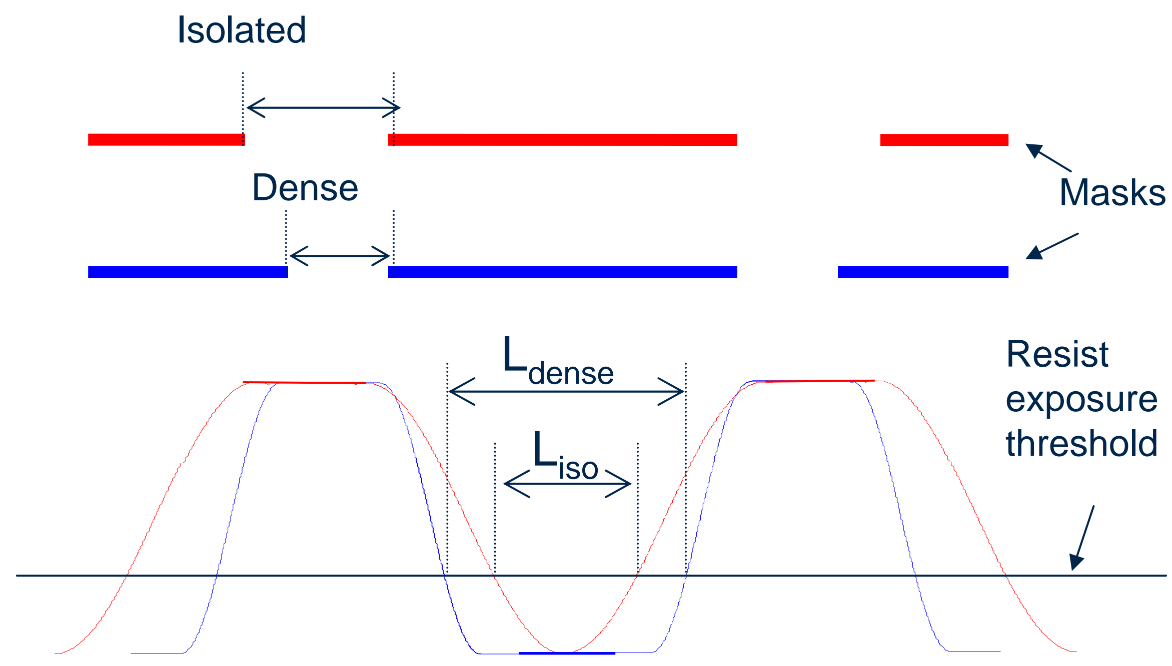
  - I-V characteristics of individual devices



  - Logic structures (ring oscillators)



Lithography: Density Effects

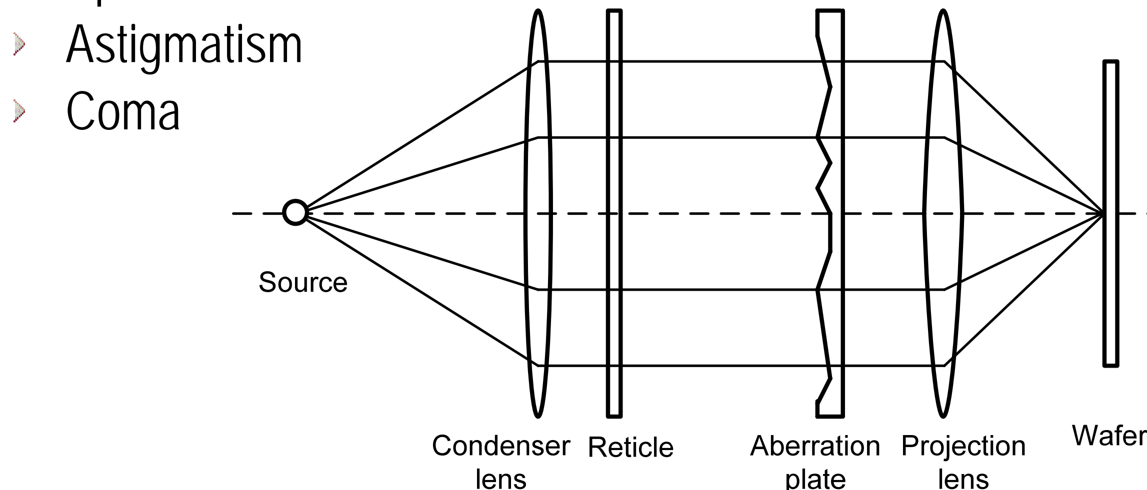


- Denser features: More accurate line width and less variation.
- Dense lines are wider than isolated lines.

Measurement structure: Poly lines with varying density

Lithography: Optics

- **Defocus**
- **Lens aberrations:**
  - Spherical aberrations
  - Astigmatism
  - Coma



- **Spherical aberrations - affect the reticle-level features**
  - Stepper dependent
- **Coma affects individual features**
  - Chip-location dependent

Lens Aberrations – Coma Effect

- Coma effect: optical aberration due to lens imperfection.
- Causes mirrored structures to display non equivalent properties
- Systematic shift between the 2 layouts

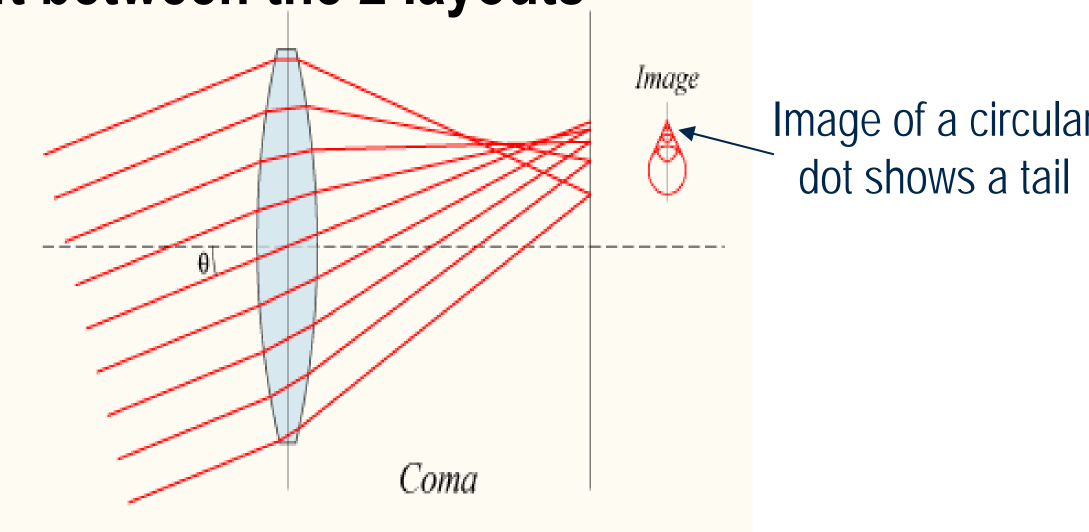
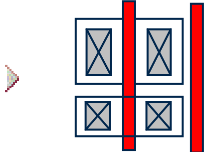
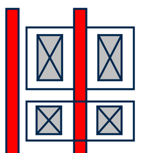


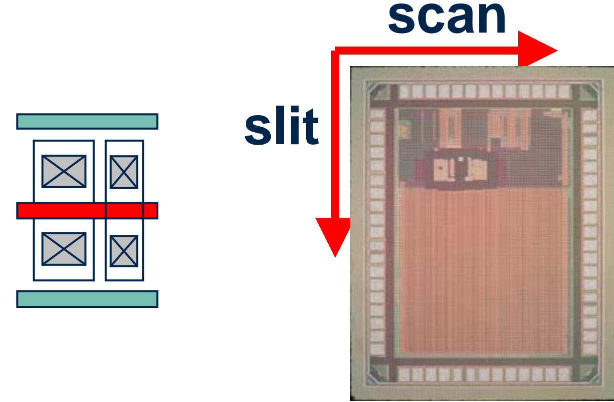
Image of a circular dot shows a tail

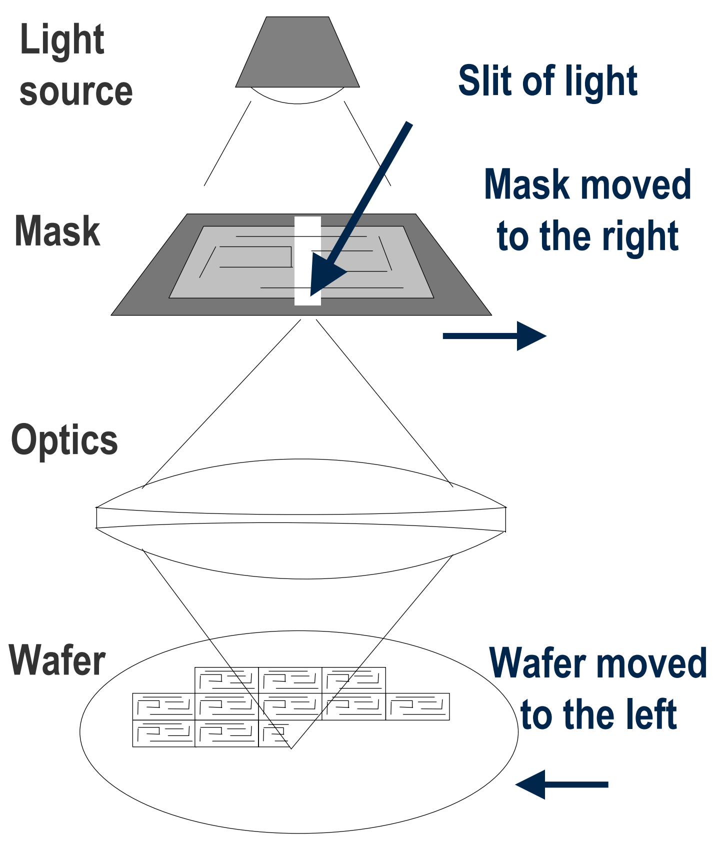
-  prints differently from 

Measurement structure: Non-symmetric poly lines

Step-and-Scan Lithography

- **Slit direction:**
  - Lens aberration in the slit
  - CD's more correlated
- **Scan direction:**
  - Dosage, scan speed and other fluctuations
  - CD's less correlated

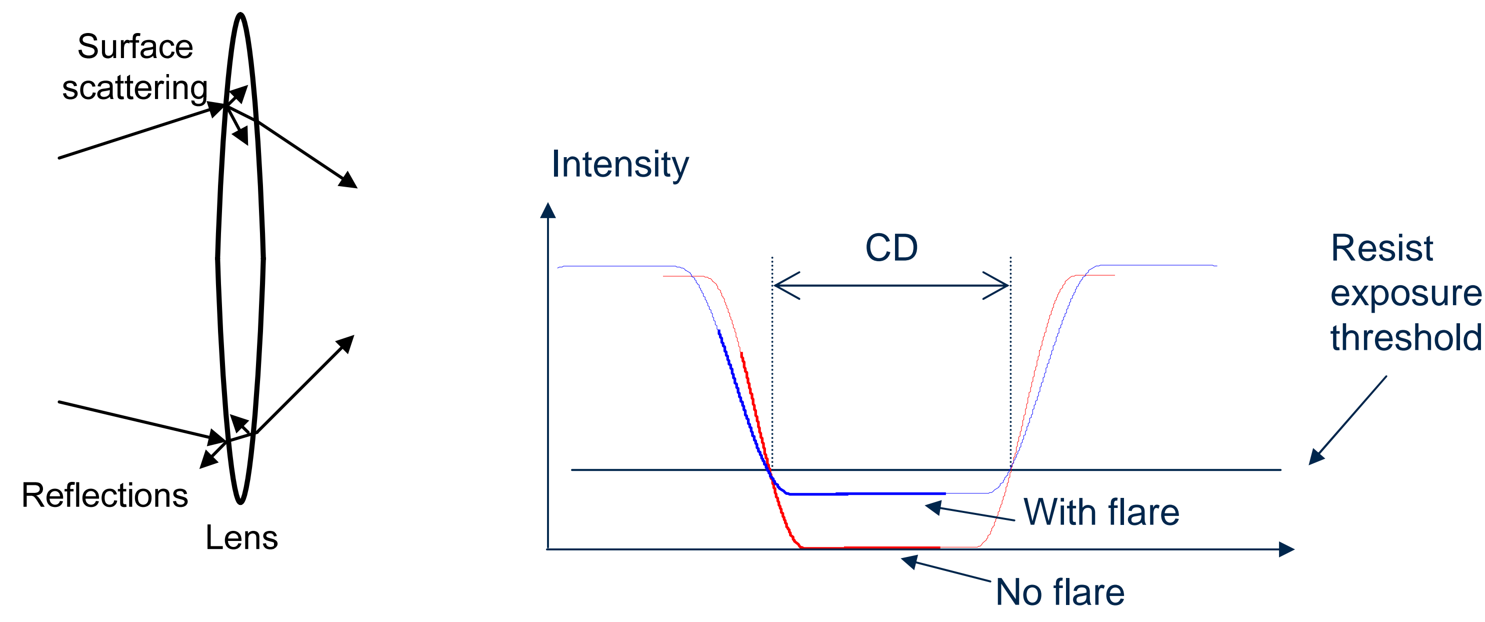




Measurement structure: Poly lines with varying orientation

Lithography: Flare

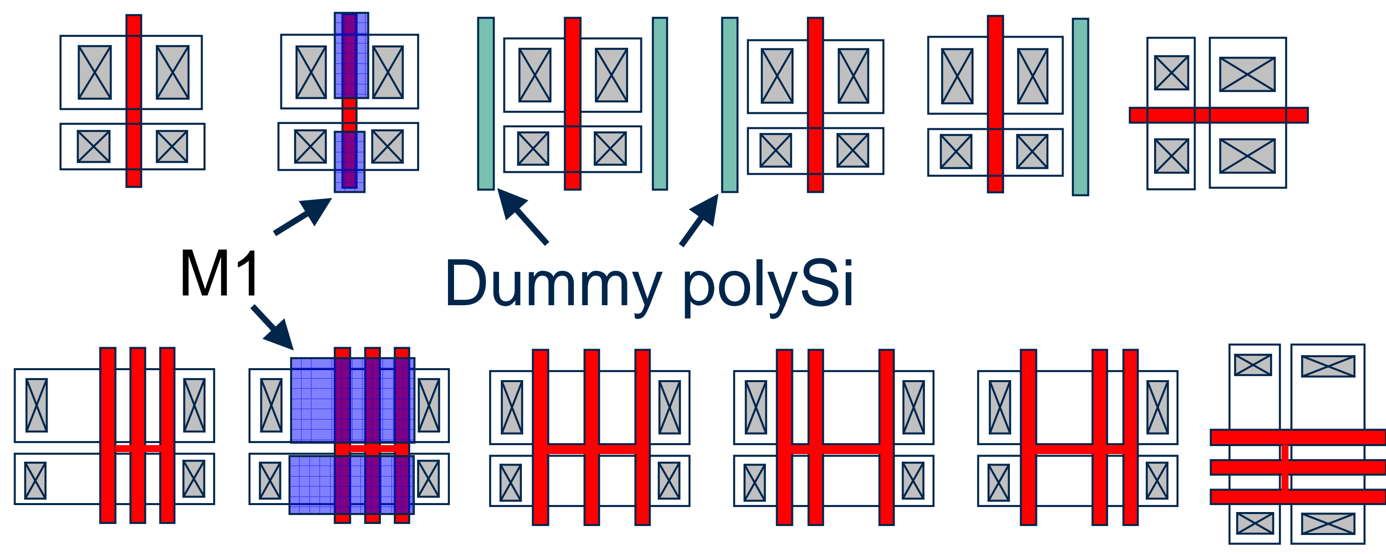
- **Light scattering and reflections**
- **More stray light under dark features in the mask**
  - Local flare depends on the density of chrome in the mask



Measurement structure: Uniform poly lines; varying spatial density

RO Arrays: 90nm CMOS Test-Chip

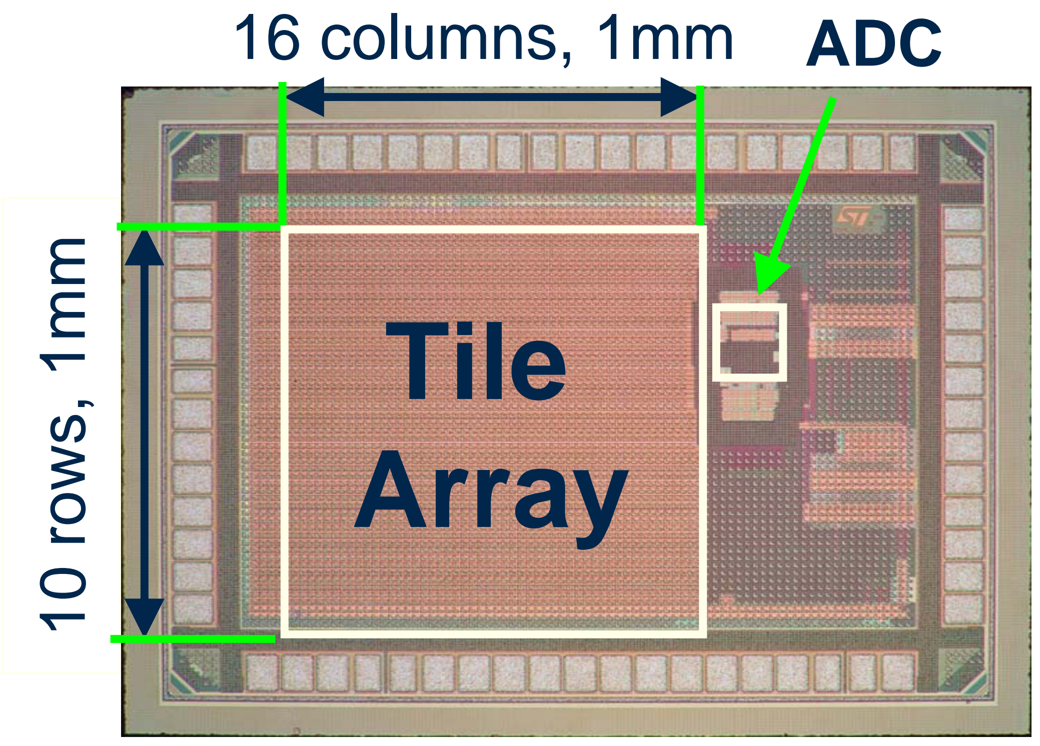
- **Layout effects: Density, symmetry, gate stacking, metal coverage**



12 layout configurations

L.T.Pang, *VLSI'06*

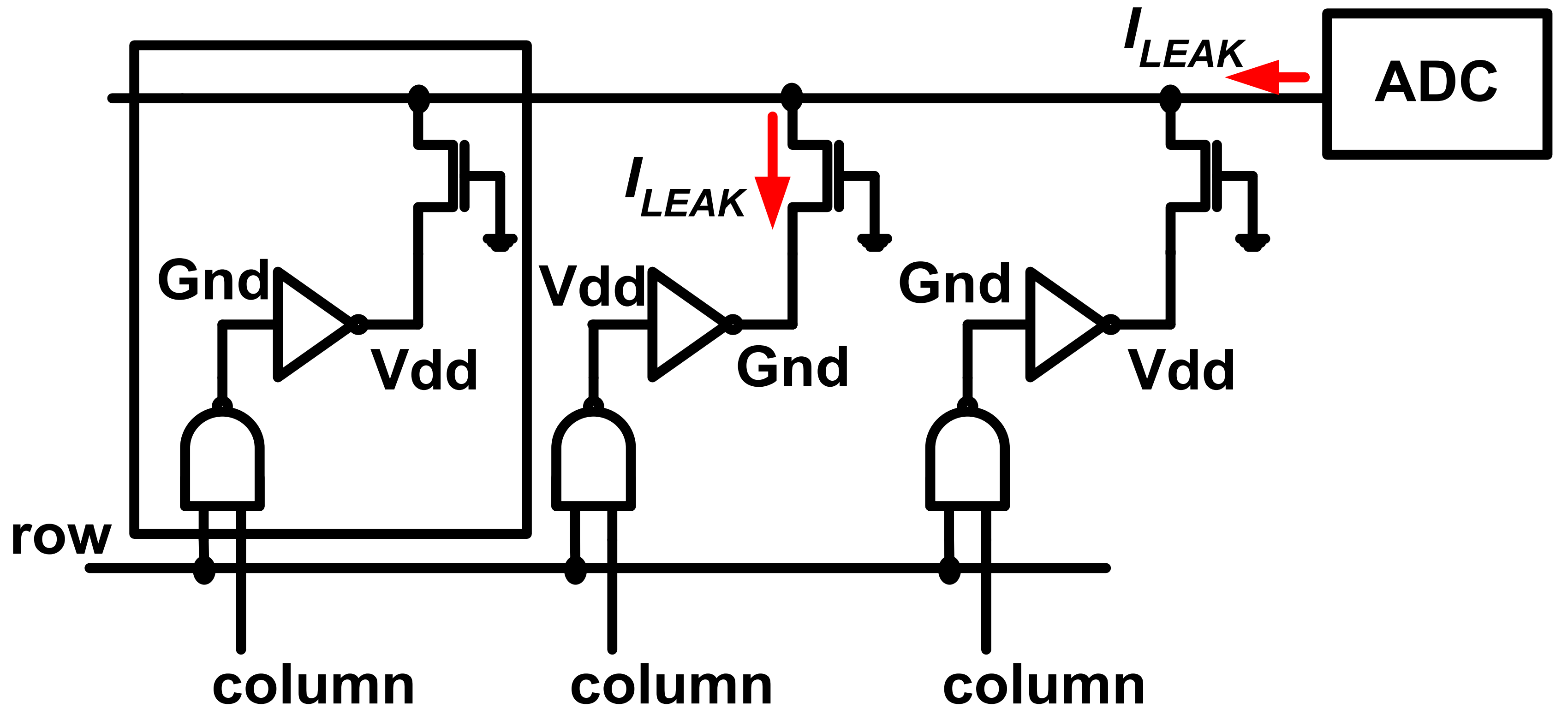
RO Arrays: 90nm CMOS Test-Chip



90nm CMOS test-chip die photo

L.T.Pang, *VLSI'06*

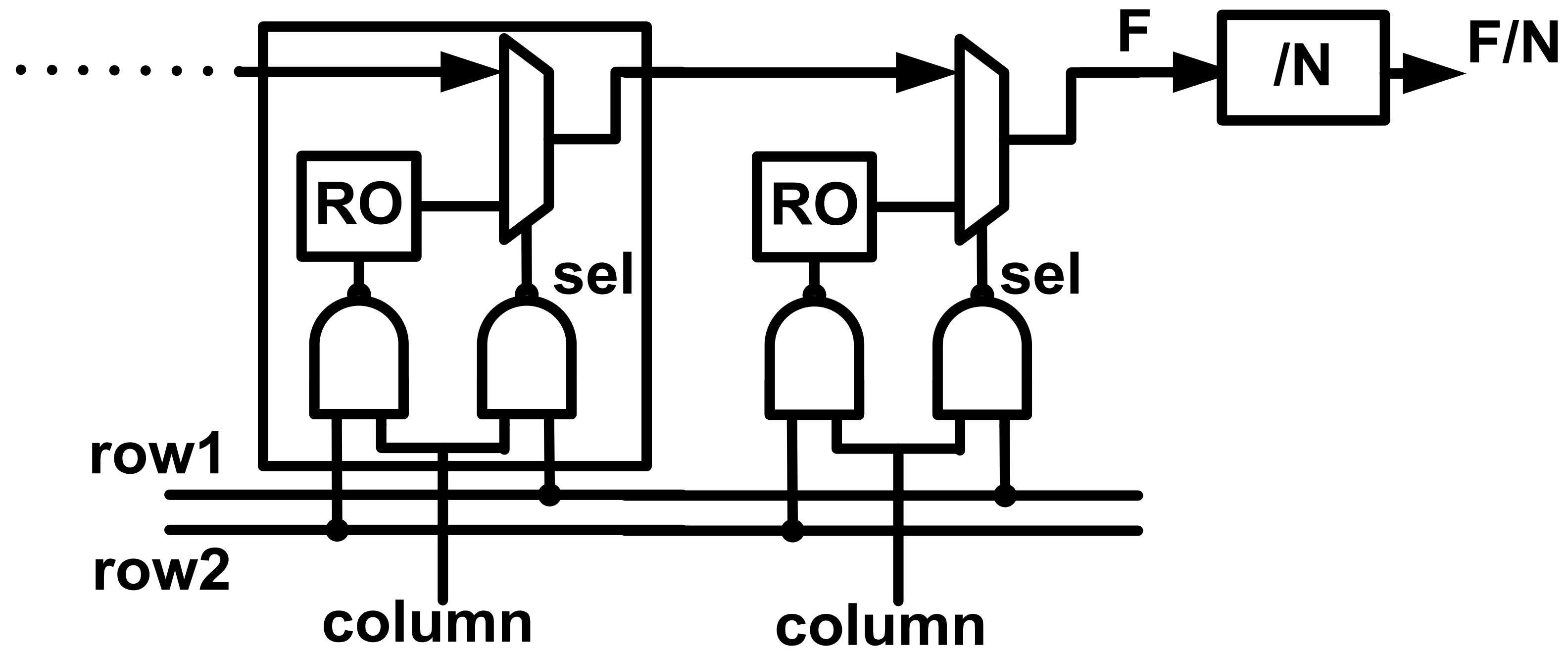
RO Arrays: Leakage Current(I_{LEAK})



- NMOS subthreshold leakage

L.T.Pang, *VLSI'06*

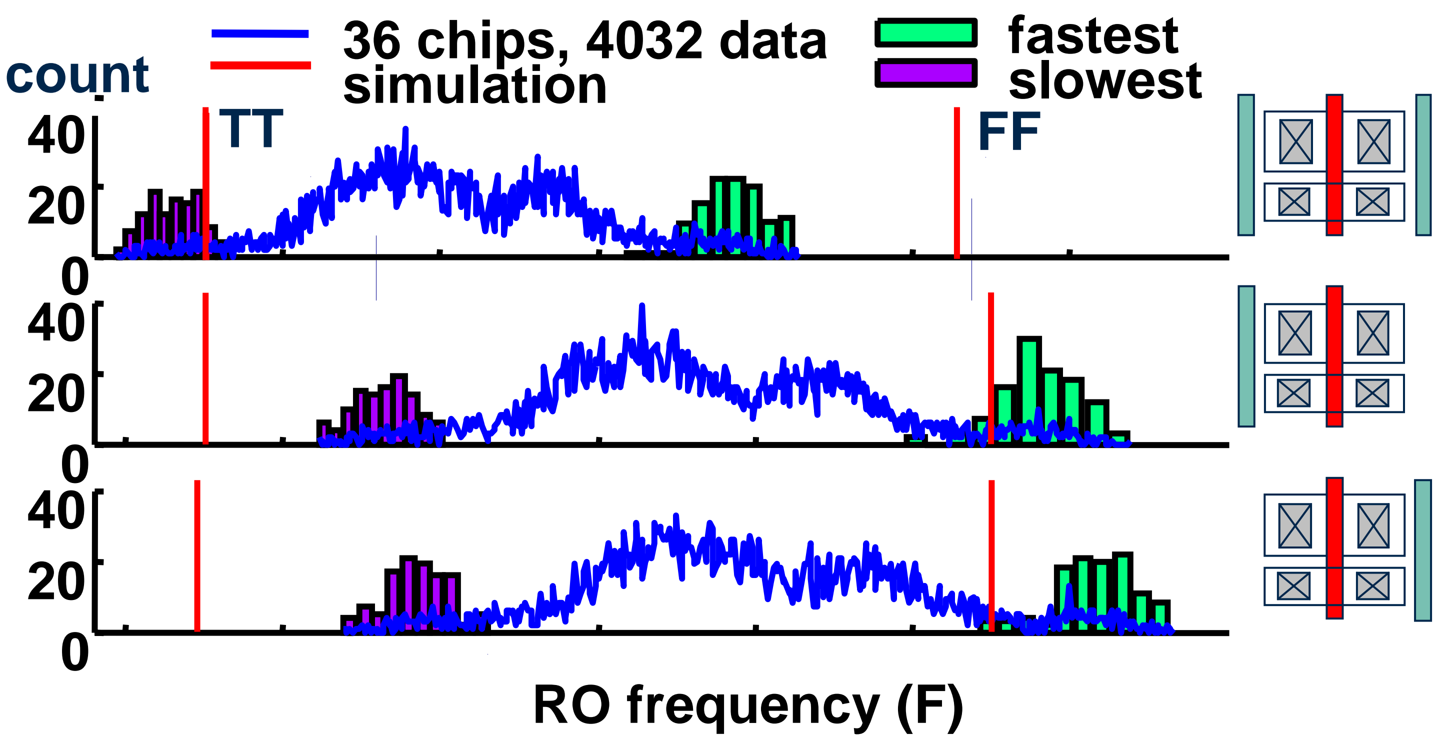
RO Arrays: Frequency(F)



Panganiban, M.Eng Thesis, MIT 2002.
Gonzalez-Valentin, M.Eng. Thesis, MIT 2002.

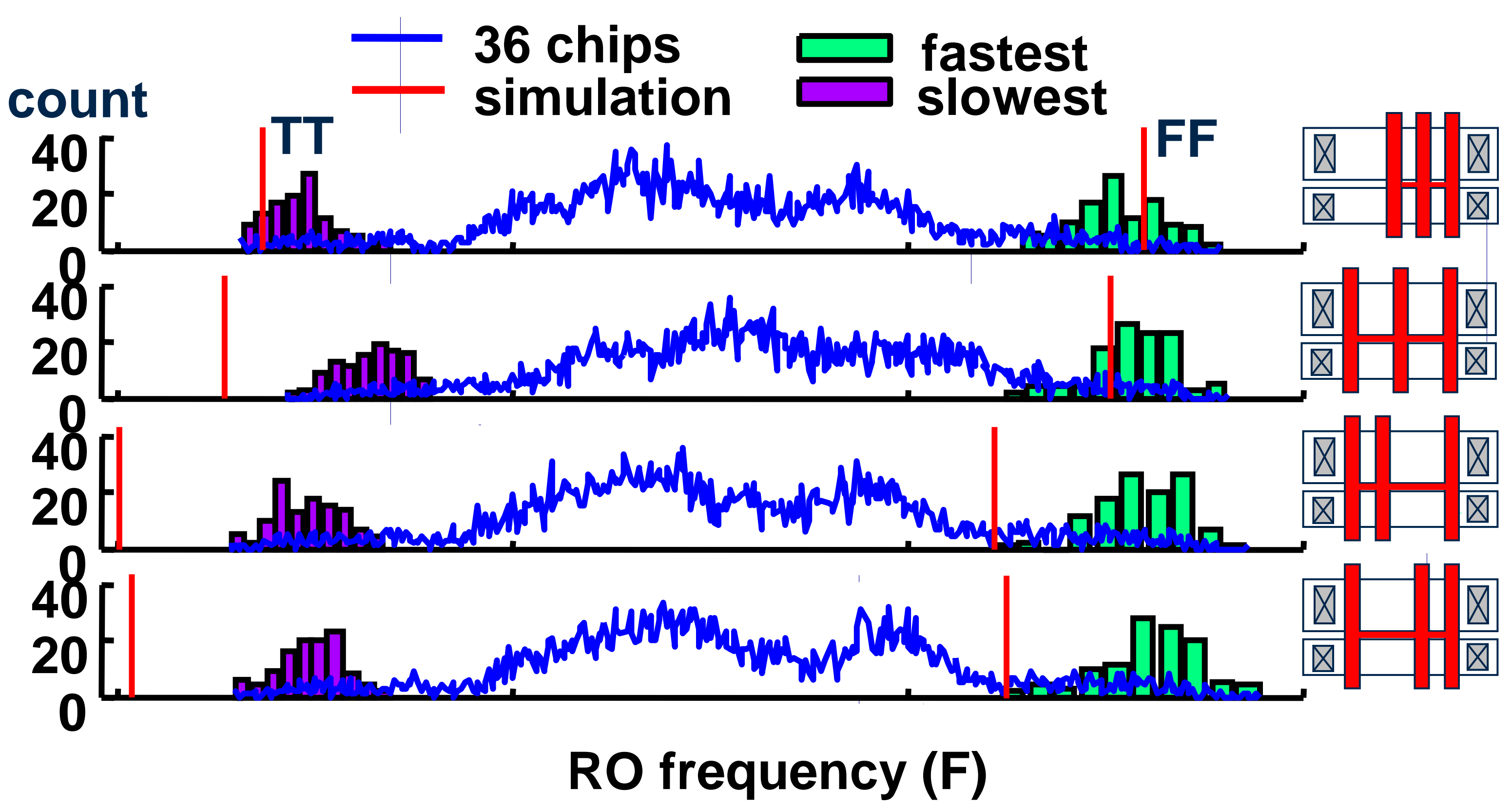
- RO enable and mux output select signals
- On-chip frequency divider

Results: Poly Density - Single Gates



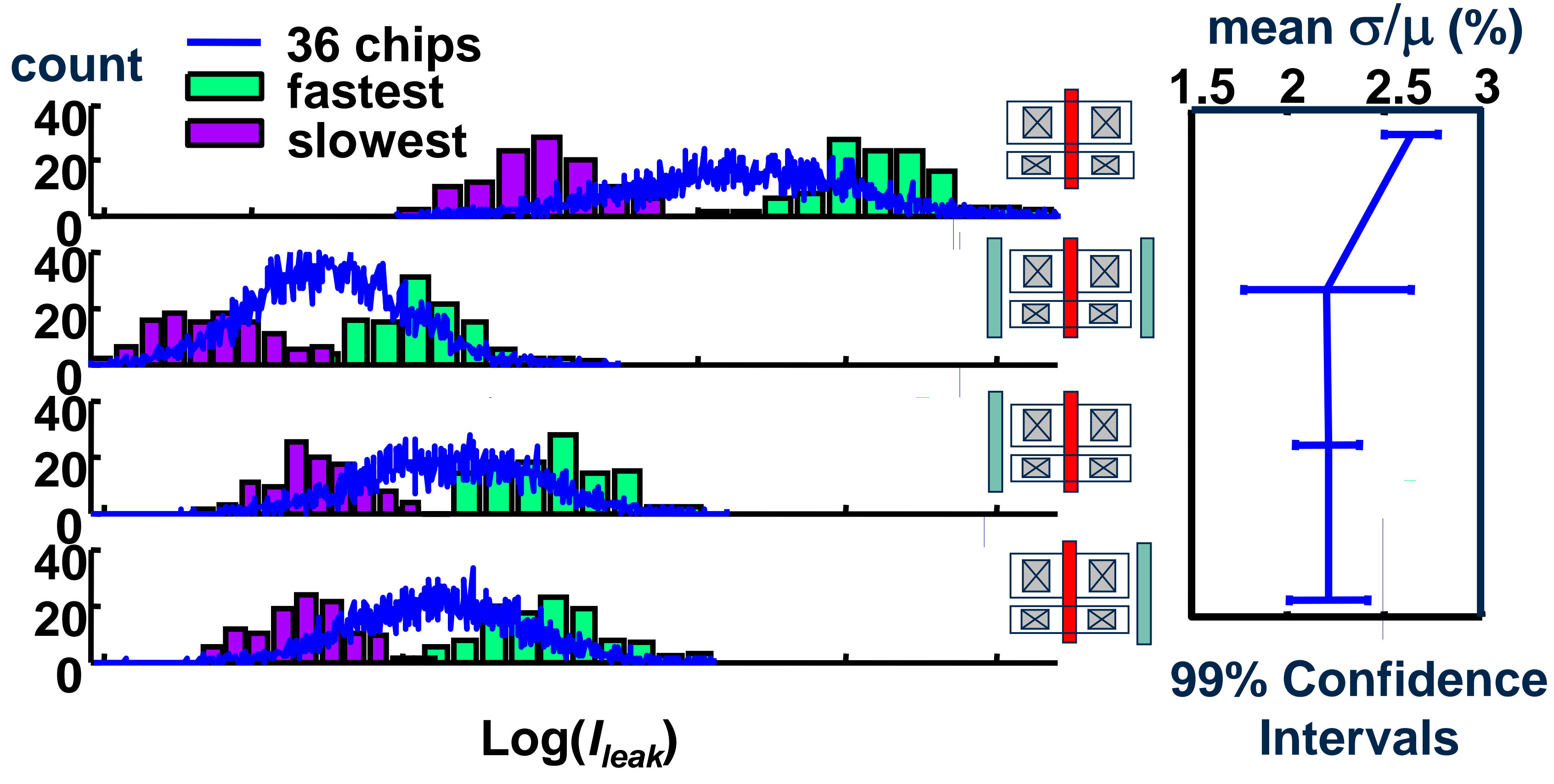
- Max ΔF between layouts ~ 10%
- Within-die $3\sigma/\mu$ ~3%, weak dependency on density (<1%)

Results: Poly Density- Stacked Gates



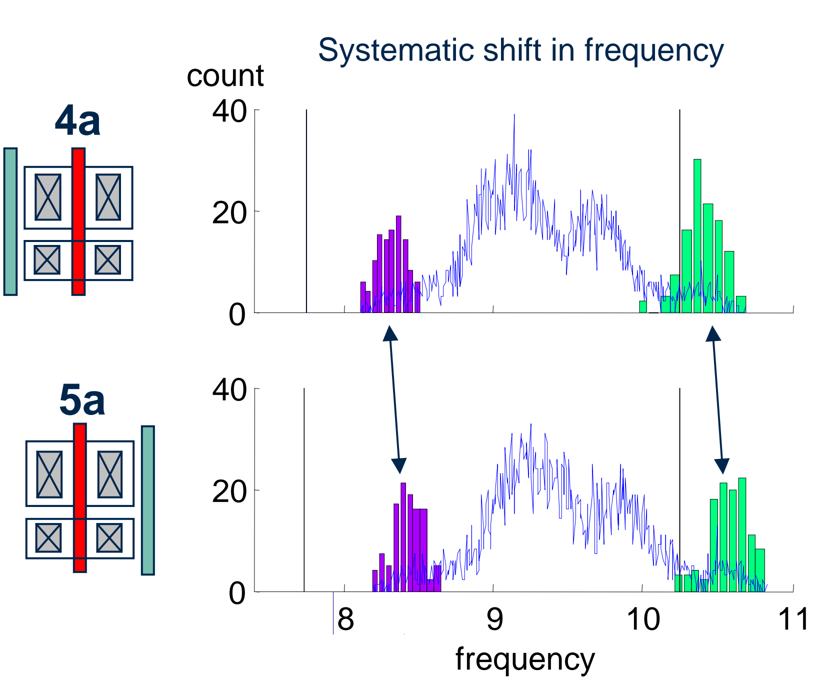
- Weaker effects, max ΔF between layouts ~ 3%
- Within-die $3\sigma/\mu$ ~3%, no dependency on stacking

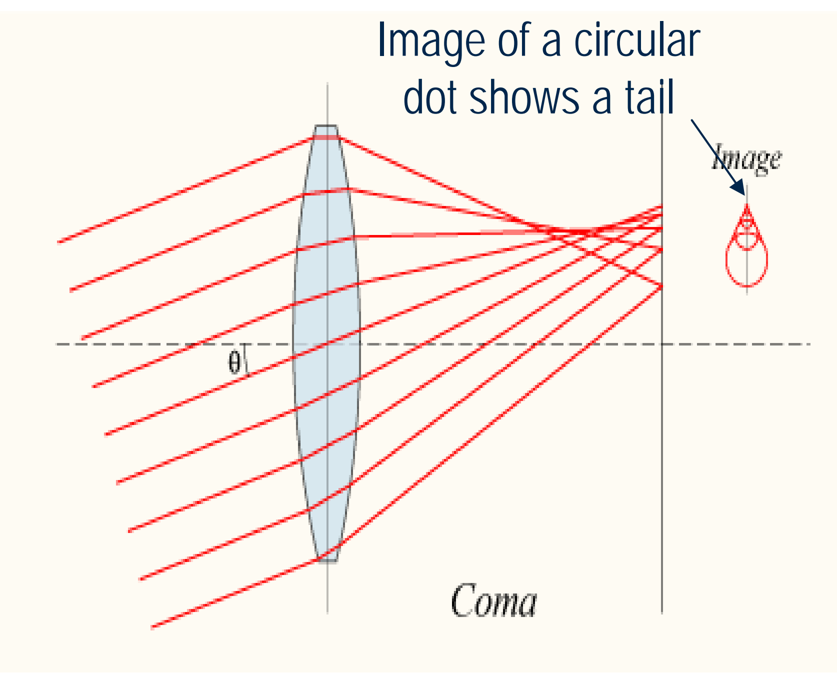
Results: Poly Density - Leakage Current



- Single gates: low poly density → faster and leakier
- Denser layout → smaller variation (σ/μ)

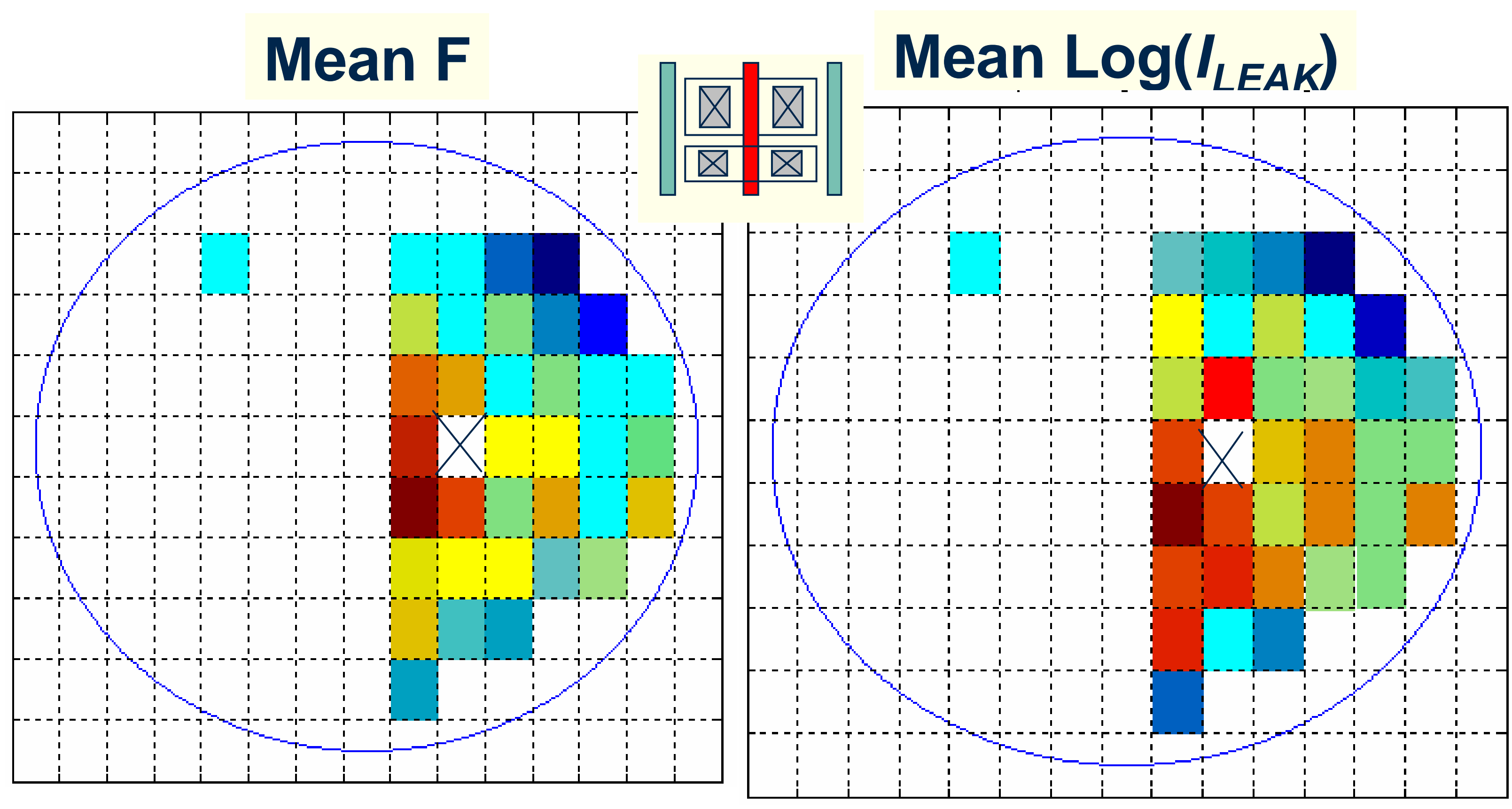
Coma Effect – Lens Aberrations





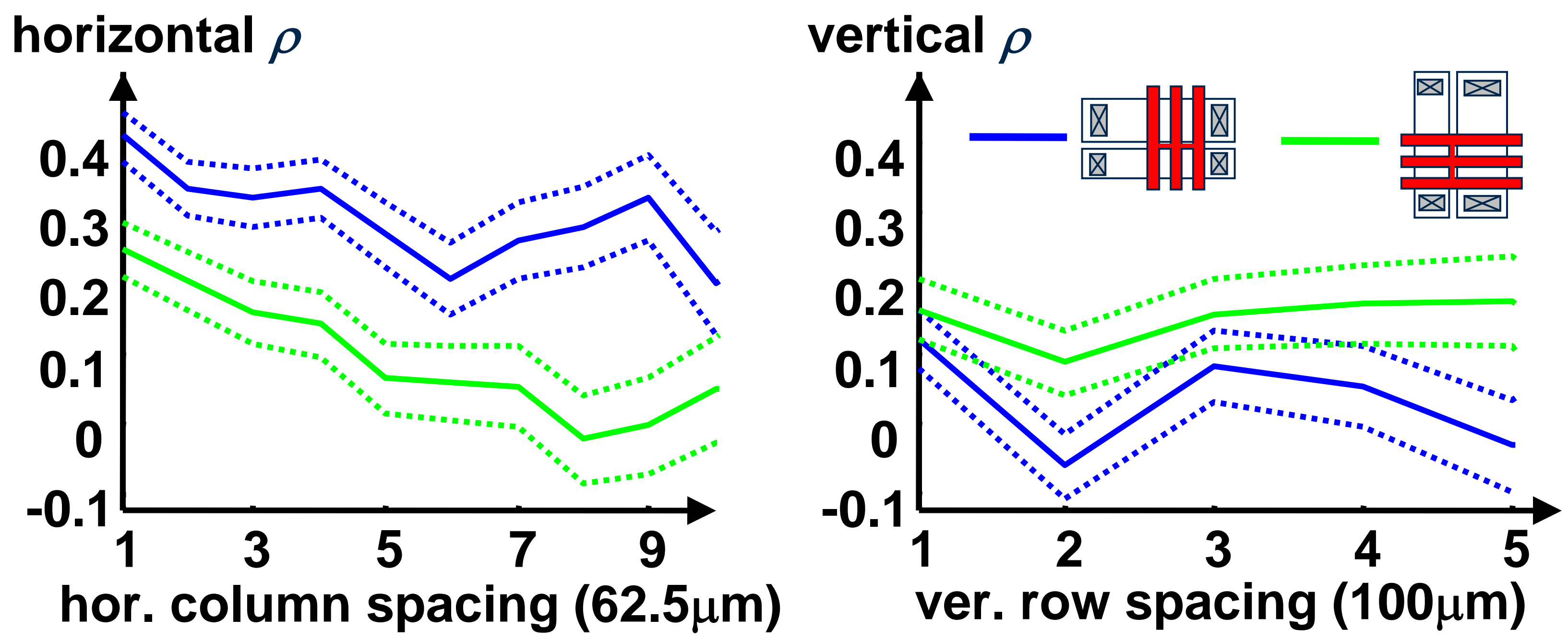
- **Measurable coma effect (~1%)**

Results: Wafer Map



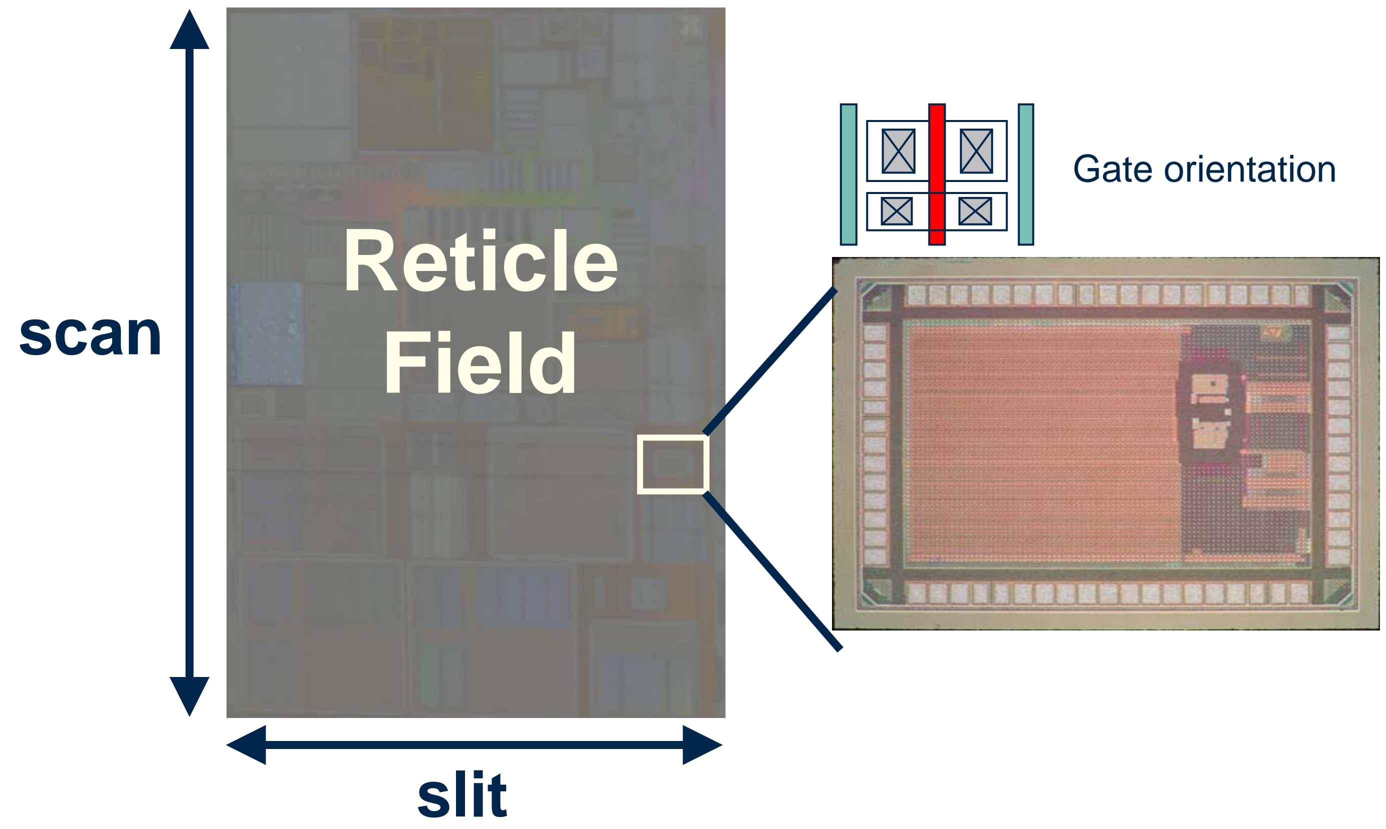
- Variation of mean F: $3\sigma/\mu$ die-to-die ~ 15%
- Radial pattern: faster and leakier at wafer center

Results: Spatial Correlation



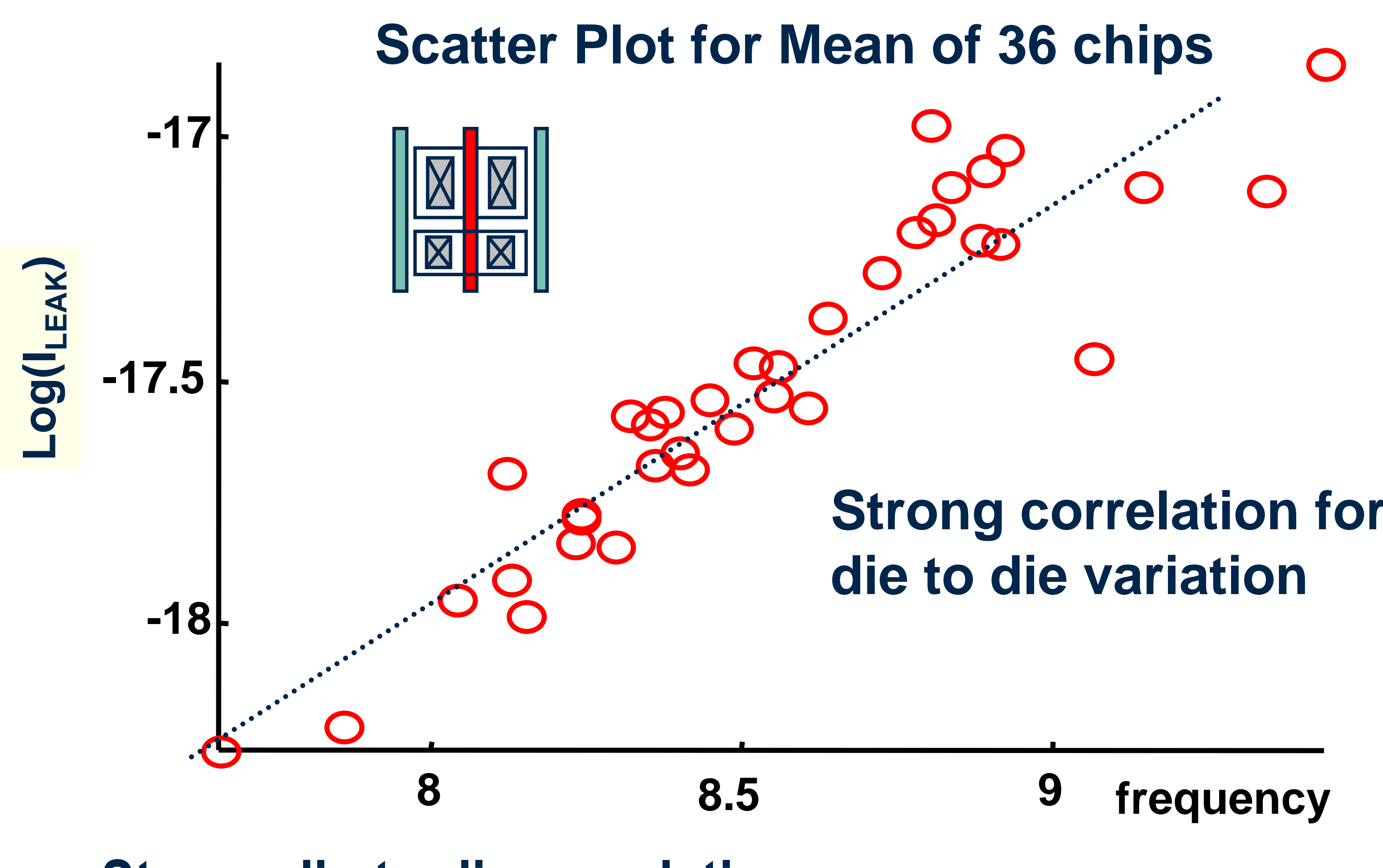
- $3\sigma/\mu$ within-die variation ~ 4%
- ρ depends on gate orientation and direction of spacing
- ROs with rotated gates have lower variation

Results: Step and Scan Lithography



- **Slit direction more correlated**

Results: D2D Correlation



- Strong die-to-die correlation

Conclusions: What to Do?

Layout Extraction	Consider proximity effects
Circuit Layout	L2L > 10%. Regular layouts
Circuit Macros	D2D > 15%. On-chip compensation circuits
Circuit Simulation	Incorporate systematic vs. random; correlation
Floor Planning	WID < 4%. Exploit spatial correlation in different directions

Acknowledgments

- Funding: FCRP C2S2
- STMicroelectronics donated chip fabrication