

A large, circular, blue-tinted image of a microchip die, showing a grid of circuitry, is positioned on the right side of the slide. The background is dark blue with a faint, larger-scale grid pattern.

PSoC As New Technology Driver

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CMOS Emerging Technologies, Whistler, July 2007

P E R F O R M

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013	Driver
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	35	32	
Mask cost (\$m) from publicly available data	1.5	2.2	3.0	4.5	6.0	9.0	12.0	18.0	24.0	SOC
% Vdd Variability % variability seen at on-chip circuits	10%	10%	10%	10%	10%	10%	10%	10%	10%	SOC
% Vth variability Doping Variability impact on VTH	24%	29%	31%	35%	40%	40%	40%	58%	58%	SOC
% Vth variability Includes all sources	26%	29%	33%	37%	42%	42%	42%	58%	58%	SOC
% CD variability CD for now; might add doping later	10%	10%	10%	10%	10%	10%	10%	10%	10%	SOC
% circuit performance variability circuit comprising gates and wires	41%	42%	45%	46%	49%	50%	53%	54%	57%	SOC
% circuit power variability circuit comprising gates and wires	55%	55%	56%	57%	57%	58%	58%	59%	59%	SOC

Category

Layout complexity

Power mgmt

Models

Layout sensitivity

Models

Power mgmt

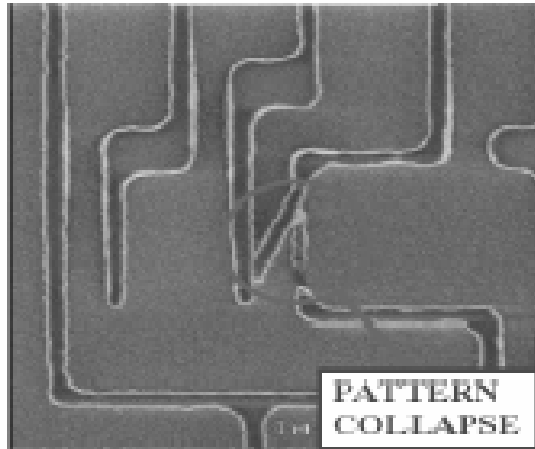
Table 1. Design for Manufacturability: Near-Term Years

PSoC = Selling solutions not Silicon by acres
Layout optimization = key process development and cost saving factor

Direction	Issue	Digital	PSoC / Analog
Horizontal	Line CD	Fixed pitch 1:1.5 Scatter Bars Double pattern	Large footprint Reduced OPC Controlled environment
	Corner and gap OPC reduction	Double pattern NIL or EUV	Correct by Construction (CBC) Layout
Vertical	Pattern density ILD thickness	Waffling	Smart waffling with extraction
	Pattern Impact on circuit behavior	Negligible	Extraction and simulation required

Horizontal CD Control: Digital Too expensive for PSoC

This catastrophic fail ...
Defocused wafer



Lucas et al. Proc. SPIE vol. 5756 (2005) p.85

has been traced to a missing assist
RET'd design



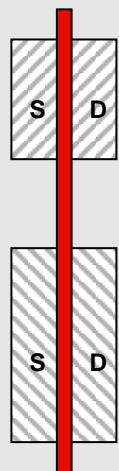
Needed: Design rules for analog/RF layout
to create CBC cells

The CBC => DfM Rule of 10

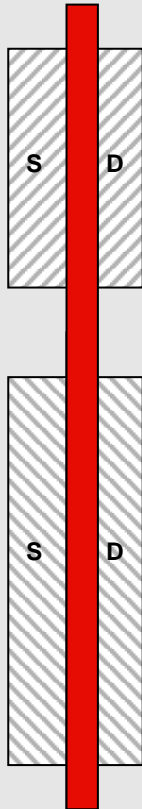
Level of completion	Cost to find & repair defect
Std cell	X
Block level	10 X
Die level	100 X
Test	1,000 X
Customer	10,000 X

Line CD Control vs. Footprint Dummy Structures

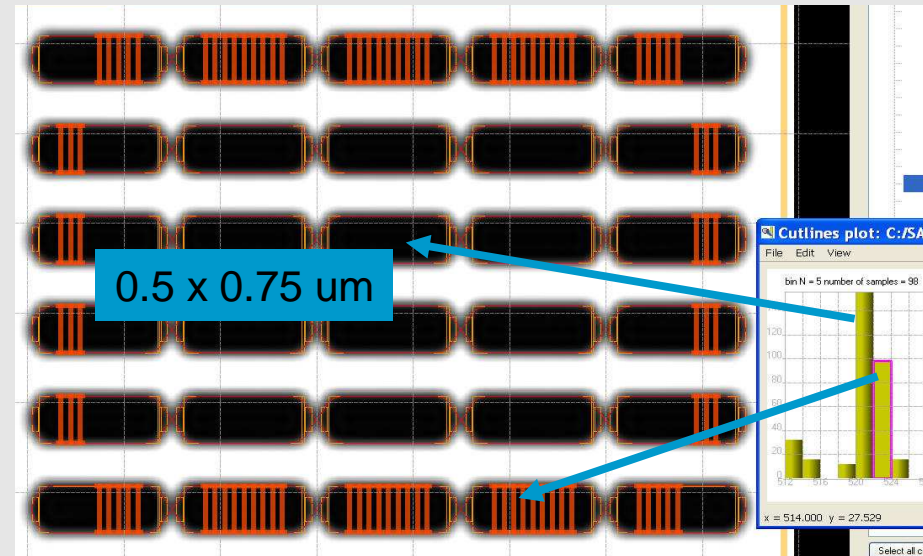
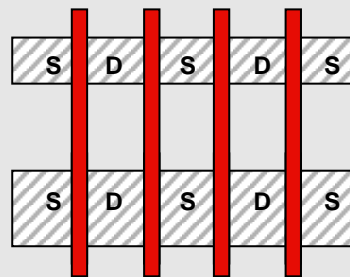
100%



230%



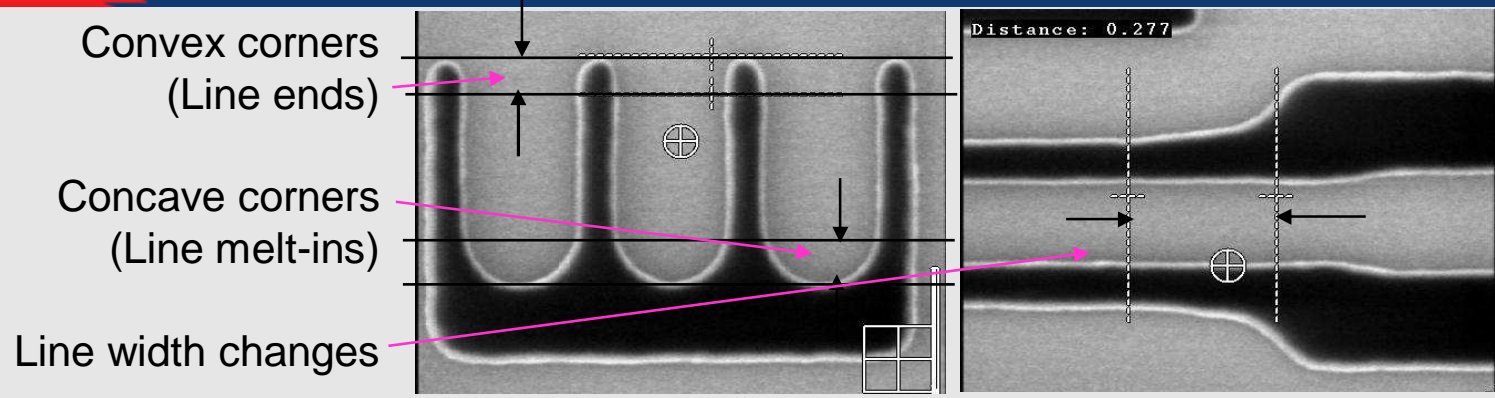
175%



- Footprint impact: 5% larger rules => 10% larger footprint
 - Would the yield increase?
 - How to prove it (5% increase requires 1 split lot, 1% - up to 25 split lots)
 - Compromise: parasitics vs. endcaps
- Rules:
 - Screening distance = $4 \lambda / \text{NA} = 4 * 193 / 0.8$ 1 μm
 - One dummy row/col sufficient for most applications
 - Min CD (analog) / Min CD(technology) 4 x

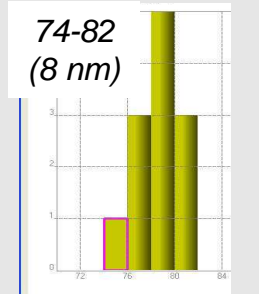
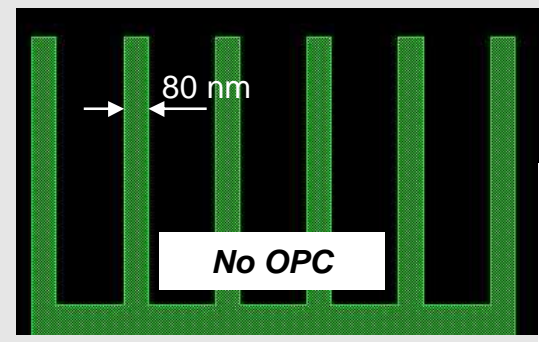


Line Discontinuity Mitigation: OPC

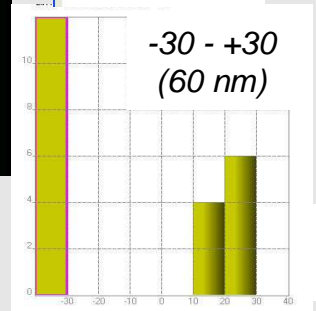
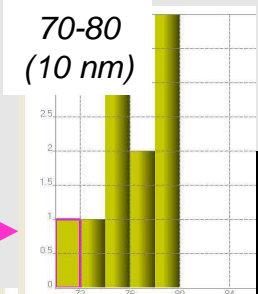


Rule aggressiveness depends on the redesign/OPC tradeoff

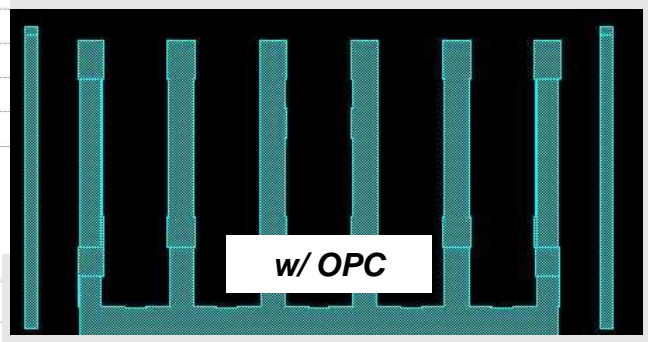
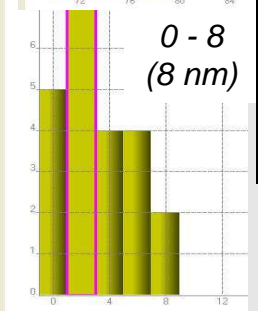
$Resolution = k1 * \lambda / NA$
 Currently pursued $k1$ - reduce to < 0.30 w/OPC
 Stable process window for $k1$ ~ 0.8 (~3x)
 High quality layout = no OPC



Line CD



Line end pullback





Device/MB DfM Simulation Flow

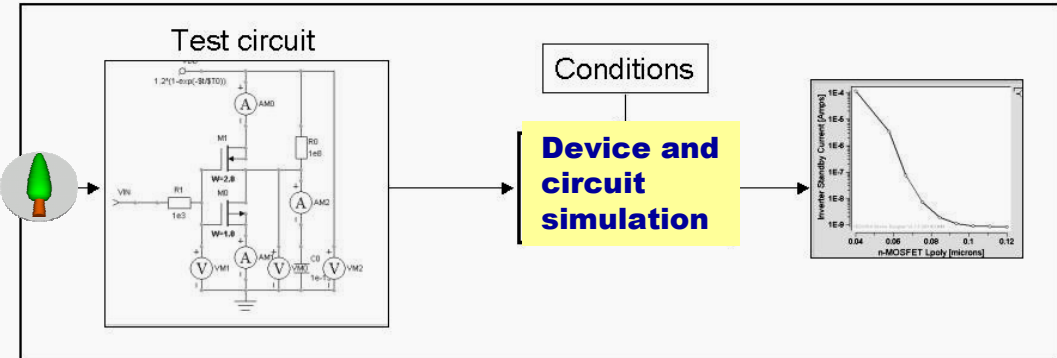
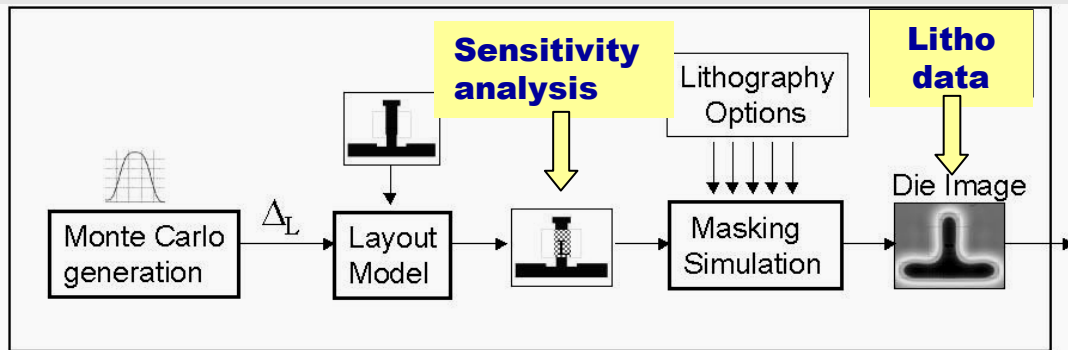
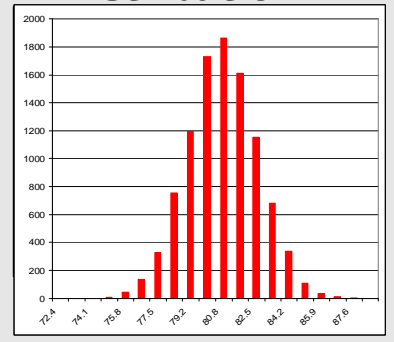
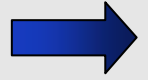


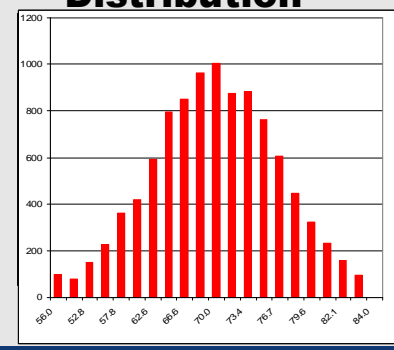
Photo Mask CD Distribution



ICWB
NA, σ,
RET



Wafer CD Distribution



SDD



Device Parameters

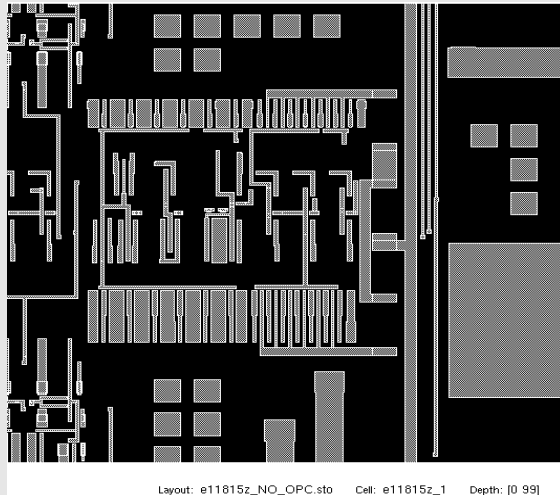
- Device Parametric Yield
- Circuit Speed Distribution



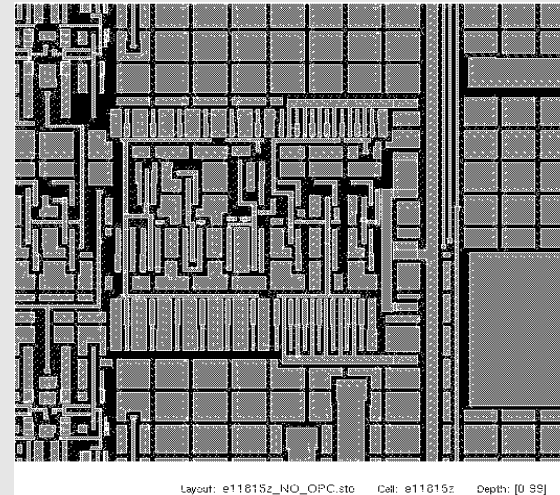
Vertical CD Control Planarization

- Impacts - **critical for PSoC** :
 - isolation => voltage tolerance
 - contact/via resistance => frequency response
- Answer: mask pattern density controlled by dummy features
 - Physical layers: isolation, poly, metals
 - Approaches:
 - geometric = fixed target oPD (“Oxide”)
 - intelligent = flexible target oPD (“Oxide”)
- Extraction issues
 - **Manual placement**
 - time consuming, random, iterative: no visibility at design block on target die PD
 - key advantage: fill pattern can be extracted electrically
 - **Automated placement**
 - simple: add dummies in empty locations not protected by keepouts
 - drawback: not acceptable for sensitive signal paths
 - not electrically extractable at die level

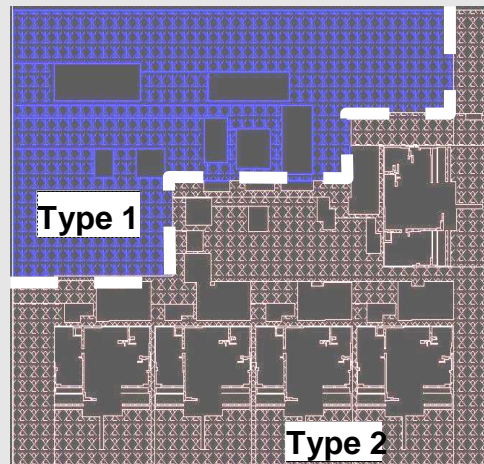
Geometric Waffling Options



Sparse



Dense



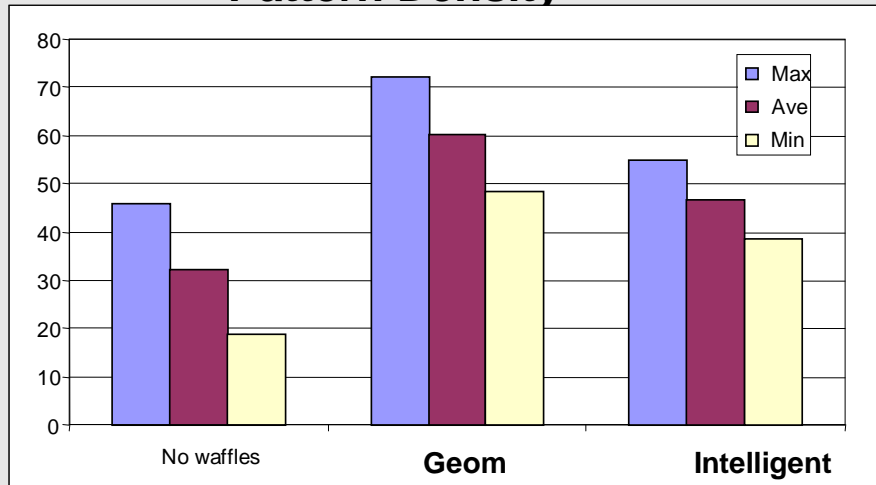
**Sparse and dense waffling:
nominal oxide pattern density
(100%)**

**Dense waffling required in the
vicinity of exclusion areas**

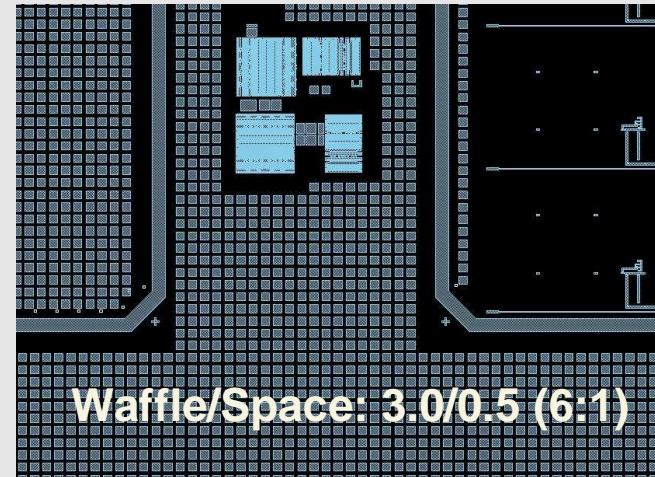
**Preferred methodology for multi-IP
testchips (PSoC IP)**

Waffling vs. Planarity

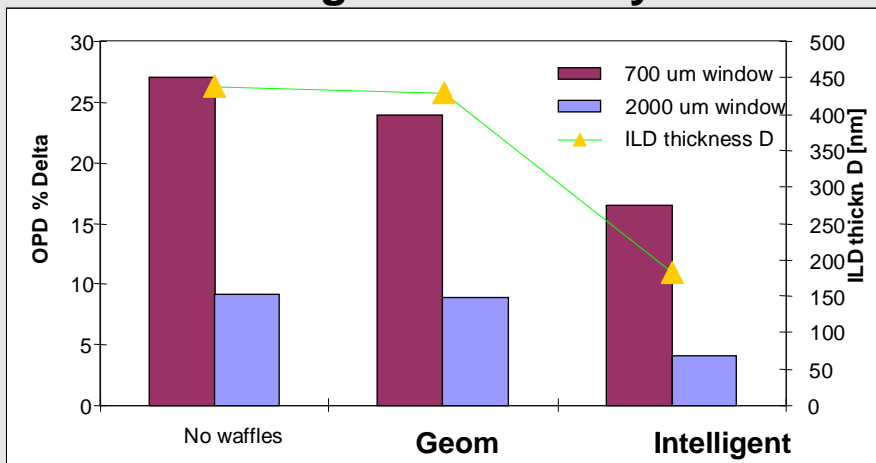
Pattern Density



Geometric waffles



PD Range vs. Planarity



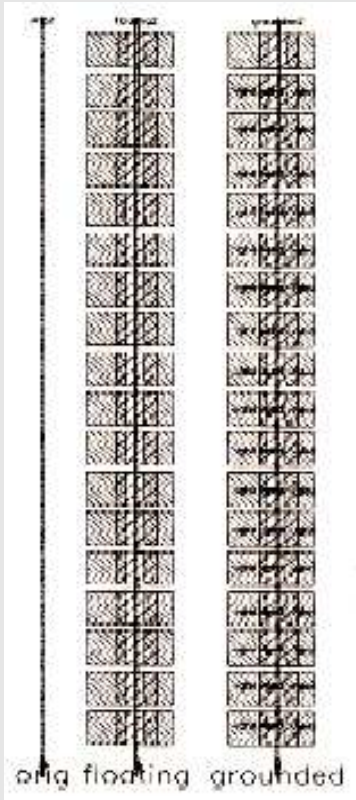
Intelligent waffles



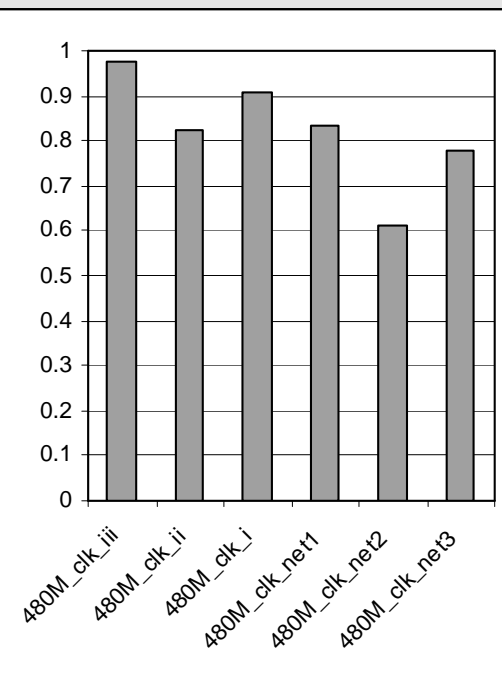
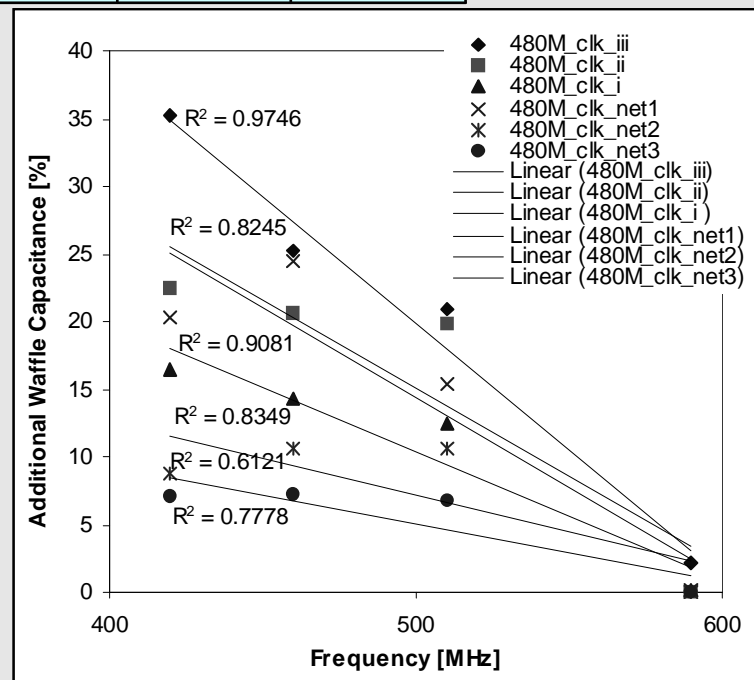
What this means: Smart waffling reduces PD and ILD range by 50% and minimizes extraction impact. However, meeting PD rules for multiple PSoC IP's on one mask may be impossible.



Waffle Capacitance vs. Frequency Response



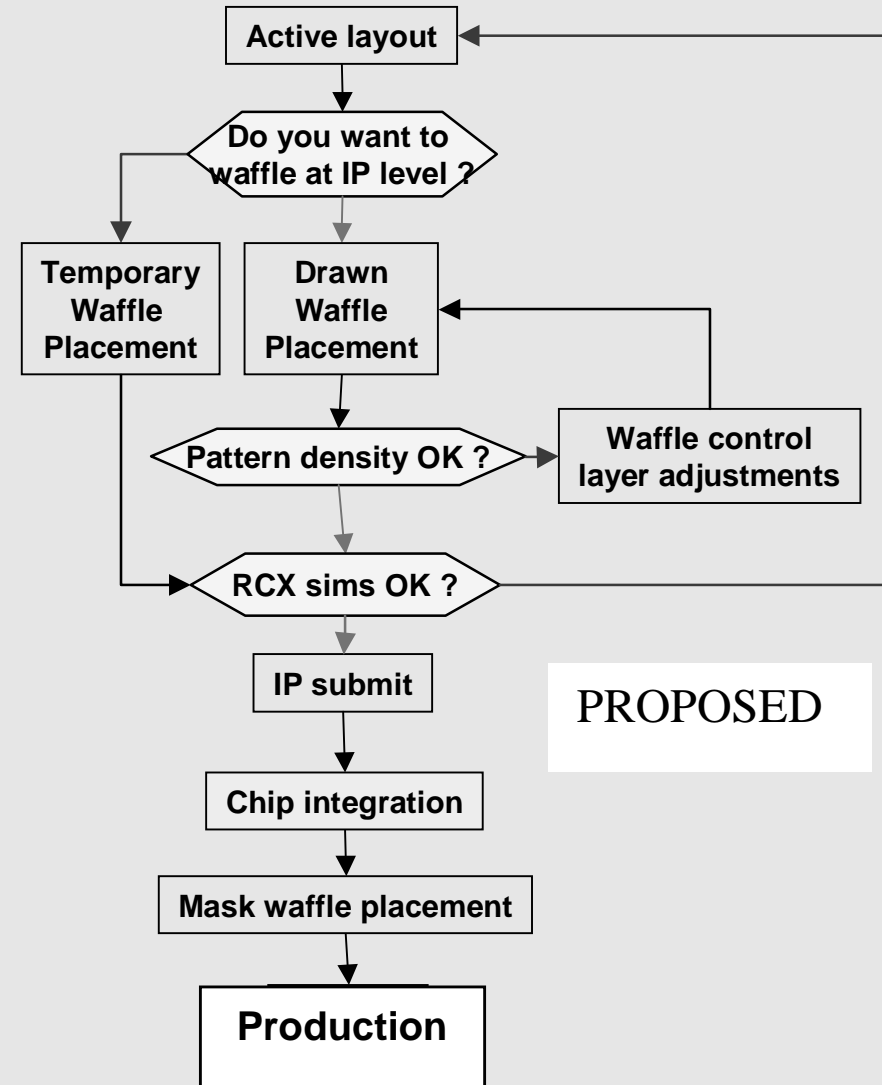
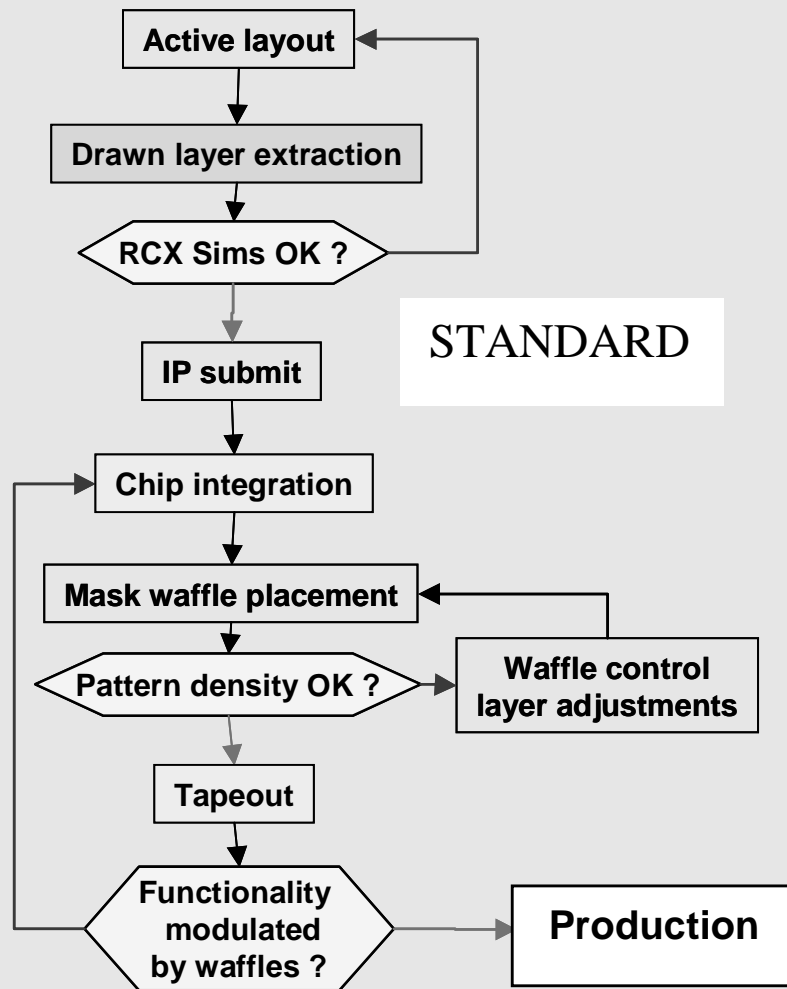
Non-LVS (fF)		
No waffles	Floating	Grounded
4.96	10.46	10.46
LVS with or w/o extracted floats (fF)		
No waffles	Floating	Grounded
5.33	10.51	10.51



What this means:

Capacitance of random waffles degrades frequency, with correlation >0.6 (nominal fast USB frequency = 480MHz)

Dummy Fill Extraction Flow



- **Variability reduction critical for PSoC Technology**
- **CD control critical for die variability reduction:**
 - **Horizontal CD control**
 - **Layout footprint**
 - **OPC**
 - **Vertical CD control**
 - **Pattern density**
 - **Geometric fill**
 - **Smart fill**
 - **Electrical extraction and simulation of variability required:**
 - **Horizontal – point tools exist, need flow integration**
 - **Vertical – no tools exist**
- **Correct by construction layout**
 - **Significantly increased footprint**
 - **Improved CD control**
 - **Increased parasitics**
 - **Needs tools to optimize**
- **If all else fails, simulate**