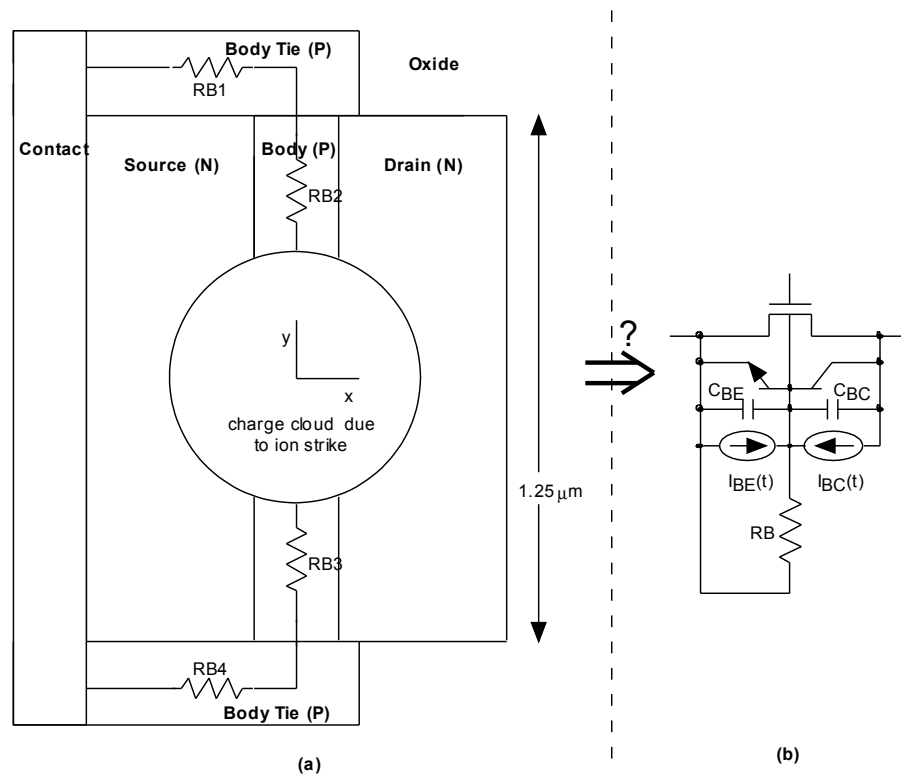

Models for Radiation Effects in SOI (and bulk CMOS)

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- Introduction
- Two-dimensional analysis of charge distribution
- One-dimensional analysis of charge distribution
- SPICE model for an ion strike
- SPICE simulation of threshold linear energy transfers (LET's) of various circuits
 - Comparison to experiment
- Application of the model to bulk CMOS
- Conclusions

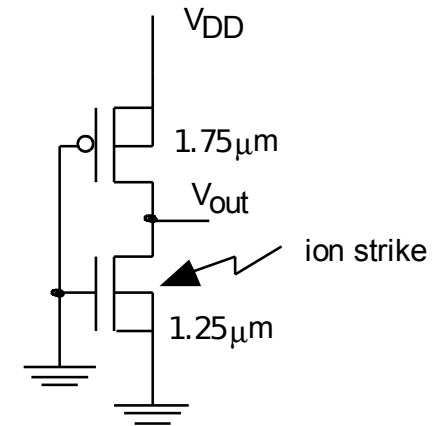
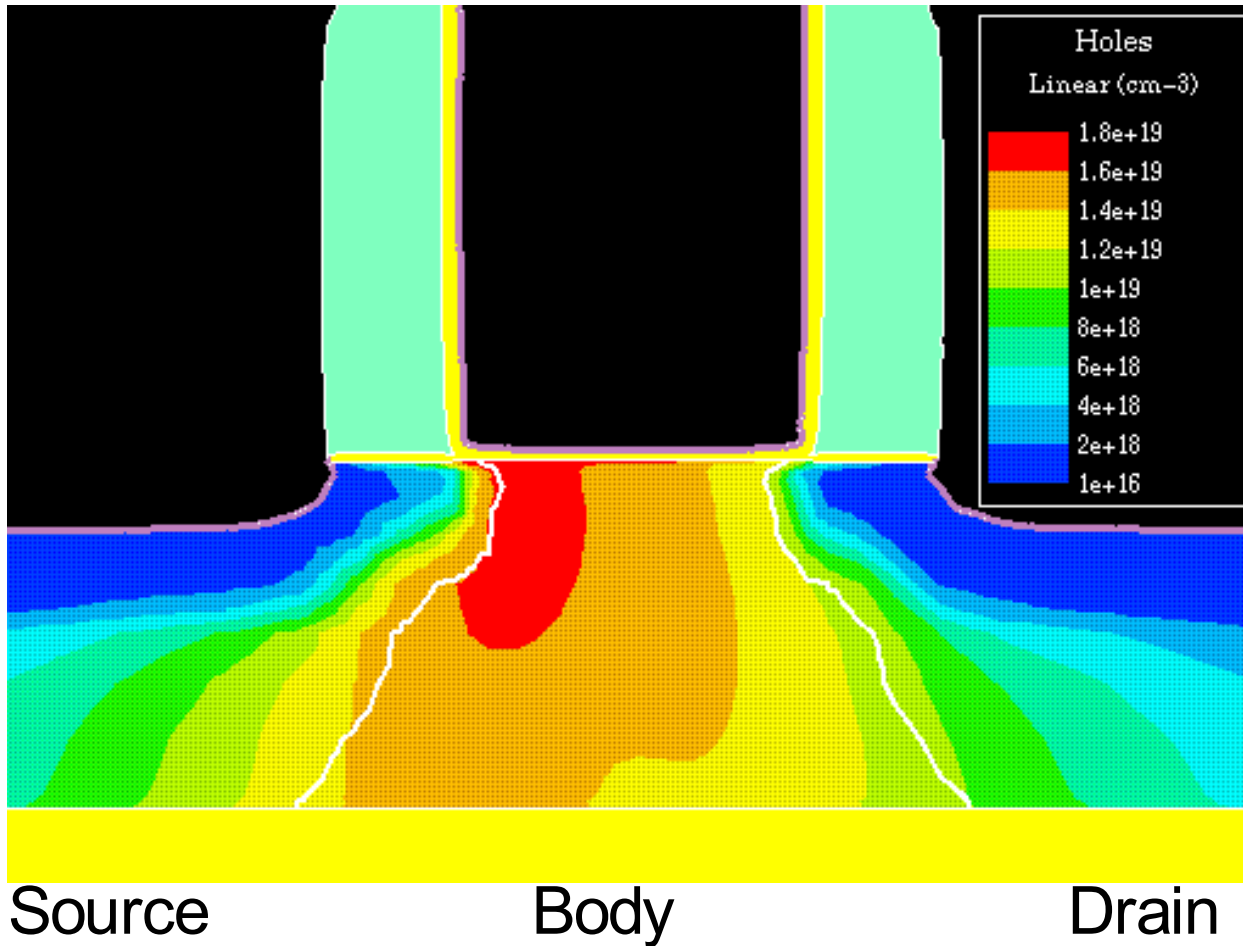
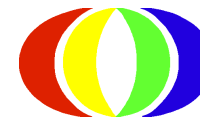
- Goal: a simple SPICE model using closed-form, physics-based equations
 - Enables SEE analysis of large numbers of circuit cells and logic storage cells and their various combinations.
 - 3D/2D analyses [2]-[4] are too expensive and time-consuming for such general engineering use.

(a) Layout of NMOS transistor and (b) SPICE model [13]



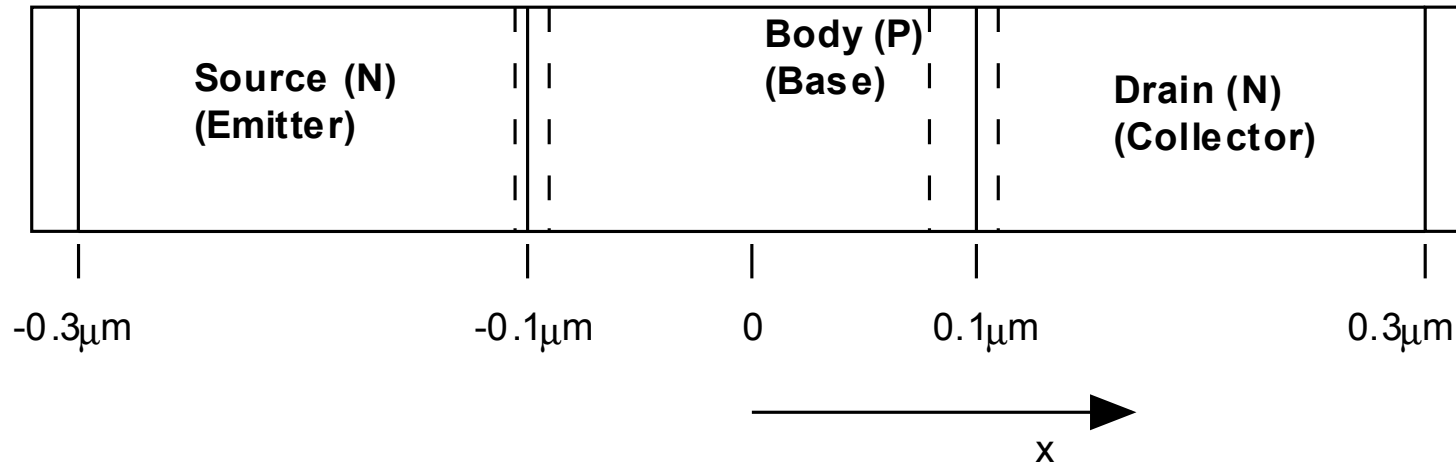
- Goal: Translate from the physical device (a) to a physics-based SPICE model (b).
- Process: 0.15 μm partially-depleted SOI from Honeywell.

2D simulation [6],[7], holes at $t=100\text{ps}$, 100fC vertical ion strike on the center of NMOS body within inverter [13]



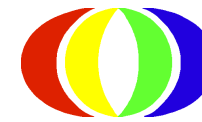
Note: Excess carriers penetrate substantially into source and drain regions.

1D approximation of the parasitic bipolar npn transistor [13]

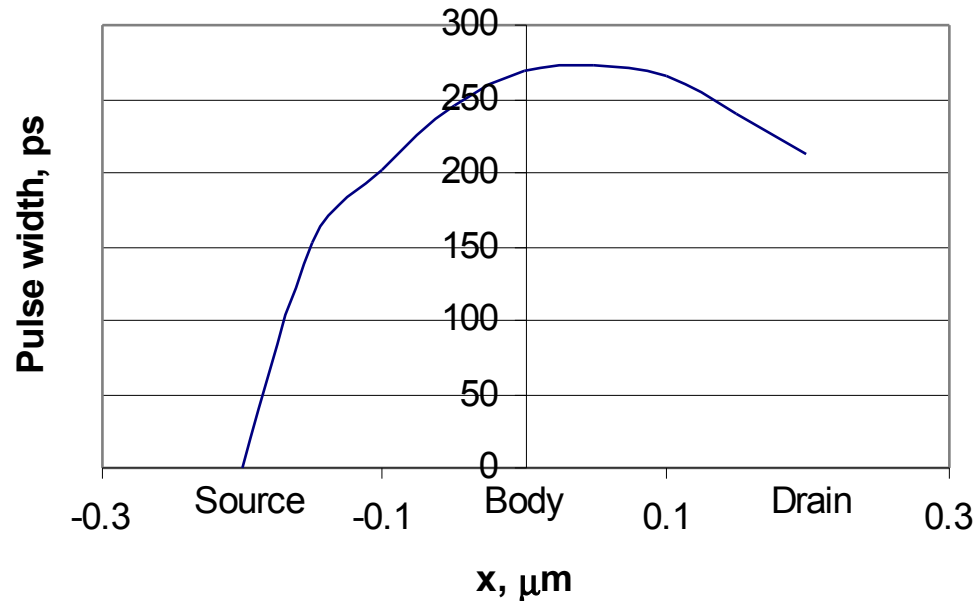


- 1D simulation gives insight into a physics-based closed-form SPICE model.
 - Ohmic contact at ends.
- 1D transport equations [10] solved to determine effects of ion strikes.
 - Equation solver is an original one [13] programmed in BASIC.

Pulse width vs. Position from the 1D simulation of a 100fC vertical ion strike on the inverter [13]

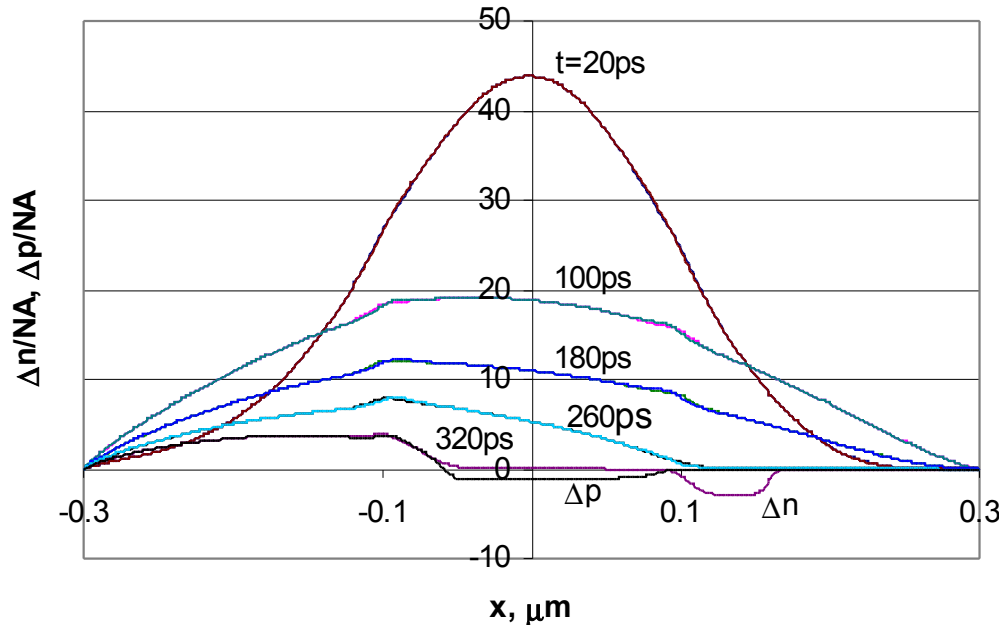
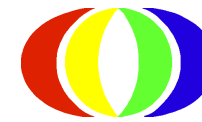


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- Pulse width defined from $V_{DD}/2$ to $V_{DD}/2$.
- Worst-case (max) pulse width is near the center of body.
- Pulse width rapidly drops to zero in the source.

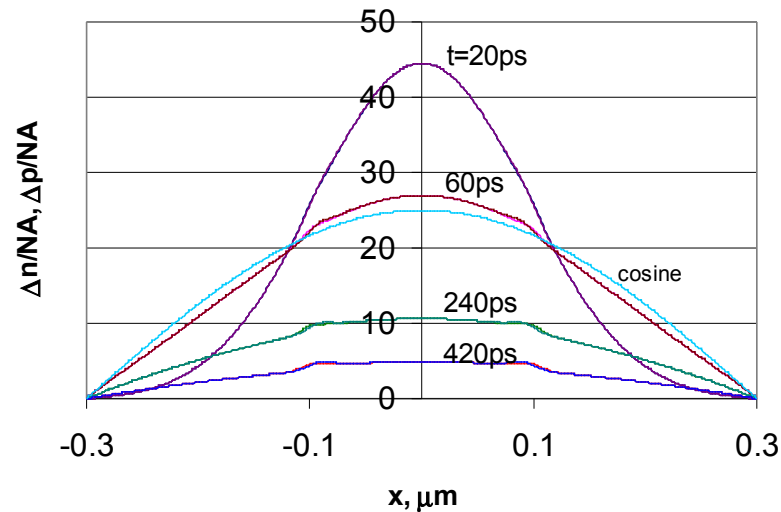
Excess carrier concentration in the NMOS transistor in the inverter (1D) [13]



- Excess hole and electron concentration almost identical (“quasi-neutral” concept) except when junction reverse-biases (e.g. at 320ps).

- 1D solution similar to 2D.

Excess carrier concentration in the NMOS transistor with no external discharge currents (1D) [13]

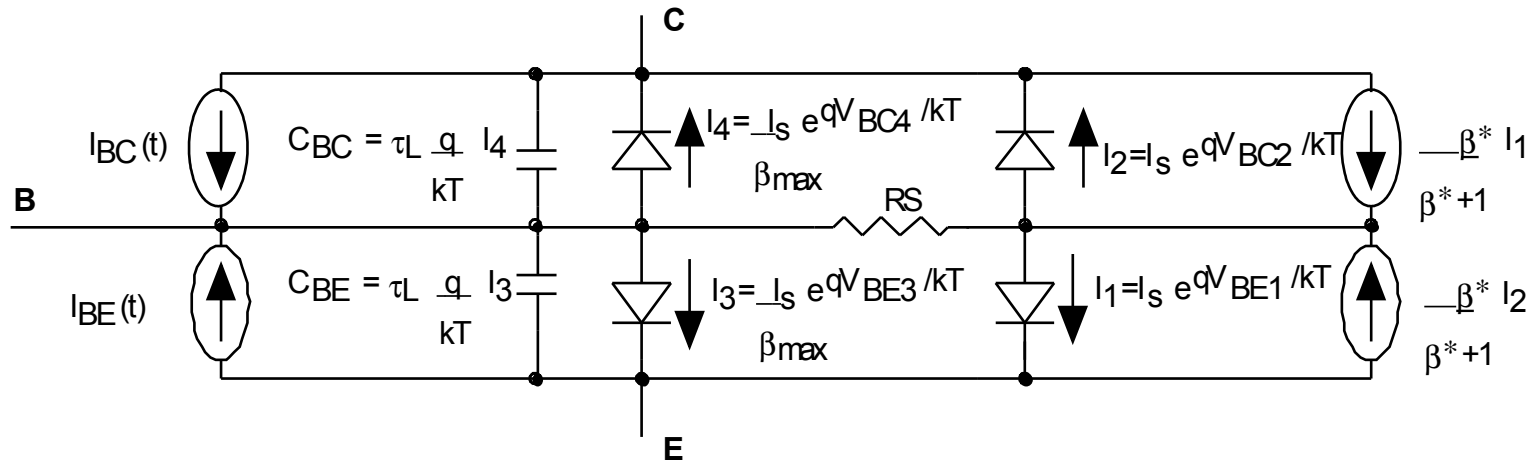


- From the ambipolar diffusion equation, it can be shown that the time constant for charge decay is [6]

$$t_L = \frac{L^2}{\pi^2 D}$$

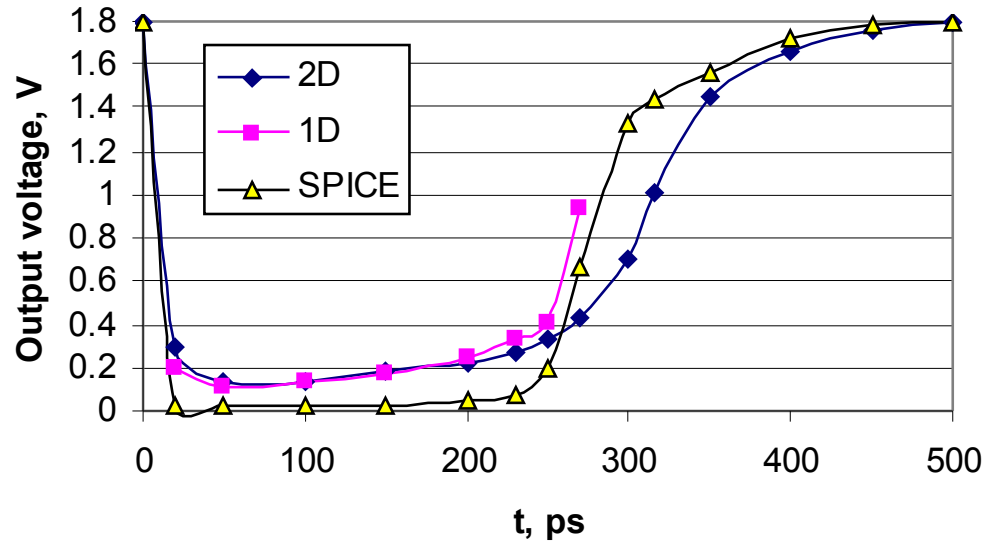
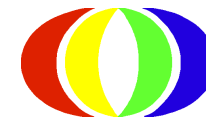
Using $L=0.6\mu\text{m}$ and $D=2\text{cm}^2/\text{s}$, this is 180ps (consistent with above 1D solution).

SPICE model for the parasitic npn bipolar transistor [13]



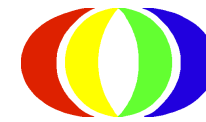
I_{BC} and I_{BE} are radiation photocurrents from [6].

Output voltage of the inverter from 2D, 1D, and SPICE for a vertical 100fC⁻ ion strike on NMOS [13]

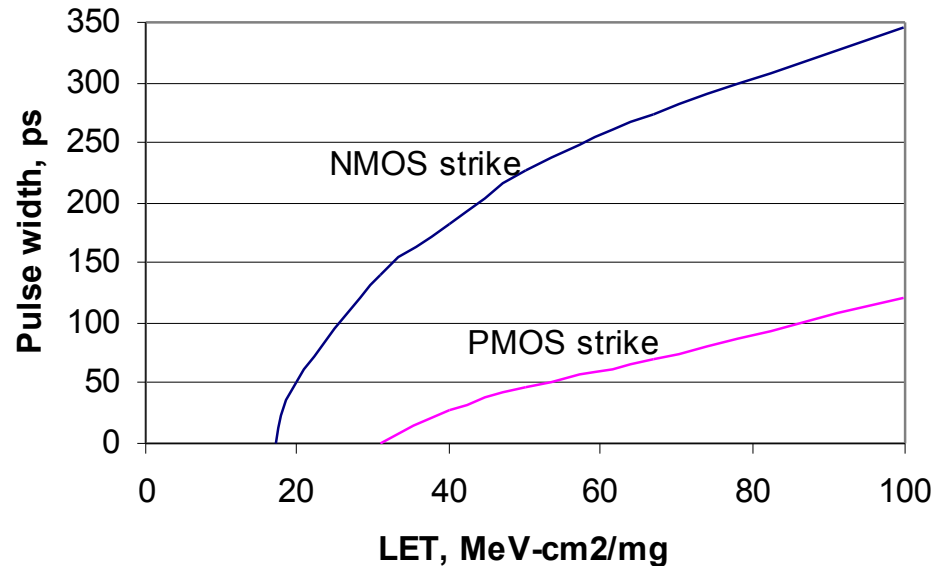


All 3 methods give similar results!

Output voltage pulse width vs. LET for strikes on NMOS and PMOS transistors in the inverter [13]



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Deposited charge was converted to LET by [12]

$$\text{LET} = 0.1 Q_d/d$$

LET in MeV-cm²/mg, Q_d in fC, d is depth of Si in μm .

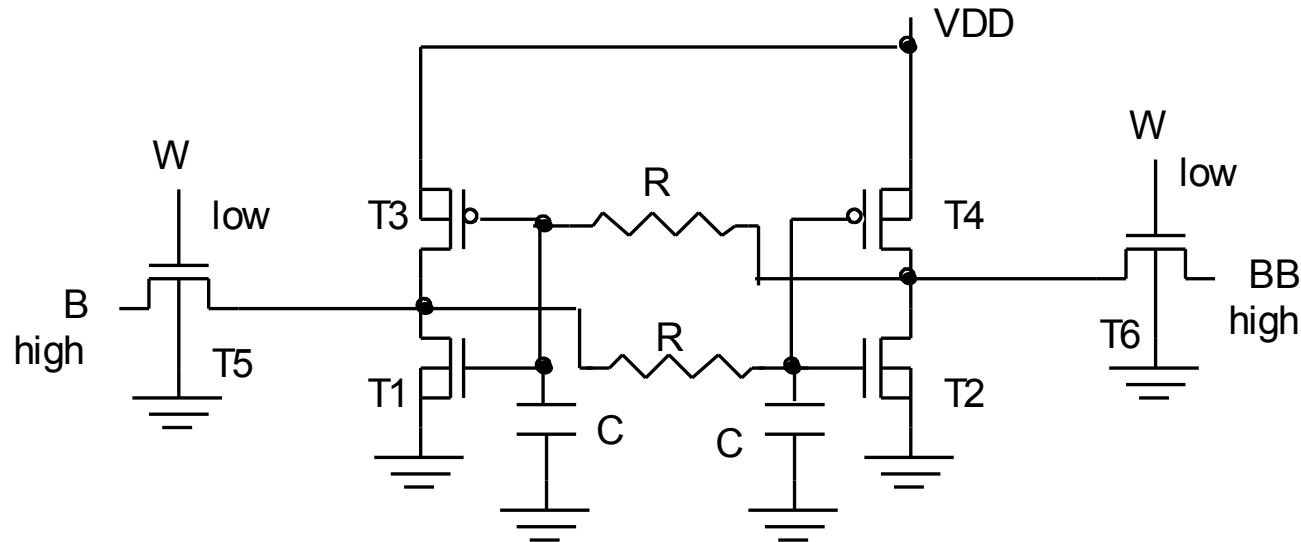
SPICE-simulated vs. Experimental threshold LET for various circuits[13]



<u>Circuit</u>	<u>Simulated threshold LET</u>	<u>Exper. Threshold LET</u>
1X Inverter	43	36
2X Inverter	80	>93
2-PMOS Inverter	24	20
1X Delay FF	23	19
2X Delay FF	89	>93
6T SRAM	7	6

SPICE model matches experimental results well!

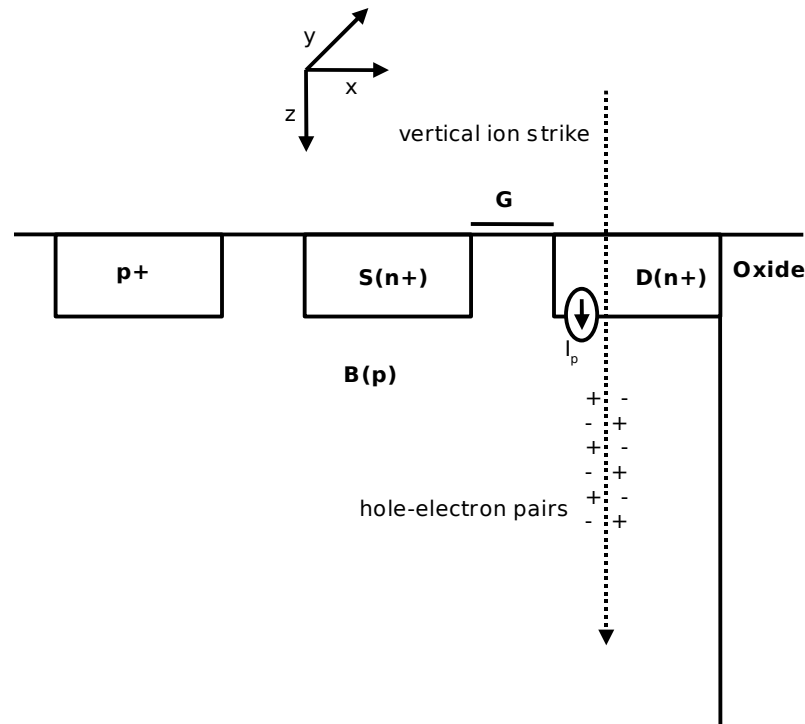
Circuit diagram of an RC-hardened SRAM [13]



- Hardened to an LET of $80\text{MeV}\cdot\text{cm}^2/\text{mg}$ with $RC=190\text{ps}$.
- An RC time constant of 900ps is required to achieve the same hardness in a bulk process with similar feature sizes [1]. This means much slower speed.

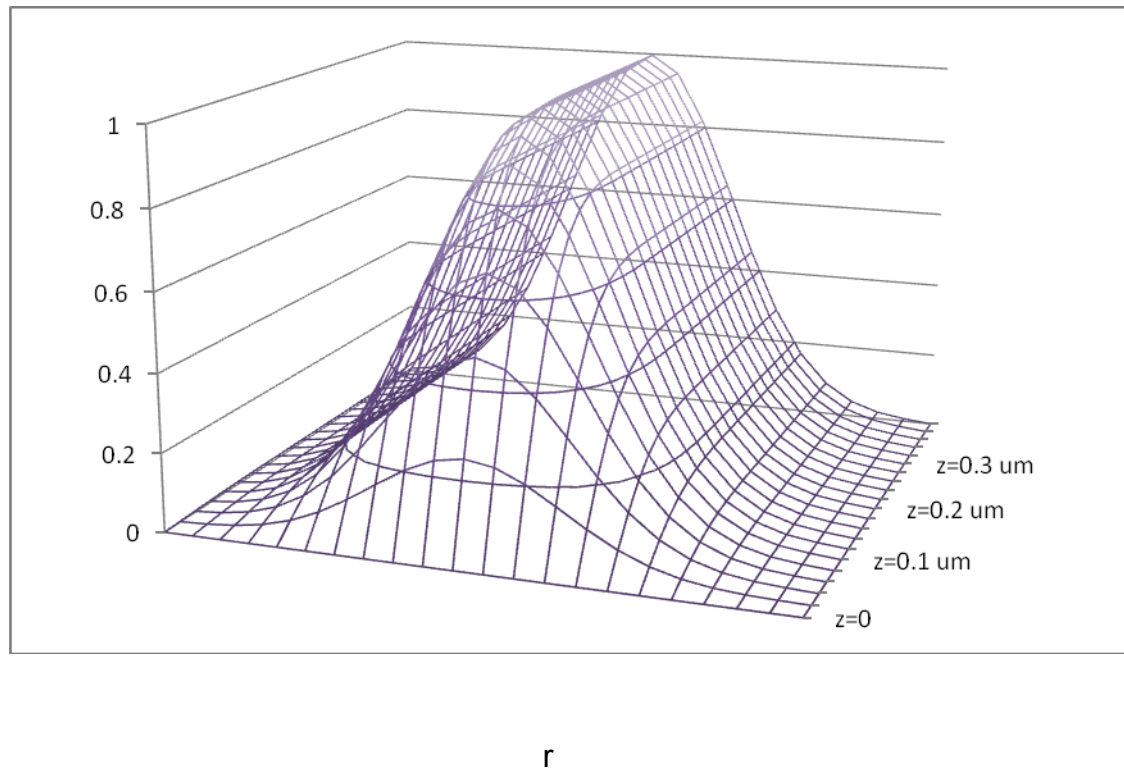
- In an analogous but simpler manner, bulk CMOS can also be analyzed using the ambipolar diffusion equation.
- Patent pending; David Fulkerson, inventor and assignee.

Cross-section of a bulk NMOS transistor



- SOI CMOS has no bulk region under the drain.
- Additional hole-electron pairs are created in the bulk region, thus adding to SEE sensitivity.

Normalized carrier concentration vs. lateral distance (r) and depth (z), 10 ps after an ion strike normal to a pn junction



Above is a closed-form solution to the ambipolar “diffusion” equation (which actually takes into account both drift and diffusion at high injection) [6]:

$$\frac{\partial n}{\partial t} = D \nabla^2 n$$

where D is the ambipolar diffusivity. Reverse-biased pn junction is at z = 0.

Note: Above differential equation must be solved very carefully because of subtleties in the physics!

Soft error rate of previous unhardened SRAM in SOI and bulk CMOS



Soft error rate (SER, in errors per bit-day)
can be calculated either from CREME96 [14] or a simpler proprietary method in the “Adams 90%” radiation environment:

SOI
9.1E-9

Bulk
1.8E-8

- By re-interpreting 2D results in a 1D format, closed-form physics-based equations can be derived for SEE effects.
- SPICE model is derived from closed-form equations.
 - Simple SPICE model is very desirable because of large number of cells and their combinations.
- Experimental LET thresholds of several different circuits were accurately predicted by the new SPICE model.
- Compared to bulk CMOS, time-delay hardening is obtained in SOI with much less speed compromise.
- Model is effective engineering model for both SOI and bulk CMOS.

Honeywell Plymouth for funding the majority of the SOI analysis and providing SOI circuits and testing.

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