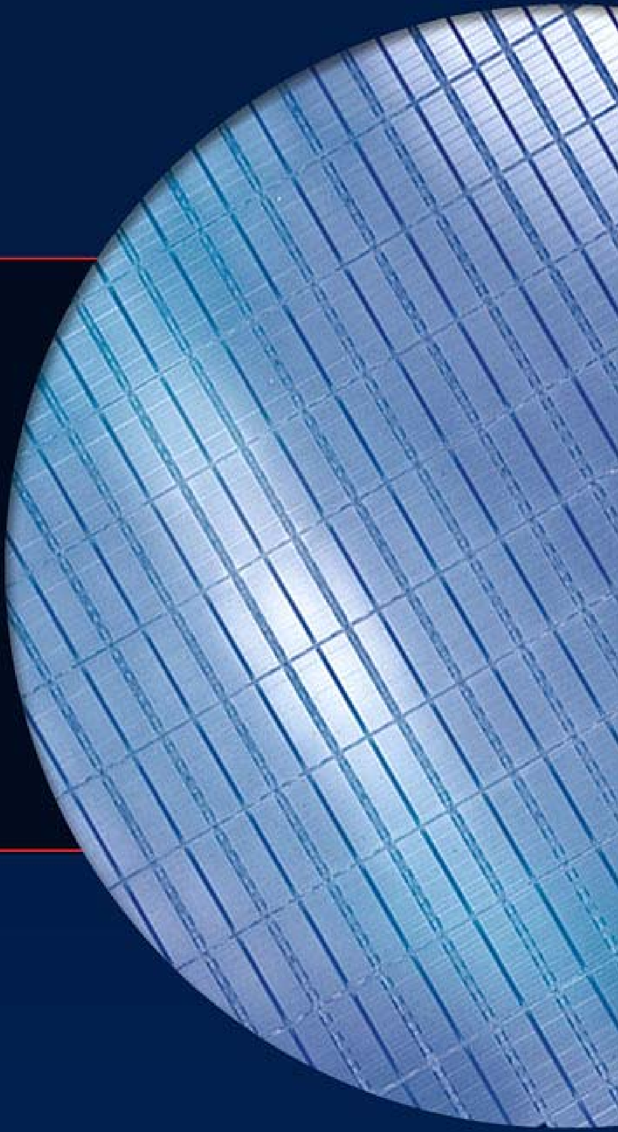
Improving Quality of Analog/RF Designs



Artur Balasinski, Joseph Cetin
Cypress Semiconductor
San Diego, CA 92128, USA

Motivation

Analog/RF design: new challenge for technology

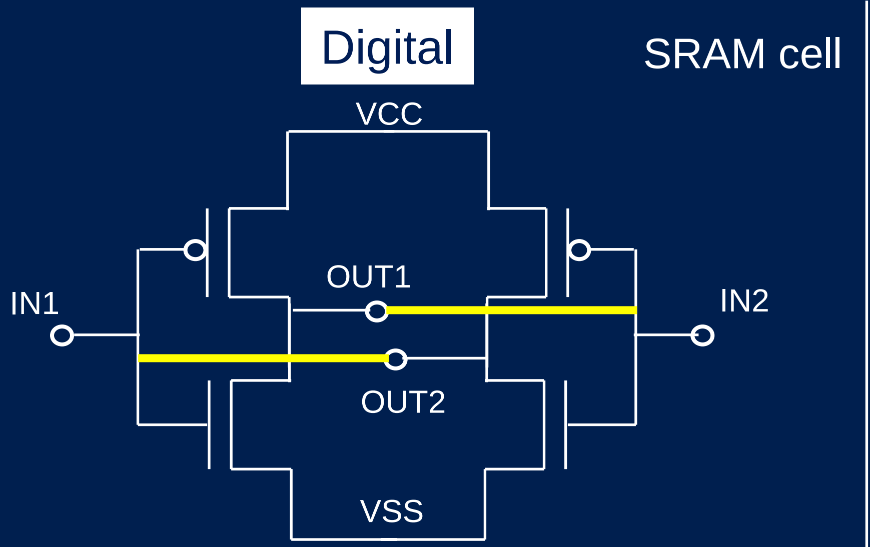
- New circuit requirements => better modeling accuracy
- Reduced distances between features => increased interactions
  => slower shrinkpath

Design Issue	What to Improve - Technology Issue	How
Exponential leakage (5 nm CD = 10 x leakage) incompatible with handheld applications	Horizontal dimension (CD) variation 10% guardband is too wide	OPC High-NA litho tools
Capacitive coupling for RF as dangerous as resistive path for DC	Vertical dimension (planarity) variation Capacitance sensitivity to fill pattern	New fiil or extraction
Mismatch among identical blocks (standard cells)	Layout environment incl. OPC and dummy features	Fixed orientation and placement rules

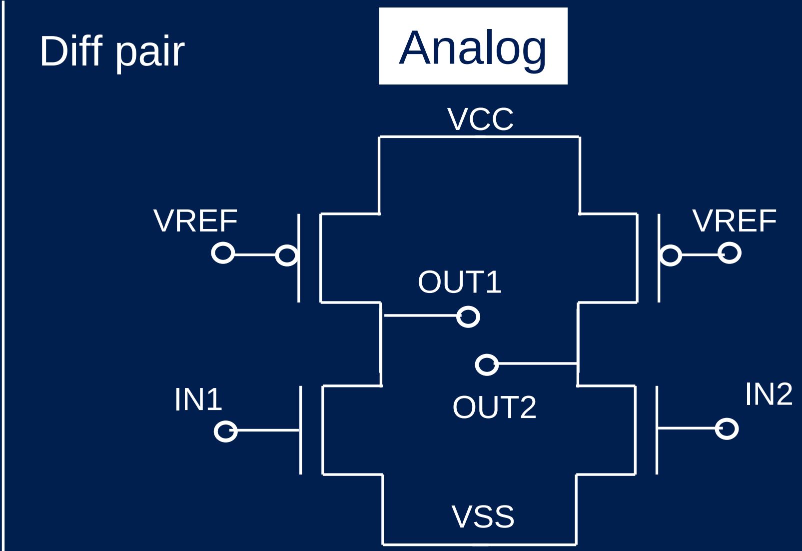
Should we improve design, CAD, or technology ?
At what cost/priority ?

Why RF/Analog ?

Digital SRAM cell



Diff pair **Analog**



< 0.3 VCC; e.g., 300 mV	**Vin for 0**	**May require sensitivity down to μV level**
> 0.6 VCC, e.g., 600 mV	**Vin for 1**	
Tied to input – low gain	**Output**	**High gain**
>100 mV	**SNM / mismatch**	**3% of RC, 5mV VT 1σ**

High Sensitivity:	Response:
Differential pairs	Same CD and orientation
DAC/ADC	Precise mismatch models
Phase lines	Symmetrical inputs

DfM or MfD ?

Category	Issue	Response	Example	Cost
DfM	Low bandwidth	Restrictive design rules	Larger spaces to dummy fill Fill extraction	IP invalidation Area penalty
DfM	High leakage	New design rules	Pitch Orientation	IP invalidation CAD execution
DfM	Device mismatch	New OPC and fill engines	Multiple CD control targets	Model calibration Mask issues
DfM	Frequency shift in time	New design flow	Reliability simulation	Runtimes Models
DfM	High power noise	New devices	Fixed layout Wide L precision R	No layout options Area penalty
MfD	High leakage	Upgraded fab equipment	New etch for better line profile	New equipment
MfD	Poor yield	New fab process	Exposure correction to tighten CD budget	Process development
MfD	High via R	New materials	New CMP slurry	Cost of slurry Time to etch

Methods needed to evaluate impact

DfM vs. MfD

- Issues:
  - Financial impact: cost of tools, delays, silicon vs. yield advantage
  - Confusion: rule deck options: mandatory / mandatory and optional
  - Training: manufacturing success a function of design discipline
  - Responsibility: “improve design” or “improve technology” ?

- Solution:
  - Analyze failure modes relating to individual rules (FMEA)
  - Calculate RoI
  - Compare FMEA and RoI approaches
  - Select the required rules

DRC/DfM for Analog/RF

Variability reduction required for analog/RF design

Domain	Type	Optical/Pattern	Physical	Electrical	Time	CAD
Single feature	Issue	Can we print it ?	Would it work if built ?			
	Single layer	CD line, space, area	Wall thickness	Isolation Gate L		Sizing
	Multiple layers	Enclosure, overlap	Contact fill	VT, ID, S, BVDSS	EM, HCI, NBTI, TDDB	Creation algorithms
Feature to feature Interaction	Issue	Can we manufacture it at profit ?				
	Interaction	Horizontal	Vertical		Runtime	
	Short range	RB OPC MB OPC	Stress relief	ESD Latchup	OPC algorithms	
	Long range	CD control for etch	Planarity ctrl for via R and cap Matching		Fill pattern algorithms	

FMEA and RoI

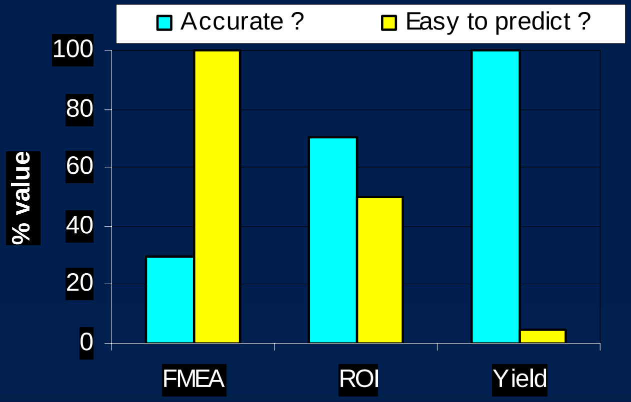
- **FMEA criteria:**
  - **severity (S)**
  - **occurrence (O)**
  - **detectability (D)**

RPN = Risk Priority Number

1. S
2. S x O
3. S x O x D

- **ROI criteria:**
  - **development**
  - **area penalty**
  - **execution time**

Time to Money



FMEA - Severity

Effect	CRITERIA	EXAMPLE	RANK
Hazardous w/o warning	Affects existing good parts or equipment	Photoresist lifting and re-dep on other wafers	10
Hazardous w/warning	Affects existing good parts or equipment	Not possible to etch – no endpoint reachable	9
Very high	Current part inoperable	No useful PR pattern	8
High	Operable; reduced performance	Printing all lines not possible	7
Moderate	Operable at center of process window only	Wafers require retargeting for every lot	6
Low	Operable over process window, poor control	Poor image contrast – potential for bridging	5
Very Low	Operable, features visually inconsistent	Poor OPC correction of some resistor lines	4
Minor	Operable; non-critical features off target	CD control poor along some connecting lines	3
Very minor	Minor / cosmetic items	Symmetry of fill pattern	2
None	No effect	Meets all process targets	1

FMEA - Occurrence

Probability	CRITERIA	EXAMPLE	RANK
Very high – persistent	10% or more	Core cells in typical process conditions	10
	5 – 10%	Multiple blocks	9
High – frequent	1 – 5%	Some types of blocks	8
	0.1 – 1%	Few types of blocks over process window	7
Moderate – occasional	0.01 – 0.1%	Some lines in a few blocks	6
	10 – 100 ppm	Few lines in 1-2 blocks	5
Low – relatively few	1 – 10 ppm	Single lines in 1-2 blocks	4
	Below 1 ppm	One line in one block	3
Remote - unlikely	Below 10 ppb	Part of line in a block	2
	Below 1 ppb	None or under extreme conditions only	1

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FMEA - Detectability

Detectability	Detection by	EXAMPLE	RANK
Absolute uncertainty	No design control	Poor yield = High cost	10
Very remote	P, Q, R	Product failures	9
Remote	P, Q	Detectable at end of line	8
Very low	P, Q	Detectable at dedicated etest	7
Low	Q, R	Detectable by design review, custom ORC	6
Moderate	Q	Detectable by custom ORC	5
Moderately high	Visual at defect site	Would be detected by standard ORC	4
High	Visual near defect site	Would be detected by DRC	3
Very high	Visual at block level	Gross pattern density issue	2
Almost certain	Visual at die level	Wrong data ?	1

P=Prototypes, Q=CAD QA, R=Reviews

Design Rule FMEA

	Rule	Category	Severity	Occurrence
1	Width	Photoresist	8	5
2	Spacing		8	5
3	Area		7	3
4	Enclosure	Photo Eqpmt.	7	5
5	Extension		7	5
6	Overlay		7	5
7	Length	Sub-100 nm process	4	3
8	Orientation		4	5
9	Pitch		5	5
10	Matching	Electrical	5	3
11	Wire spreading		3	4
12	Redundancy	Defect	3	3
13	Via doubling		3	4
14	Density	Planarization	5	5
15	Fill (smart)		5	5
16	Jog/notch/SB	Mask	3	4
17	Antenna	PID	5	4
18	Stress relief	Reliability	5	3
19	Infrastructure	Database	3	1

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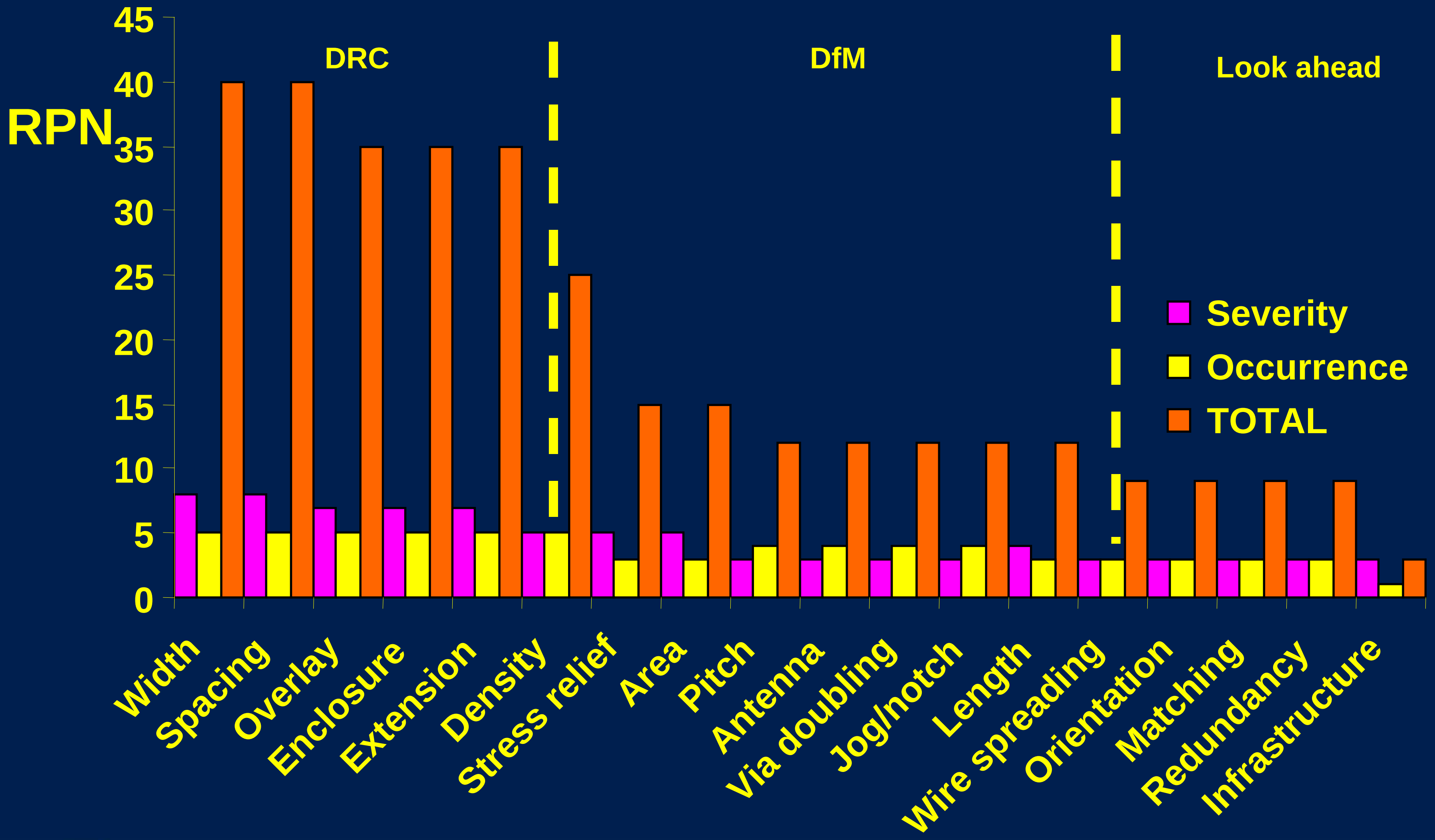
Design Rule FMEA



What this means: FMEA can set up rule priority

TTM Equation

$$TTM(weeks) = \frac{Total\_CAD\_Cost(\$)}{(\Delta Yield - \Delta Area)(\$/wk)}$$

Time to Money

cost of die yield loss

cost of die area increase

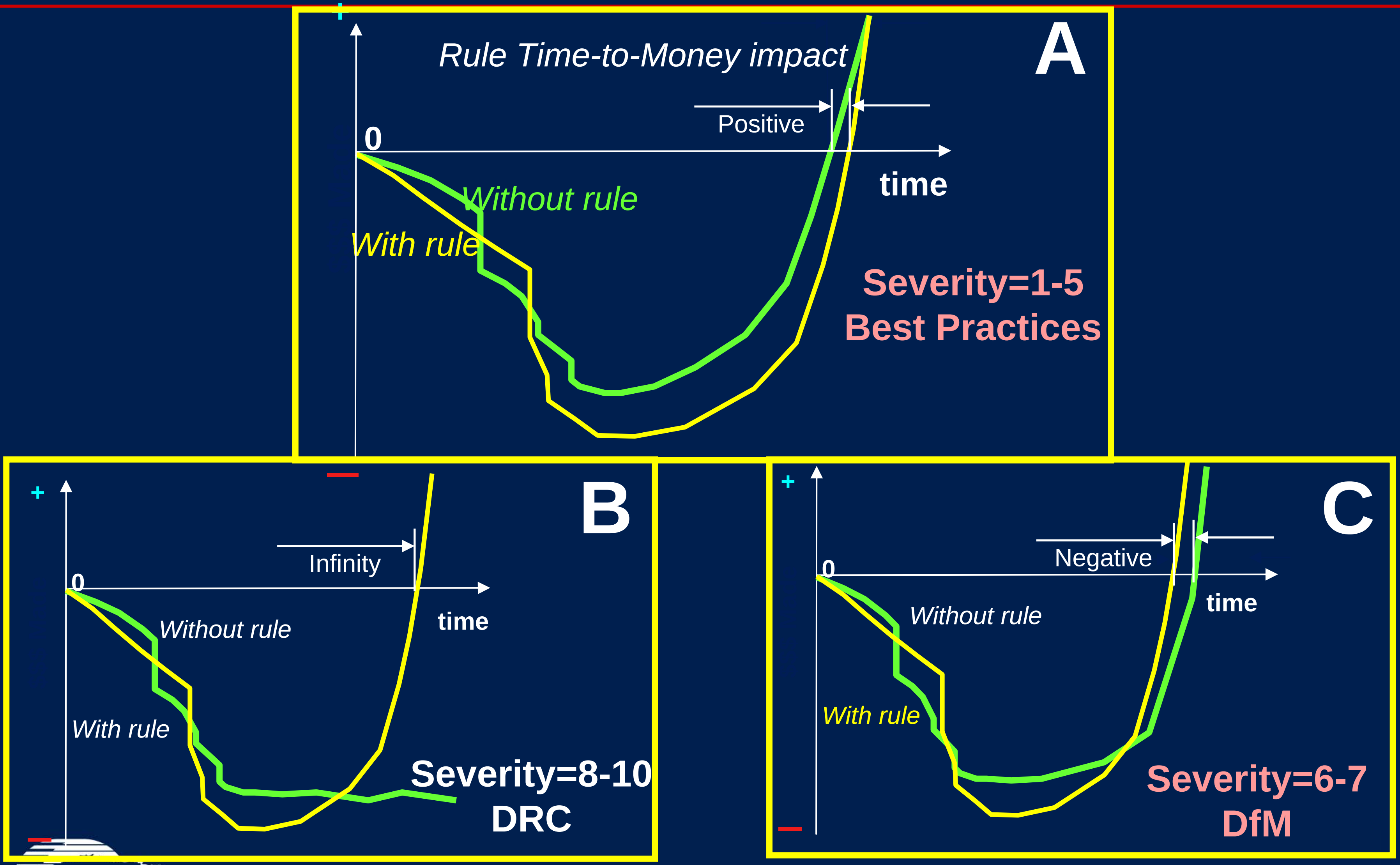
TTM = Total Design Cycle Time + Product Ramp-Up Time

$$TTM = TCT + \Delta PRT$$

Highest impact: ΔPRT reduction from infinity to finite value

Best case: ΔPRT negative (reduction of Design TCT)

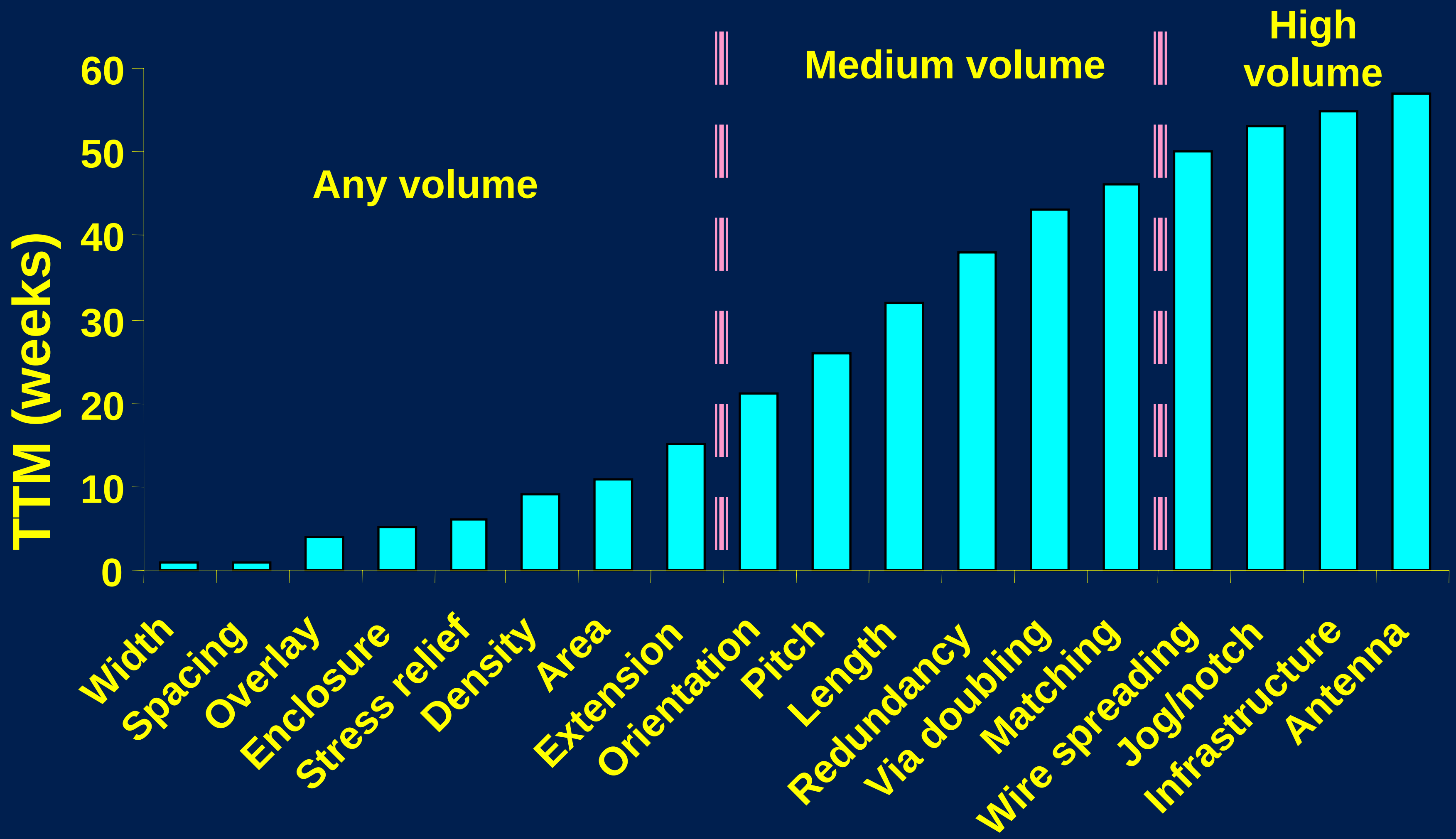
Product Lifeline Plot



RoI Example

Pattern Density	Effort	Labor	Delay	Cost of delay	DPW reduction	Total
	[mw]	[$]	[wks]	[$]	[%]	[$]
CAD Development	4	16000	2	1000000		1016000
CAD Execution	1	4000	1	500000		504000
Total CAD						1520000
Area penalty					5	25000
Yield impact per week					-40	-200000
Profit impact per week						175000
# TTM weeks						**9**

Rule Selection - Product Volume



What this means: Dangerous approach

RPN - TTM Correlation

FMEA Model

$$\Delta Yield = k_y \cdot [\cancel{(RPN)_{with\_DfM}} - (RPN)_{without\_DfM}]$$

RoI Model

$$\Delta Yield = \frac{Total\_CAD\_Cost(\$)}{k_f \, TTM}$$

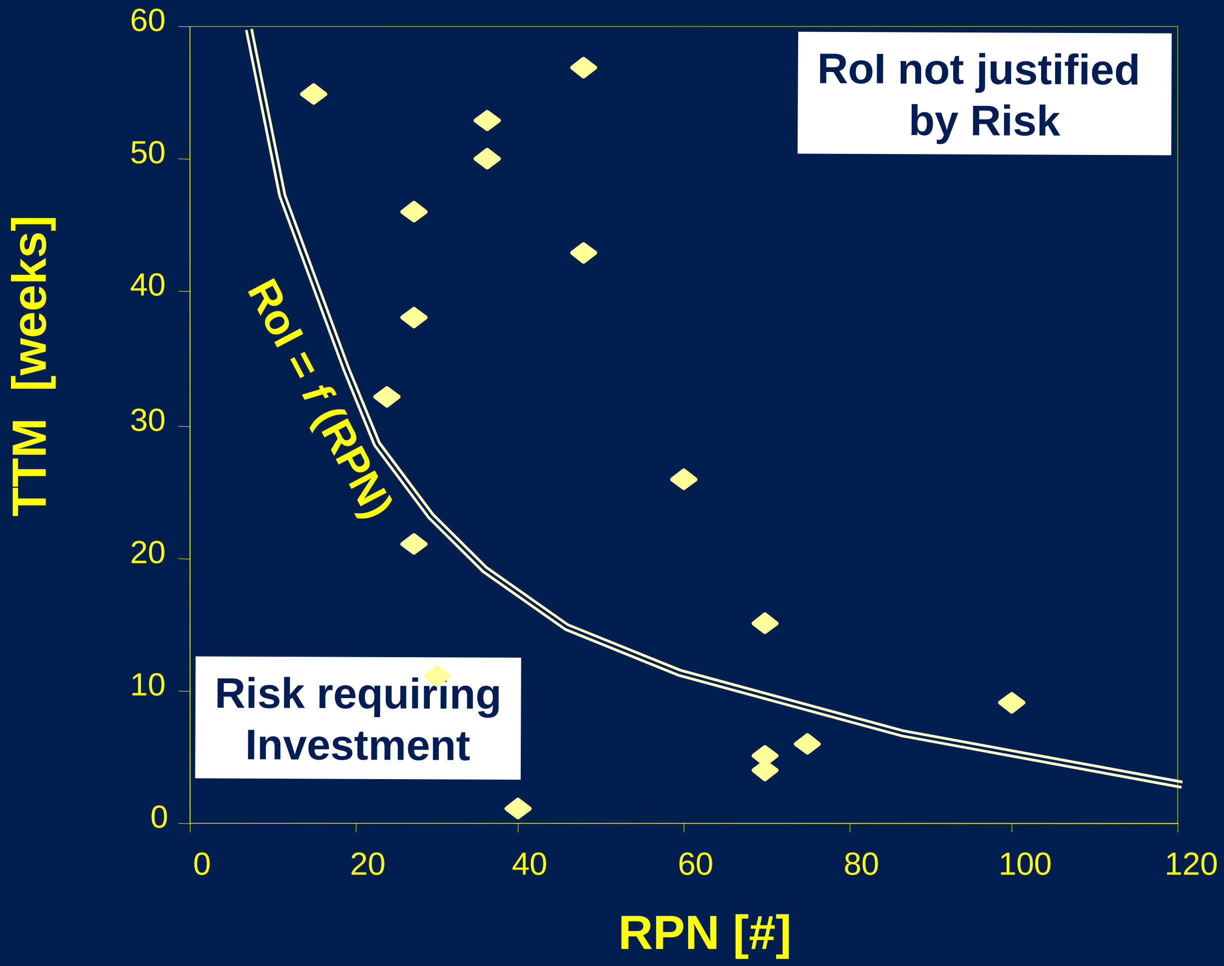
$\Delta Area = 0$

Combined

$$RPN = -\frac{Total\_CAD\_Cost(\$)}{k_f \, k_y \, TTM}$$

What this means: RPN is inversely proportional to TTM

Rule Selection: FMEA - RoI Correlation



RoI not justified by Risk

Risk requiring Investment

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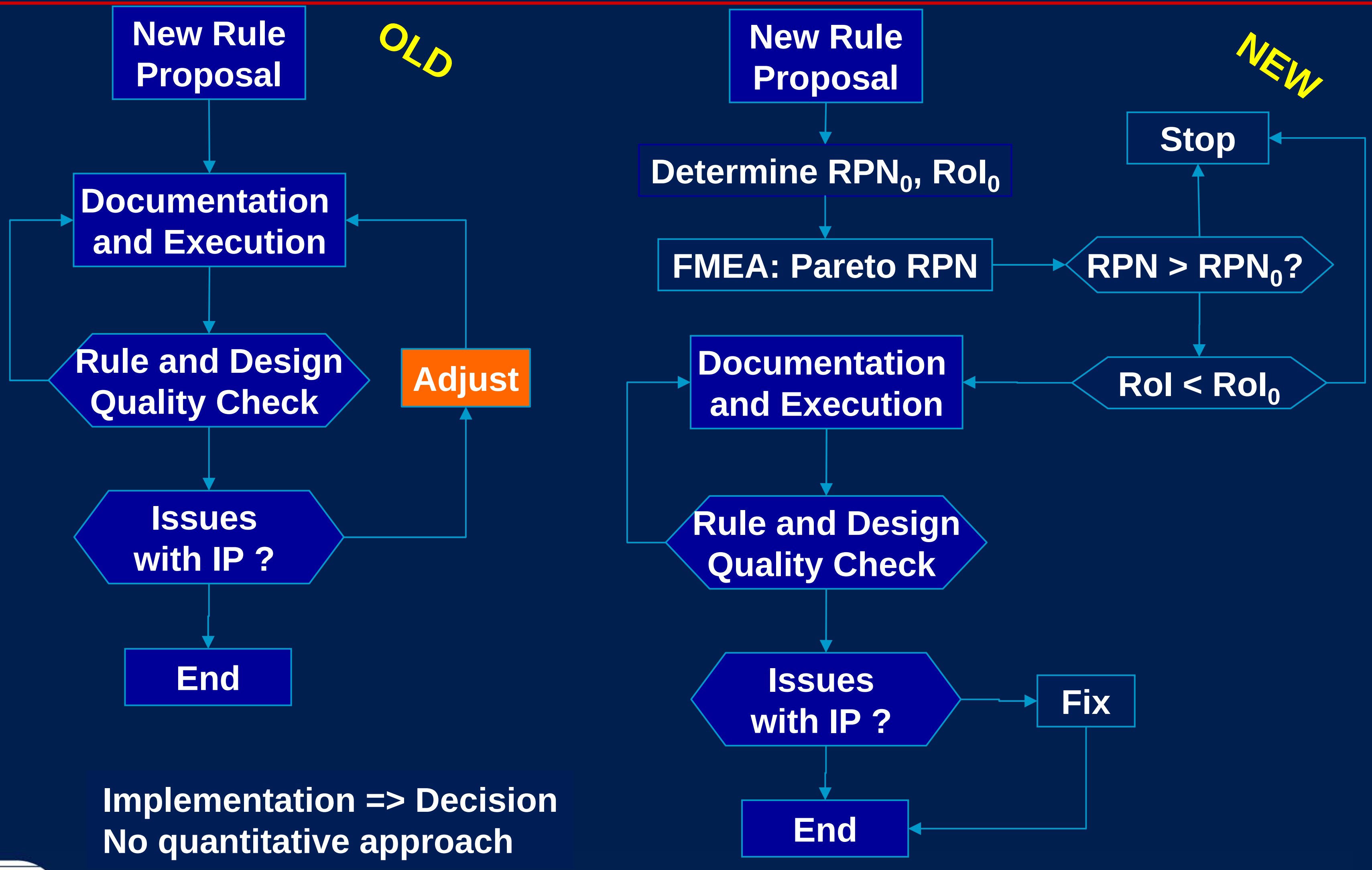
New Rule Introduction



Implementation => Decision
No quantitative approach

Conclusions

A quantitative model of design rule implementation based on FMEA and RoI:

- understand rule importance,
- clarify mandatory vs. optional rules.

Theoretical links: RPN and TTM, model parameters, yield, are explained

The methodology can be applied to determine analog/RF rules critical for design and manufacturing.