Recent Advances in VLSI Routing
- Serial Passive Clock Distribution -

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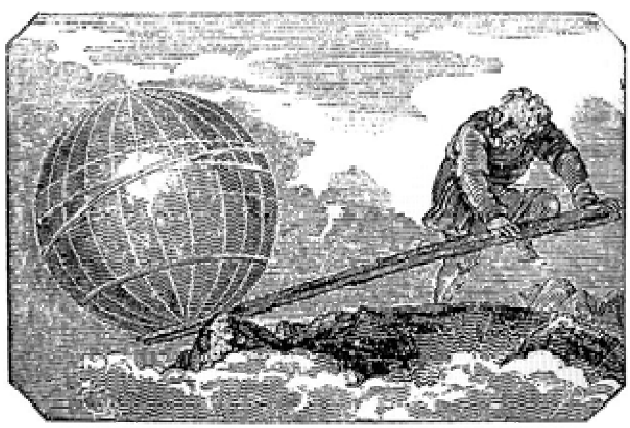
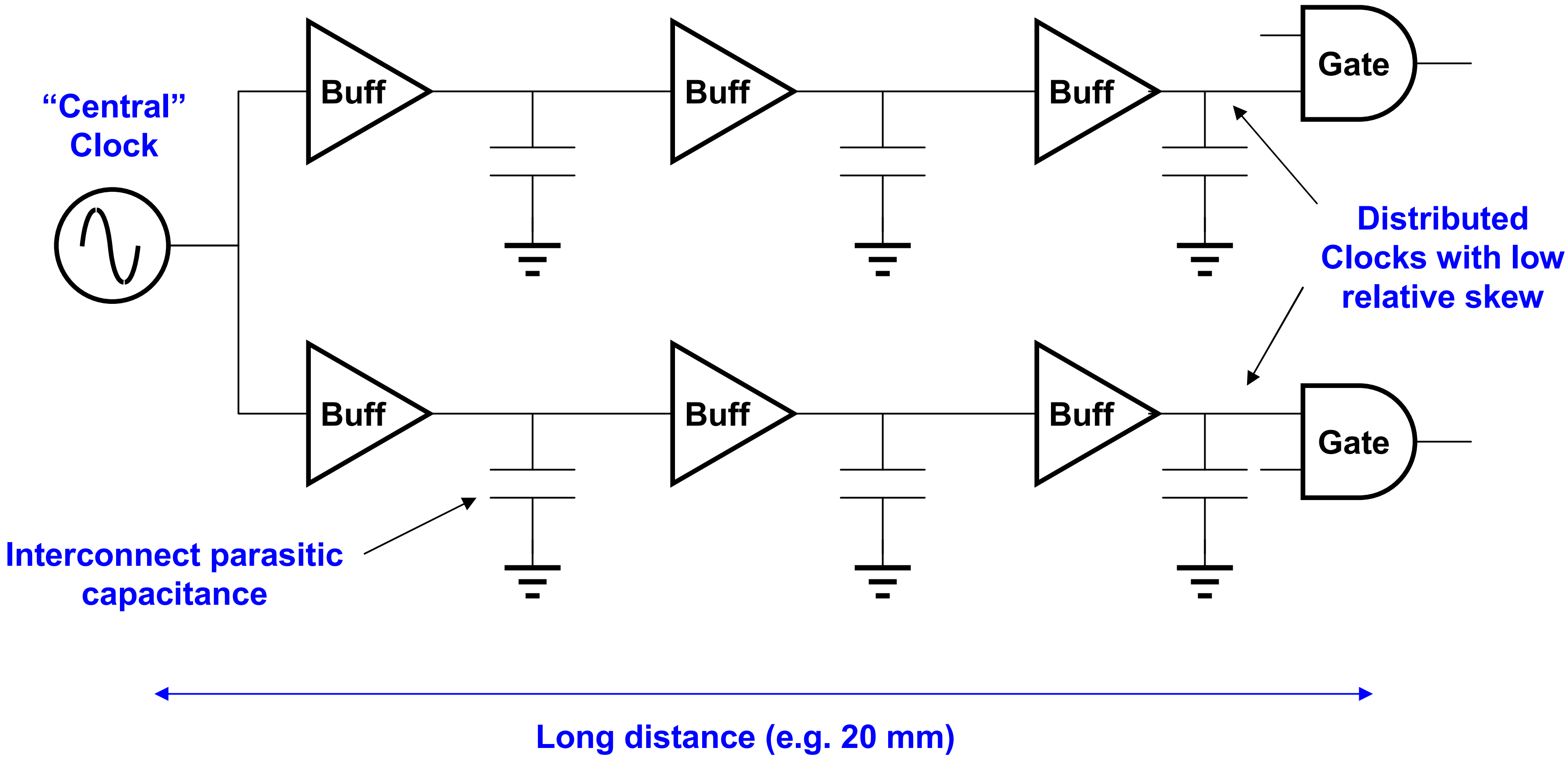
The Quest for Absolute References

Syracuse , Sicily, Circa 250 BC:
Archimedes' wish: "Give me a place to stand and rest my lever on... and I can move the Earth!"



Everywhere on Earth, Circa 2000 AD:
VLSI designers' wish: "Give us clocks without skews and jitter and we can design ICs as big as the Earth!"

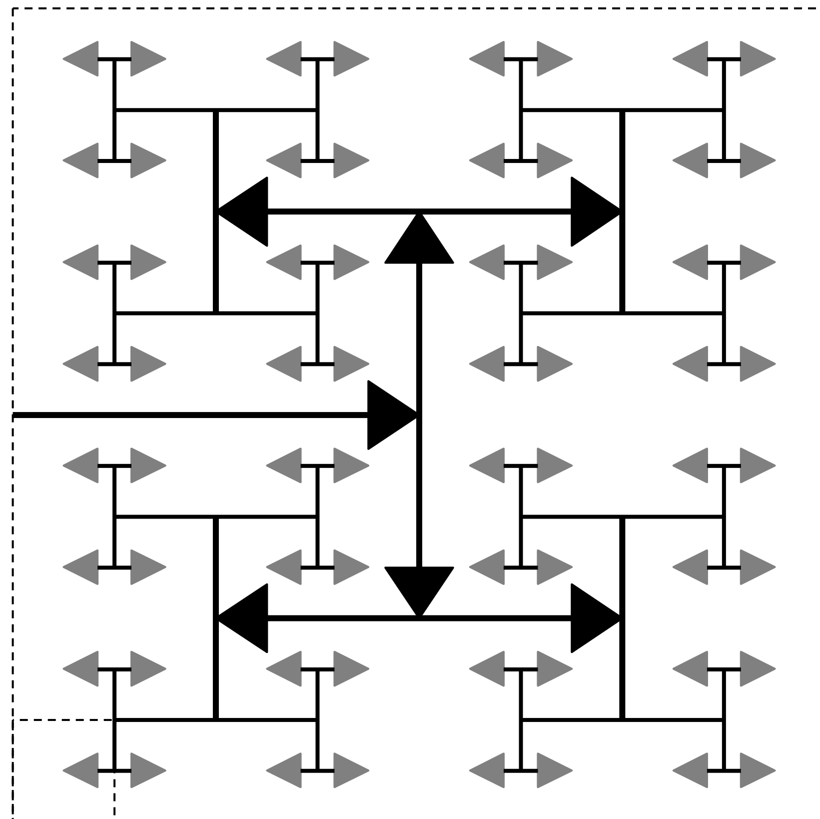
How Do VLSI Designers Synchronize ICs?



Ideal Case: The Active H-Tree

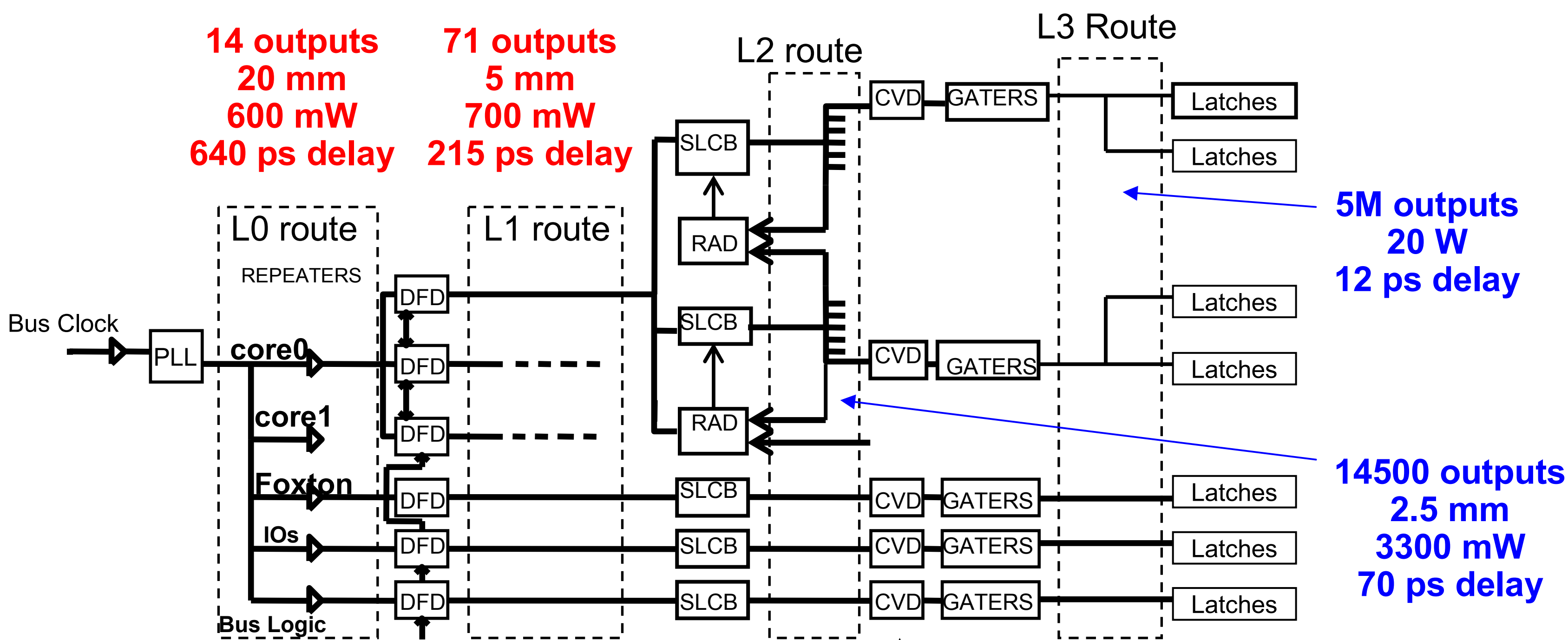
<u>Fundamental Shortcomings</u>

- **Assumes perfect electrical symmetry in clock distribution!**
- **Assumes accurate load matching at top of the tree, which is spread over entire chip**
- **Many active stages: buffers**
- **Tree loading and clock distribution highly coupled**



Real VLSI Clocking: What a Headache!

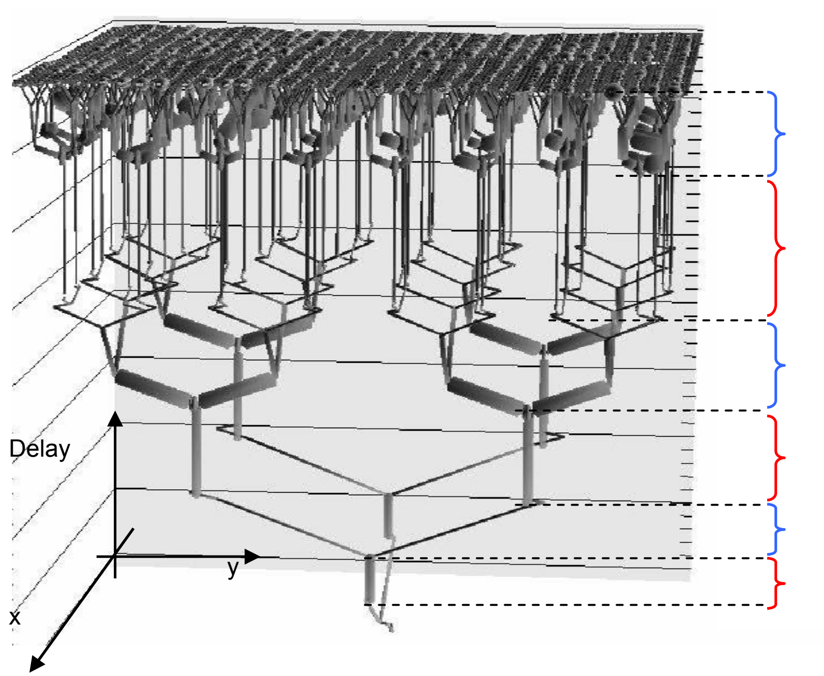
Typical VLSI GHz Active-Tree Clocking (1.8 GHz Intel Montecito ISSCC'05): High Complexity, High Power, Difficult to Scale



Thousands of phase adjusting CVDs!!!

Flat Canopy of Typical Active Tree

Power PC Processor Clocking Tree: J.D.Wornock at al, “The circuit and physical design of the POWER4 microprocessor,” IBM Journal of R&D, Vol. 46, Nov. 2002.

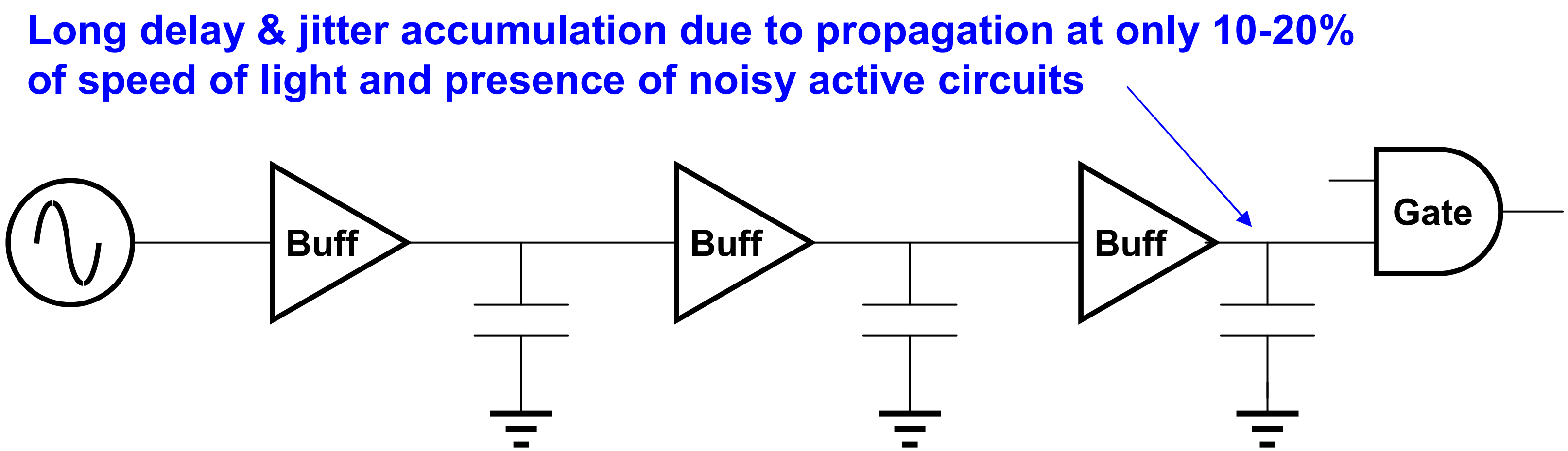


What Do We Really Really Want?

We want the clock distribution headache to go away!

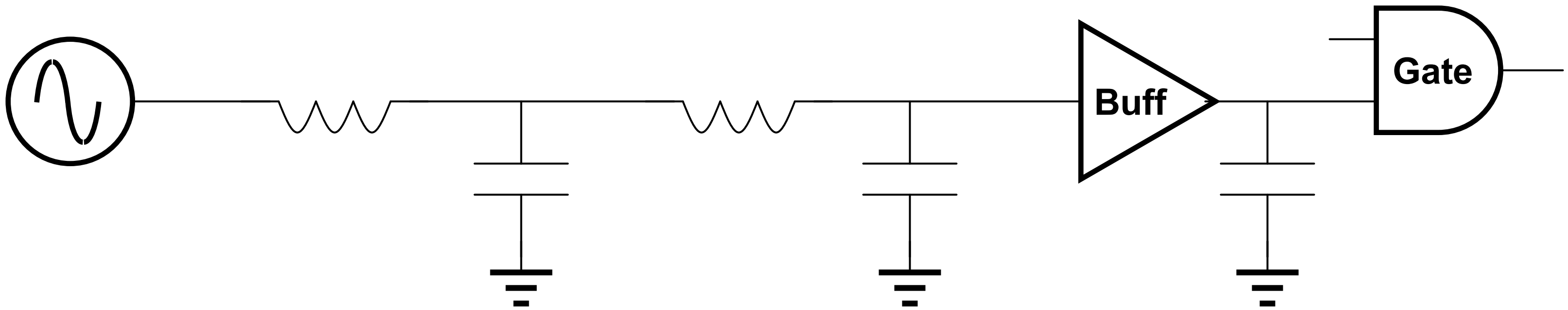
- We could try to redesign everything asynchronously and throw away 25 years of VLSI architecture knowledge/discovery work + industry wide design data bases, etc. (Good luck on this one!), or …
- We could keep digital systems the same and figure out how to make computers design the clocking distribution for us!
- And, by the way: The automatic design should be far superior in performance, power, cost, etc. to the active trees of today, humans design according to a black art!
- Therefore: We need a <u>breakthrough</u> idea in clock distribution!

What is Wrong With the Traditional Picture?



- **Why are we propagating the clock signal so slowly?**
  - Dissipative charging/discharging of line capacitors
  - This problem was solved 100 years ago by telegraph/telephone pioneers
- **Why do we need so many repeaters for only 20 mm of length?**
  - Dissipative charging/discharging of line capacitors
  - This problem was solved 100 years ago by telegraph/telephone pioneers
- **It sounds we need to get back to basics!**

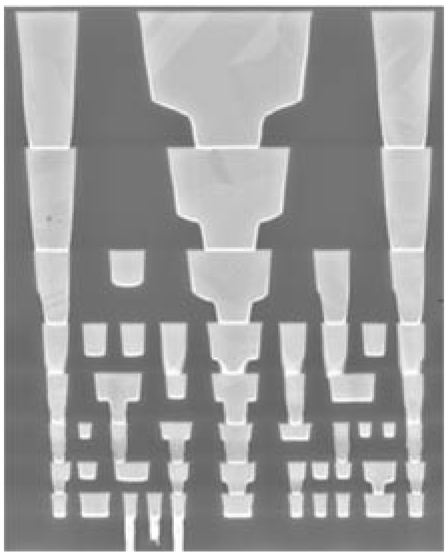
Transmission Lines to the Rescue



- **Propagation at light speed (in dielectric) up to local clocking regions!**
- **No repeaters!**
- **Lowest possible delay and jitter accumulation in clock distribution**
- **Lowest possible power dissipation in clock distribution**
- **Electrical transmission lines in VLSI already proven**
- **Optical wave guides in VLSI possible in the future**

Transmission Lines on a Chip, Really?

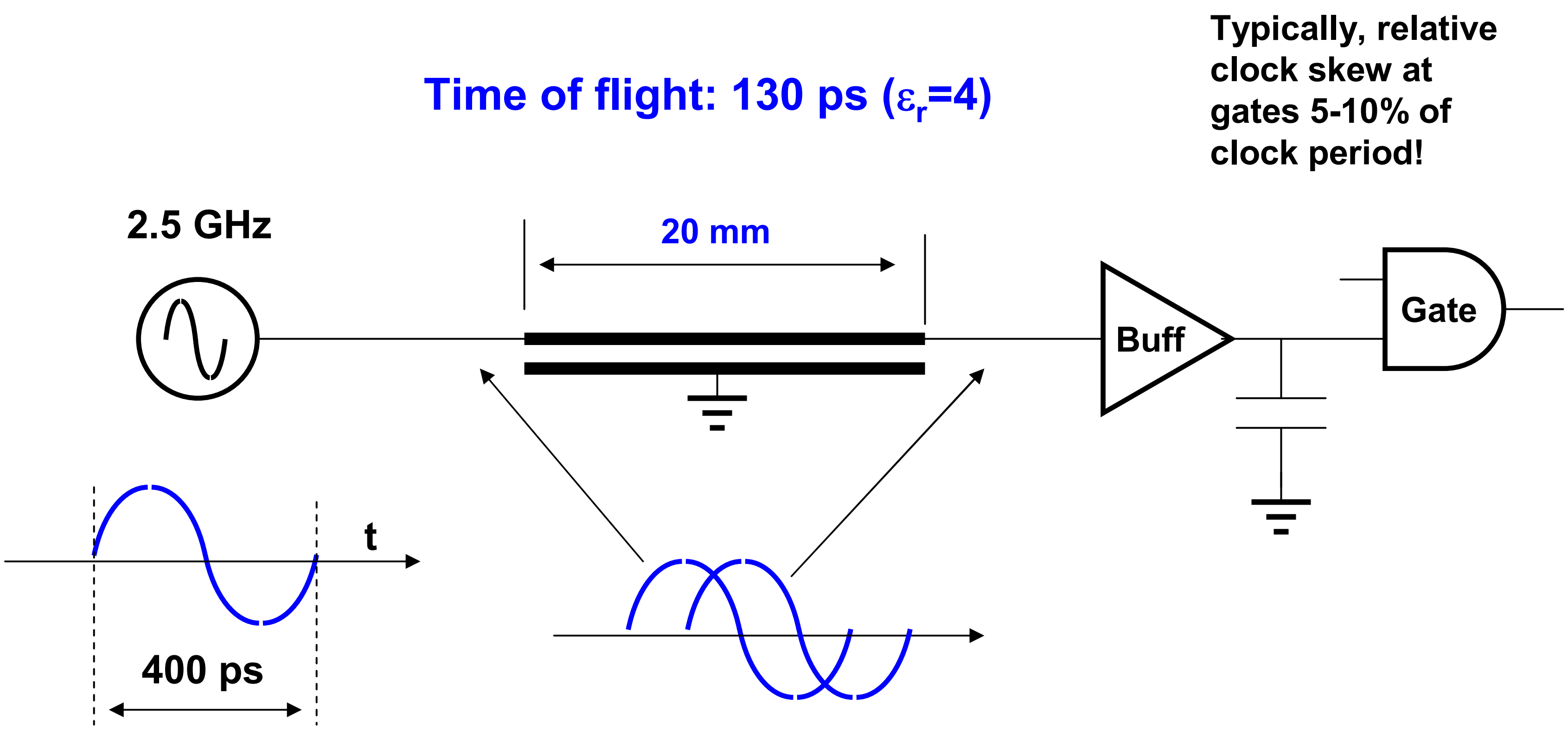
Intel 65 nm Technology
(Intel Website)



Interconnect technology in existing and future IC technologies includes the ingredients for designing high quality TLs: thick metal layers for low losses and wider dielectrics for reasonable characteristic impedance (e.g. 50-100Ω)

Wow, propagation at light speed over a few cm's!
Do we still have to worry about clock synchronization?

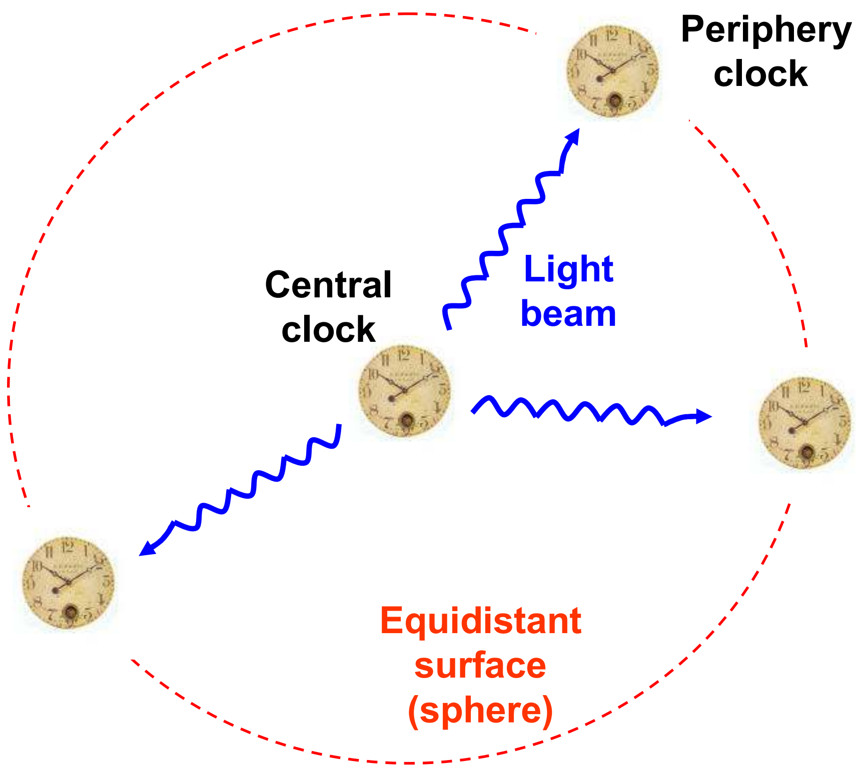
You Bet, if We Want GHz Clocks!



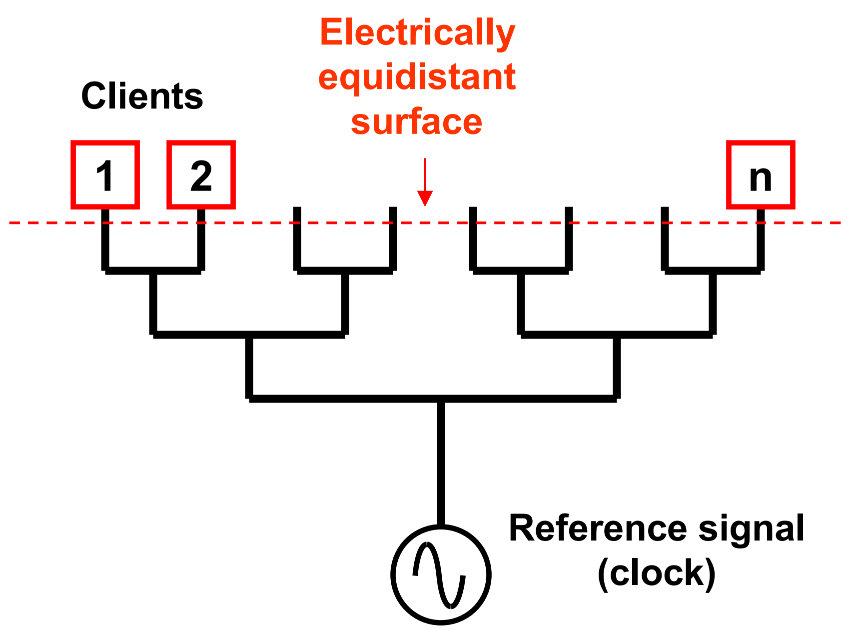
What is the best way to distribute coherent clock signals everywhere on chip using TLs?

A Classical Signal Distribution Method

Poincaré/Einstein Clock Synchronization

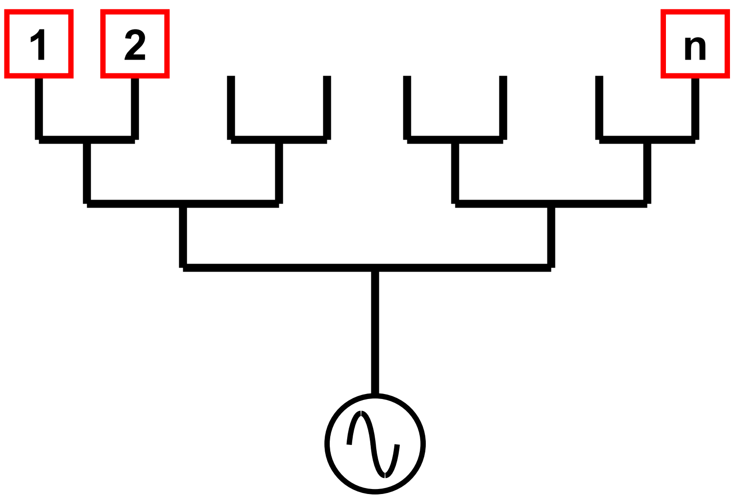


Coherent RF Signal Distribution



Passive Tree or "Corporate Feed"

Passive Tree: Not Practical in VLSI



The Good:

- **Passive transmission**
- **Low loss transmission**
- **Some freedom in geometrical symmetry**

The Bad:

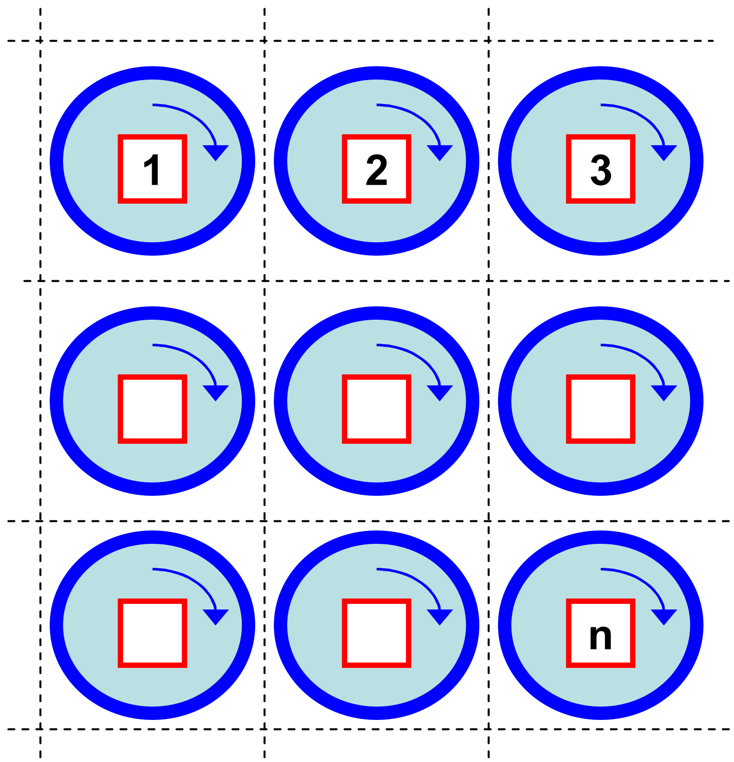
- **Electrical symmetry required**
- **Global load matching required**

The Ugly:

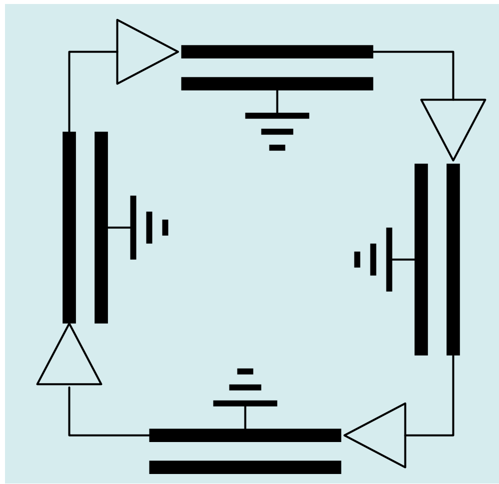
- **Signal splitting and impedance matching (at every node) are major inconveniences and sources of phase/timing errors !!!**

Recent Research Ideas

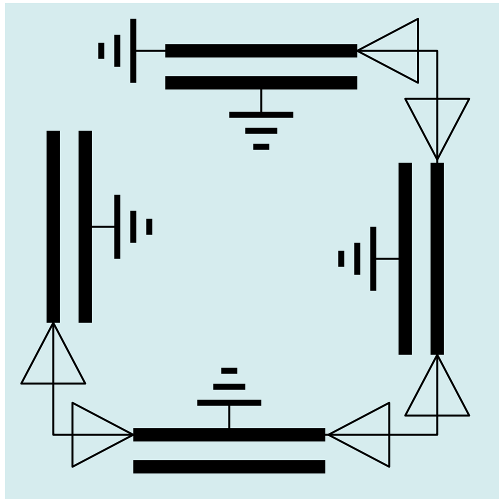
Tiling the IC with T-Line oscillators, mutually coupled at the boundaries



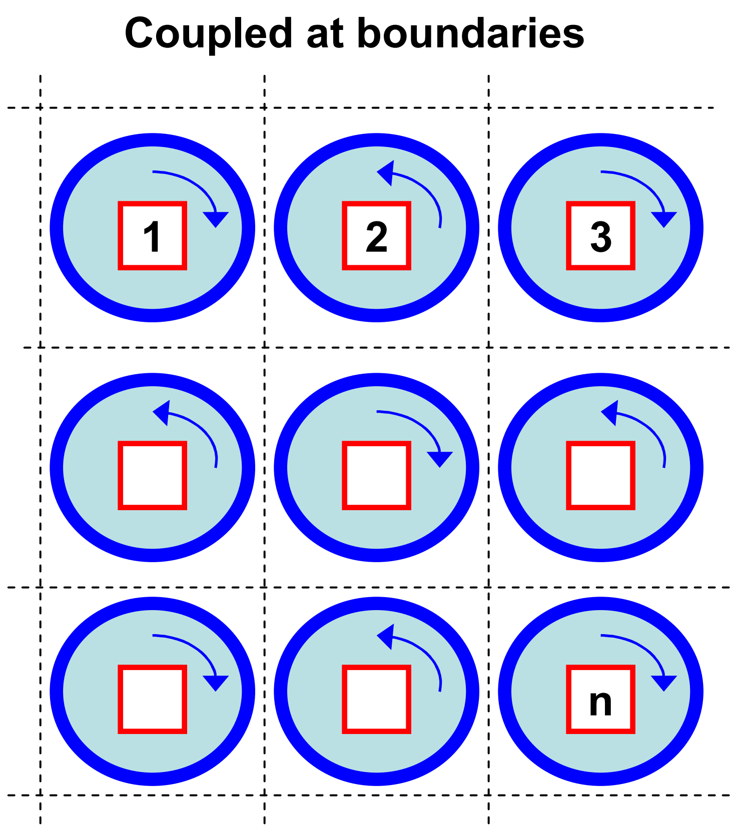
Traveling Wave Oscillator
(John Wood et al)



Standing Wave Oscillator
(Frank O.Mahony et al)



Oscillator Tiling: Nice But …



The Good:

- Low loss transmission
- Excellent jitter/power performance
- Scalable in physical dimensions

The Bad:

- Frequency hard wired and difficult to change/program or modulate for EMI reduction

The Ugly:

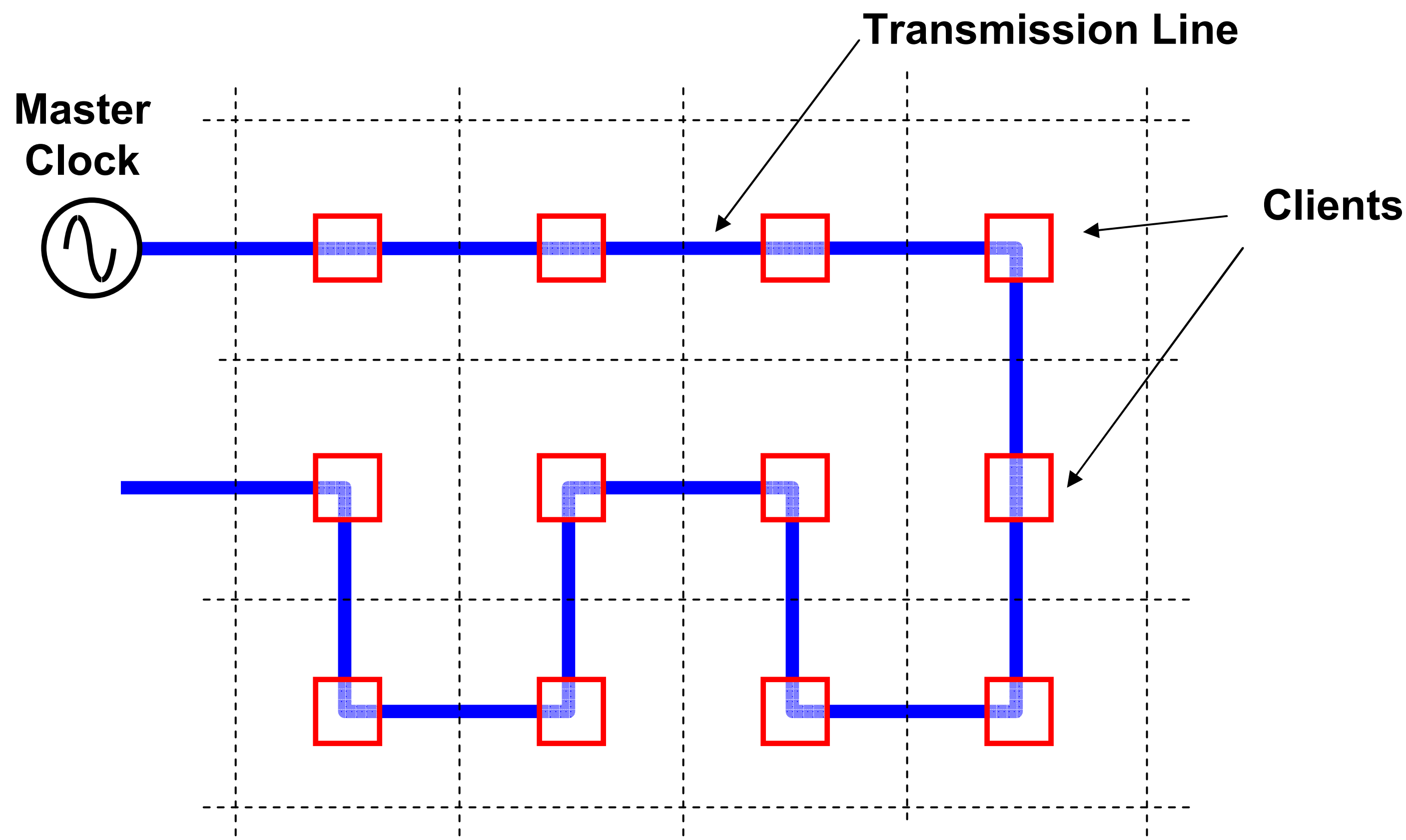
- Design methodology
- Coupled digital noise effects?
- Multiple oscillatory modes?
- Risky! Risky! Risky!

Fundamentally Good Things

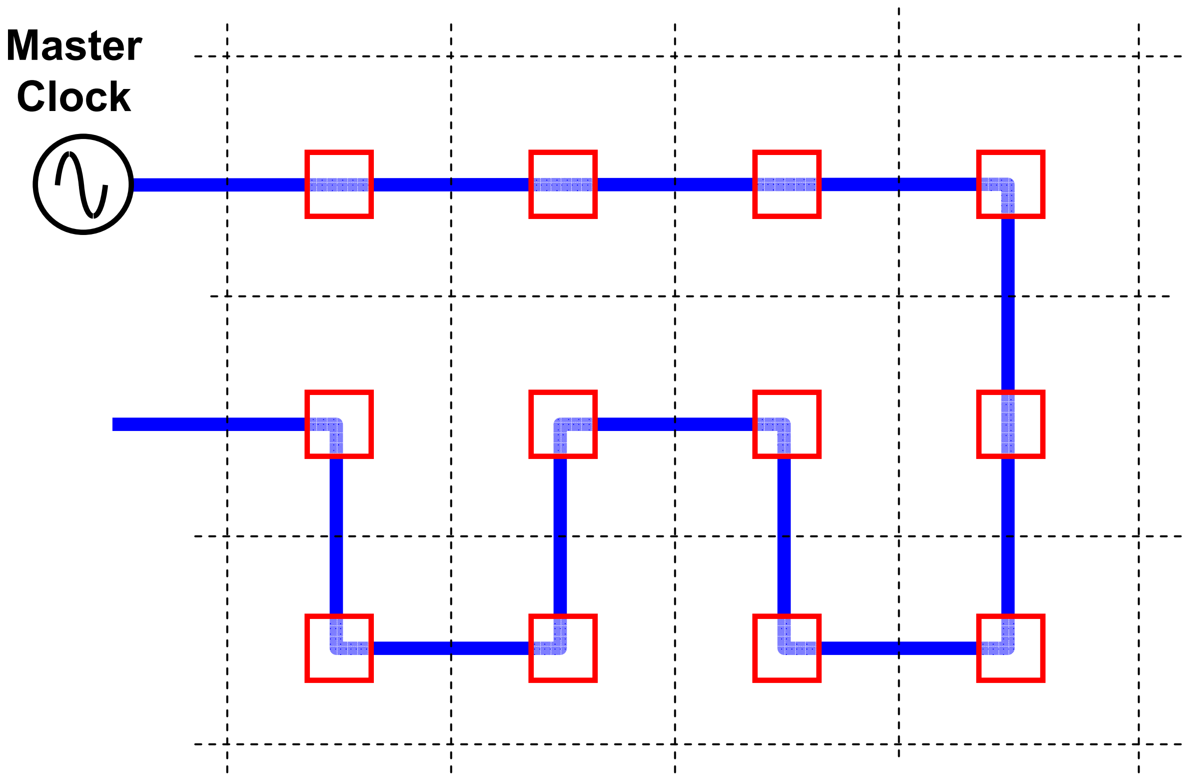
1. **Transmission Line connectivity:** *best for power and jitter*
2. **Serial architecture:** *avoids error prone signal splitting and impedance transformations*
3. **Driven, NOT Autonomous:** allows easy frequency changes and *avoids very hard to model/predict dynamic global interactions*

Let us apply these principles

TL Serial Passive Clock Distribution



Serial Passive With TLs: Almost There



The Good:

- **Simplicity**
- **Simplicity**
- **Simplicity**
- **…**
- **Low jitter**
- **Minimum power**

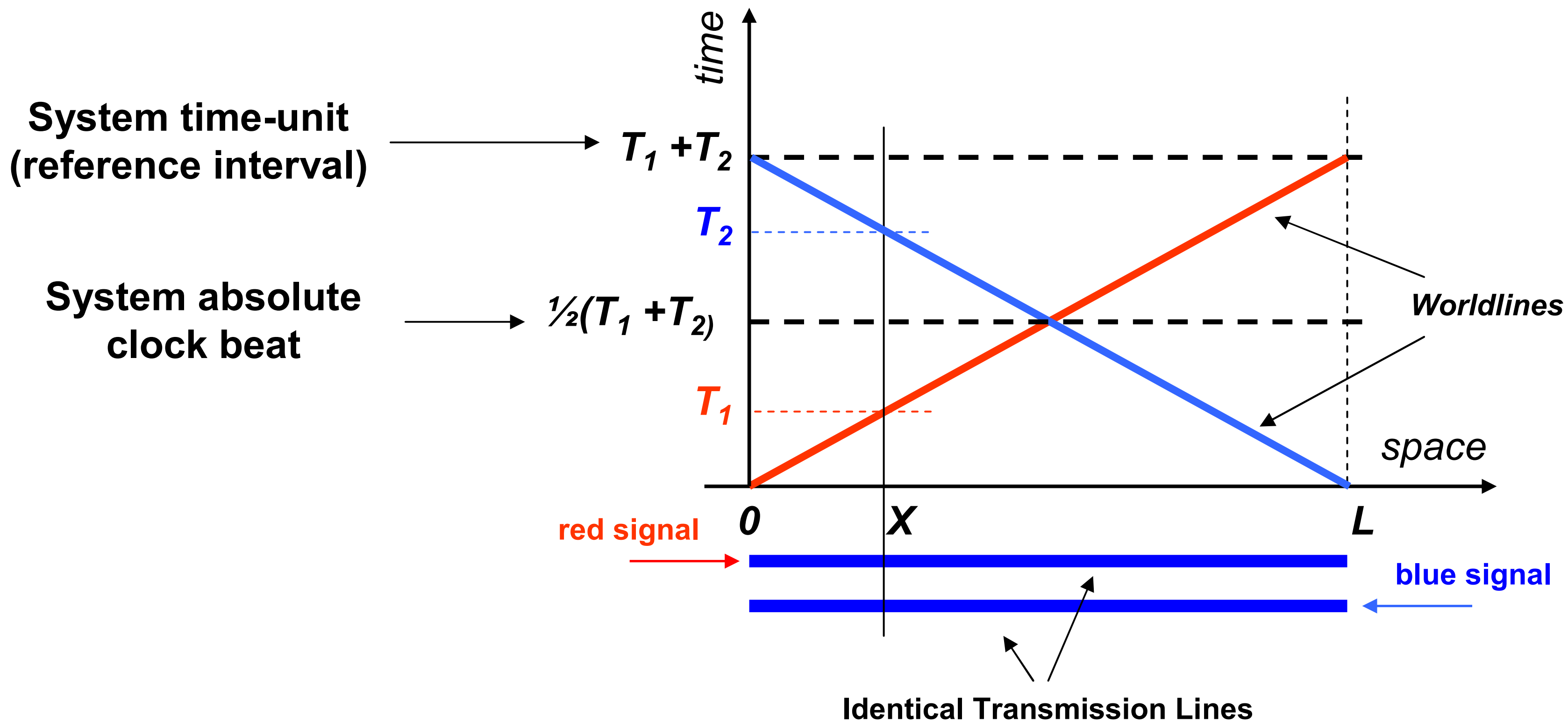
The Bad:

- **Very long TL**

The Ugly:

- **Huge skew (phase) accumulation!**

Bidirectional Signaling (BDS)



IF: **Red and Blue Signals are coherent**

THEN: **The sum of flight-times (T_1+T_2) is <u>independent</u> of position, AND:**
The average of flight-times ½(T_1+T_2) defines an absolute clock beat

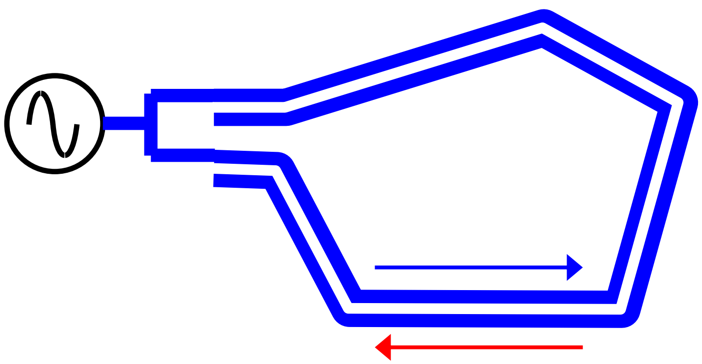
BDS Properties and Practical Issues

- **BDS Properties:**
  - No geometrical constraints on length or shape of the BDS line
  - All points on the BDS line get the global clock-tick information
  - The end-of-line generators of **Blue** and **Red** signals may have arbitrary relative phases

- **Practical Issues for BDS Application to VLSI Clock Distribution**
  - Generation of coherent **Blue** and **Red** signals
  - Circuits for extracting the absolute clock beat from the BDS line

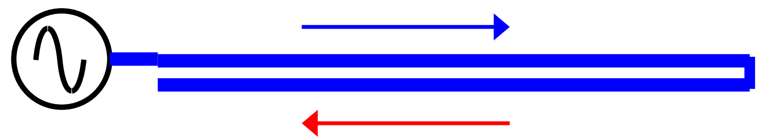
Coherent Blue and Red Signal Generation

BDS Loop
(Return to Origin)



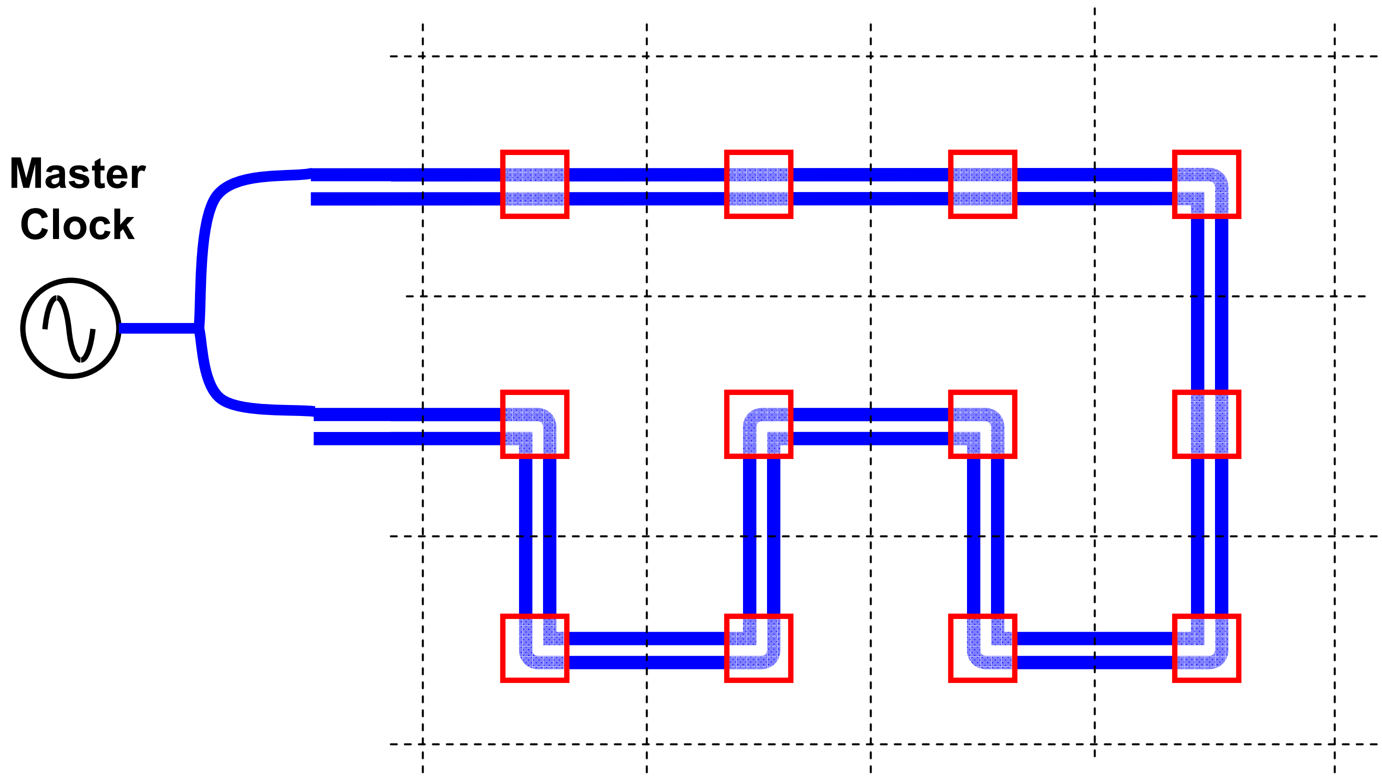
Max Loss	**=**	**x 1**
Length	**=**	**x 2**
Power	**=**	**x 2**

Signal Loopback



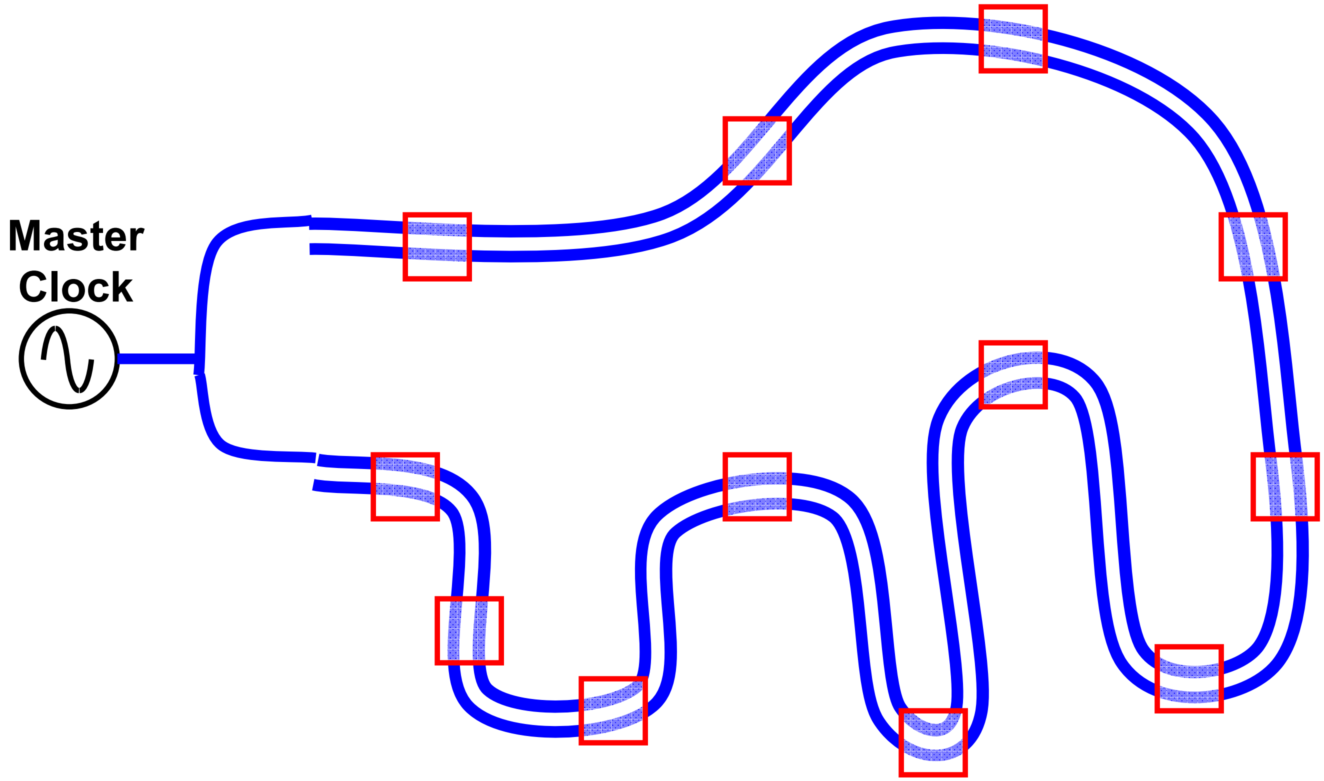
Max Loss	**=**	**x 1**
Length	**=**	**x 1**
Power	**=**	**x 1**

BDS Clock Distribution on "Tile Clients"



What happens if we slide the clients arbitrarily on the BDS line?
What happens if we bend the BDS line arbitrarily in space?

Geometry is Out!

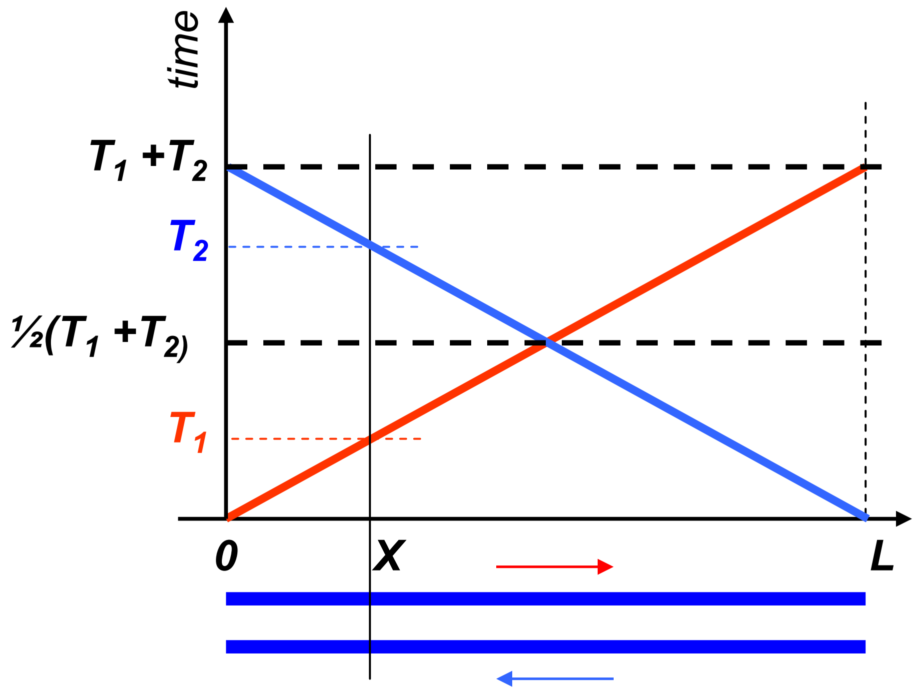


But: How do we extract the clock?

It's Time! No, It's Phase! No, It's …Trigonometry!

$$s_R(x,t) = A_R \sin\left(\frac{2\pi}{\lambda}x - \omega t + \varphi_R\right)$$

$$s_B(x,t) = A_B \sin\left(\frac{2\pi}{\lambda}x + \omega t + \varphi_B\right)$$



T_1 gives a unique red phase at x
T_2 gives a unique blue phase at x

⇒ **Local phases are measures of flight times**

Flight-time addition ⇔ Local phase addition ⇔ Local signal multiplication

Local Multiplication

$$\sin\alpha \times \sin\beta = \frac{1}{2}\left[\cos(\alpha-\beta) - \cos(\alpha+\beta)\right]$$

$$s_R(x,t) \times s_R(x,t) =$$

$$= A_R \sin\left(\frac{2\pi}{\lambda}x - \omega t + \varphi_R\right) \times A_B \sin\left(\frac{2\pi}{\lambda}x + \omega t + \varphi_B\right)$$

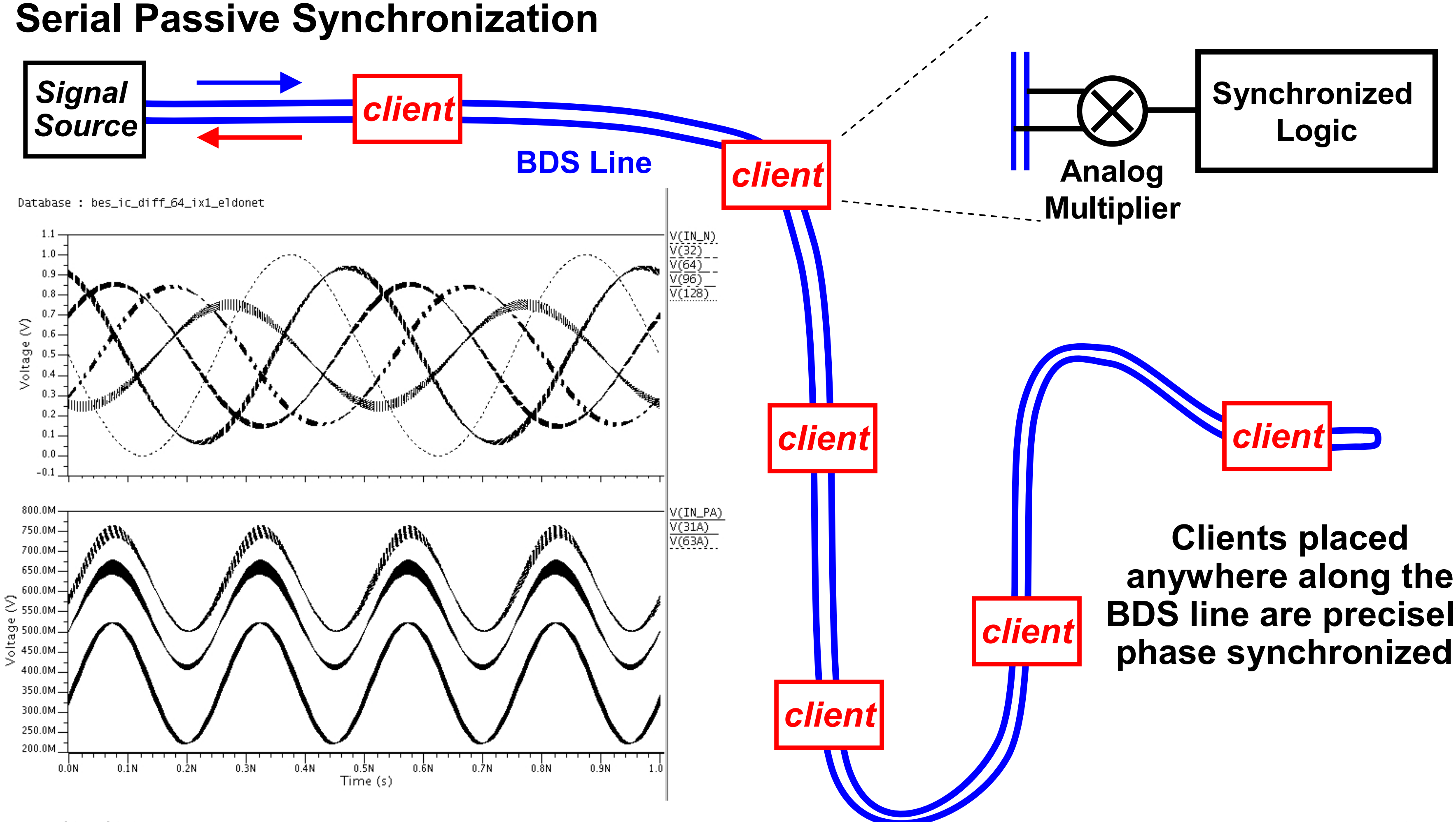
$$= \underbrace{\frac{1}{2}A_R A_B \cos(2\omega t + \varphi_R - \varphi_B)}_{\text{Global Clock Signal}} + \underbrace{\frac{1}{2}A_R A_B \cos\left(\frac{4\pi}{\lambda}x + \varphi_R + \varphi_B\right)}_{\text{DC Component}}$$

Global Clock Signal
- At twice the BDS frequency
- Phase independent of BDS magnitude and loss!

DC Component
- Position dependent
- Easily eliminated in practice

BDS Clock Distribution

Inexpensive, high performance, multi-point Serial Passive Synchronization

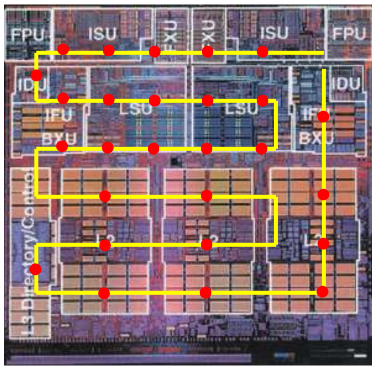


Clients placed anywhere along the BDS line are precisely phase synchronized!

BDS Advantage

Simplified Montecito Clocking System

PLL → L0 → dividers → L1 → Ph/skew align → L2 → Open-loop final path

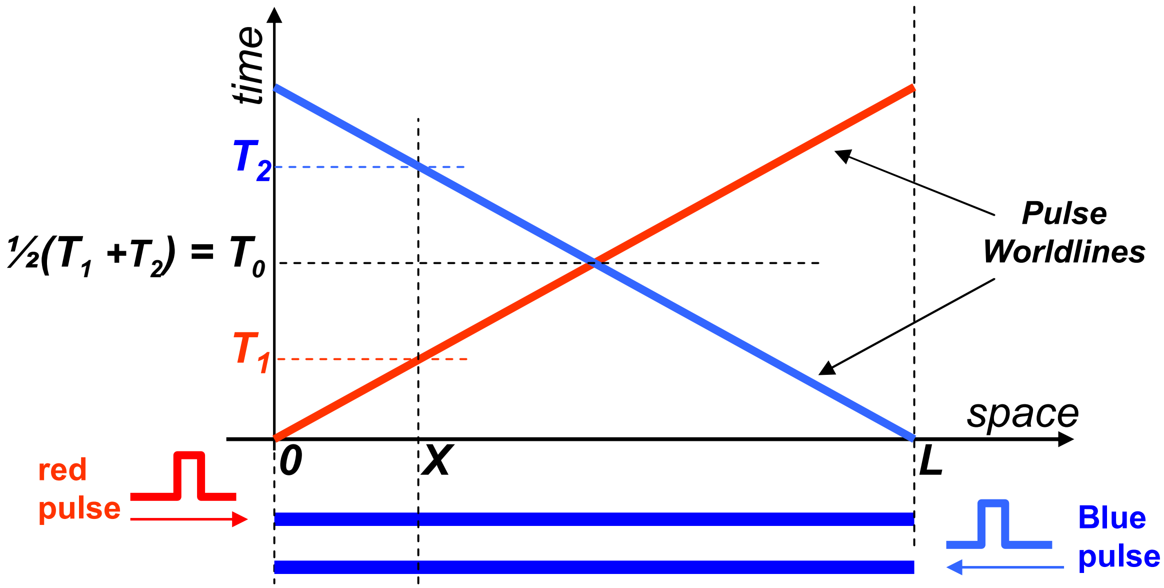


Route	Fan-out	Unit area (estimate)	Distance	Power	Delay
L0	14	5mm x 5mm	20mm	600mW	640ps
L1	71	2.5 mm x 2.5 mm	5mm	700mW	215ps
L0 & L1	71	2.5 mm x 2.5 mm	20mm	1300mW	855ps

Replacing L0 and L1 with BDS Technology

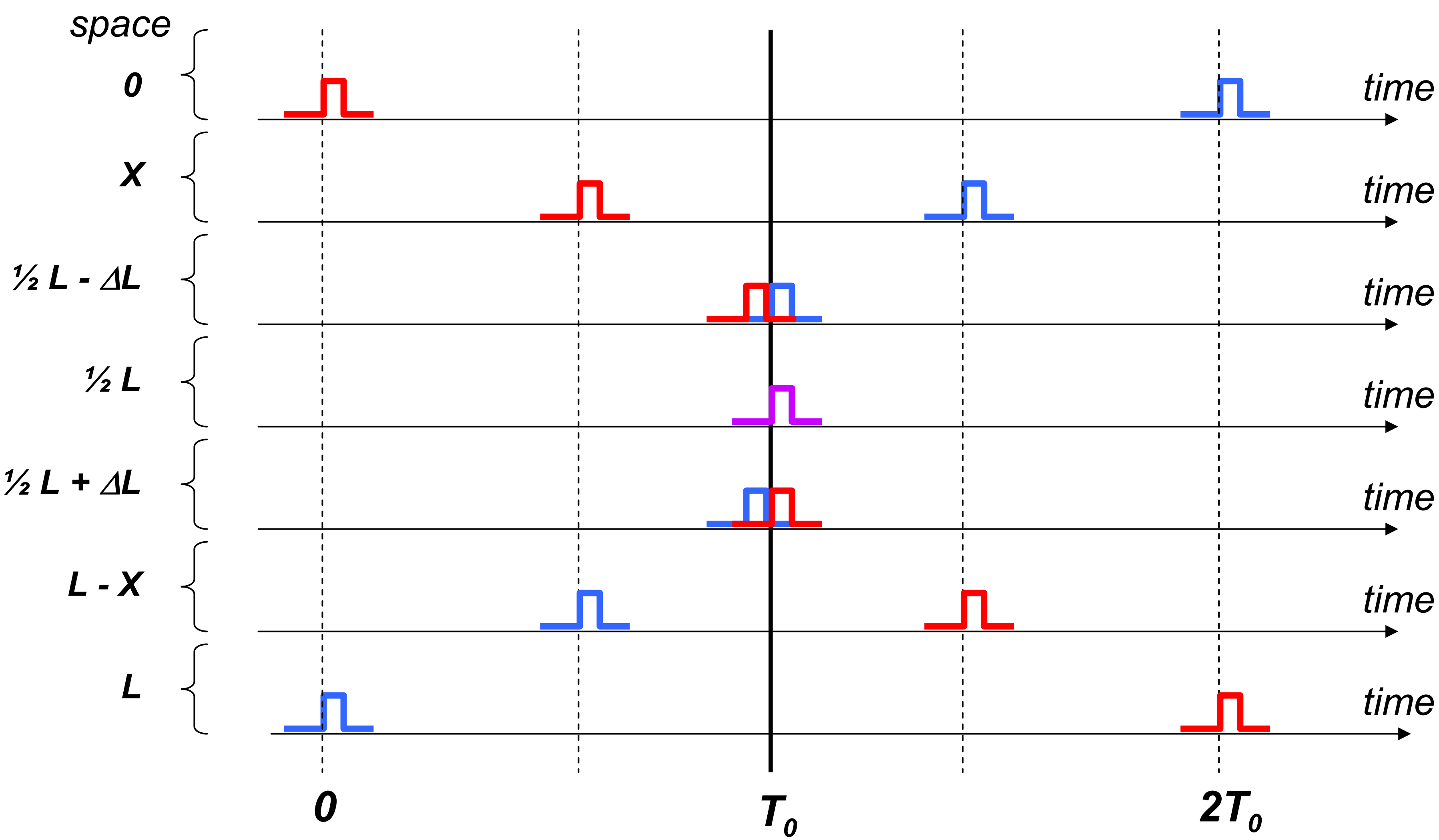
Route replaced	Architecture	BDS line length	Line z_0	Fan-out	Unit area clocked	Power (2V p-p diff signal)	Delay
L0	4 BDS	20mm	100Ω	16	5mm x 5mm	40mW	100ps
L0 & L1	16 BDS	20mm	100Ω	64	2.5 mm x 2.5 mm	200mW	200ps
L0 & L1	16 BDS	40mm	100Ω	256	1.25 mm x 1.25 mm	200mW	200ps

Pulsed BDS

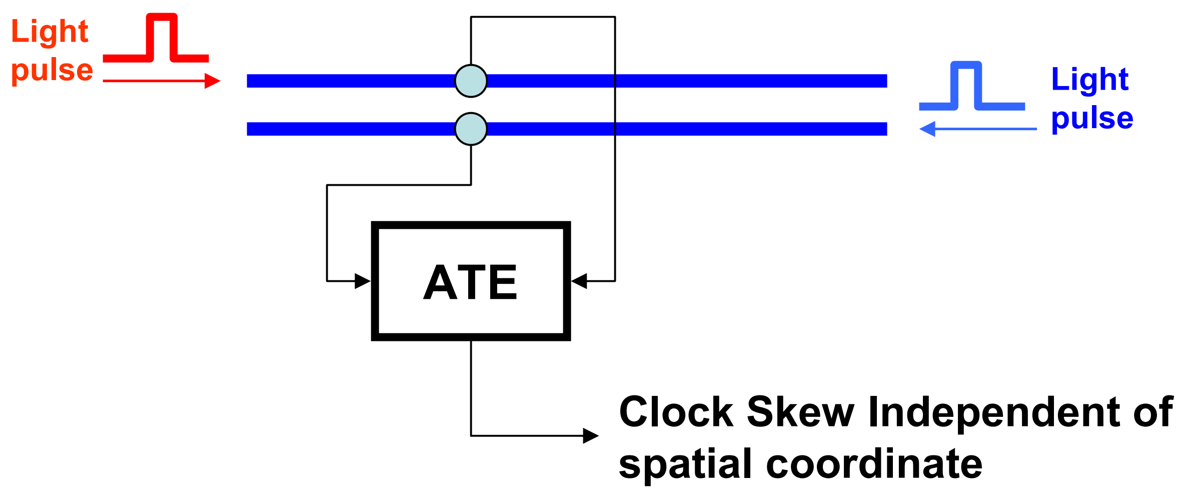


- The average between the pulse arrival times in the two lines, $T_0=½(T_1+T_2)$ is <u>independent</u> of X

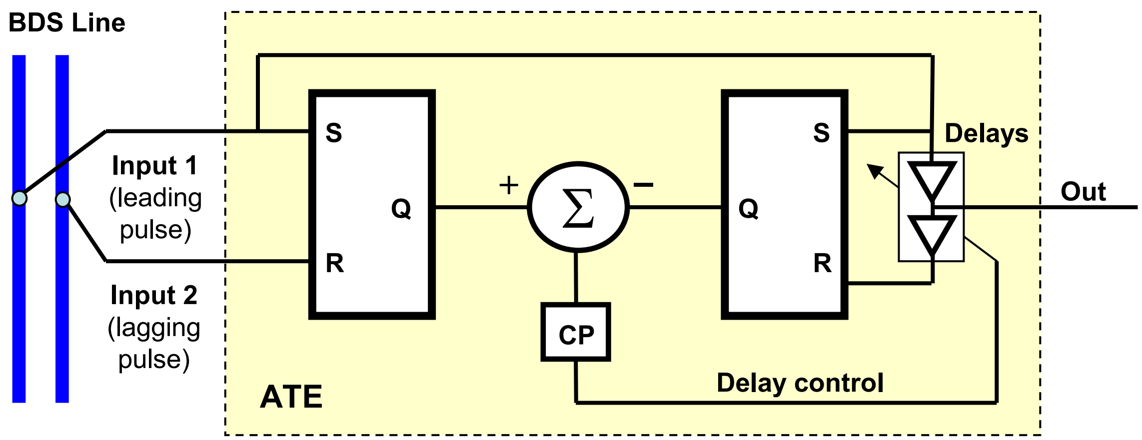
Pulse Pattern by Spatial Coordinate



Average Time Extractor (ATE)

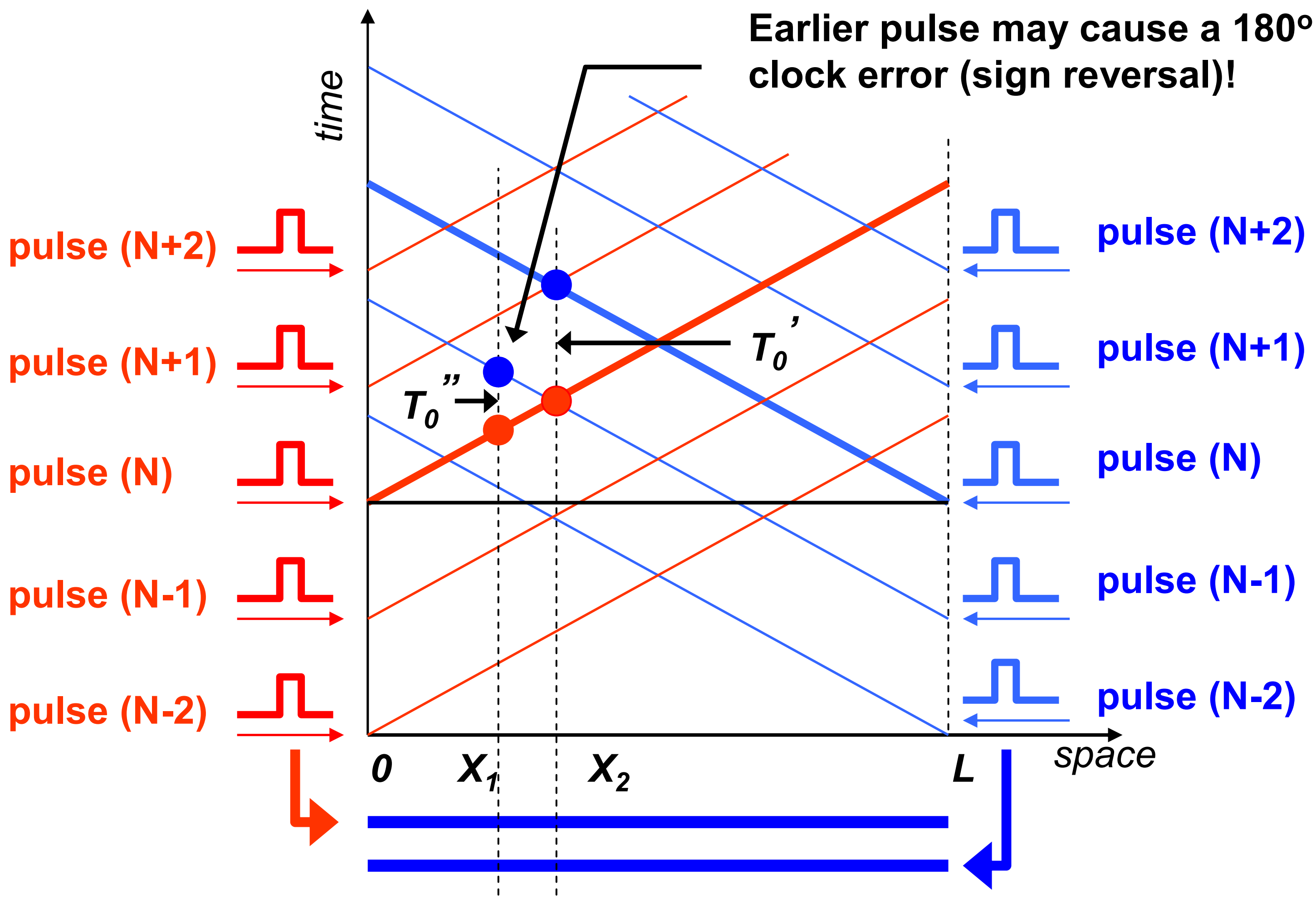


An ATE Example

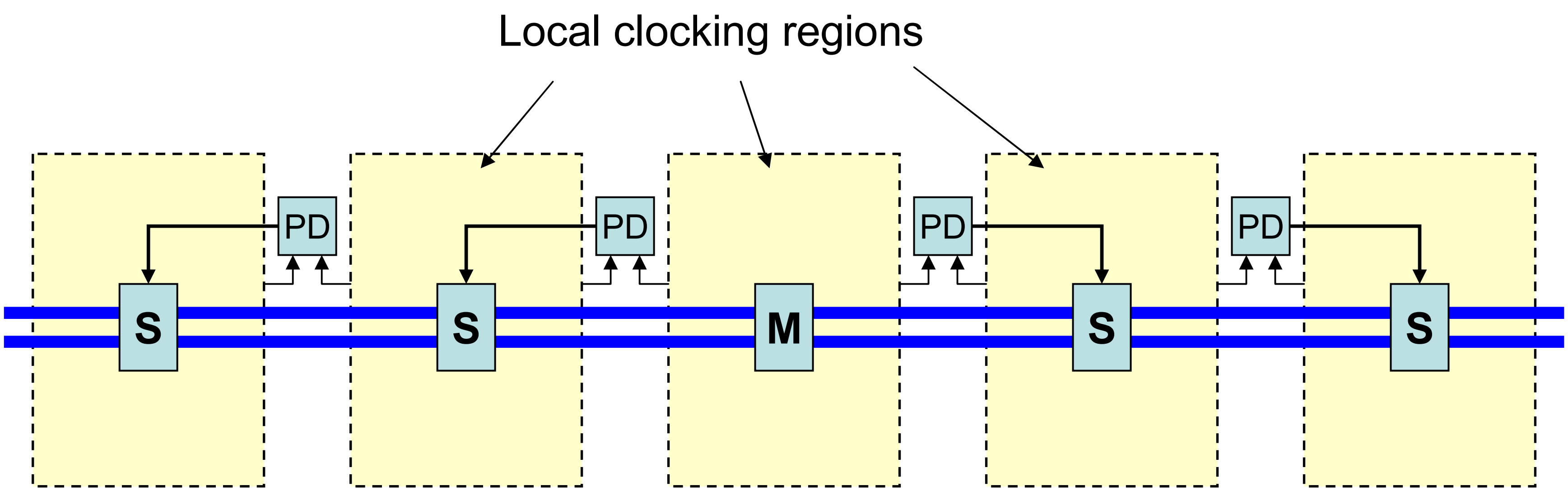


- Similar in architecture and performance to conventional DLL circuits
- Several variations possible based (DLL or PLL based)
- Susceptible to pulse shape distortion and other practical errors

Pulsed-BDS Sign Ambiguity



DC Phase Alignment for Pulsed-BDS



- Master and all Slaves generate local clocks using BDS, subject to sign ambiguity
- Phase detectors at the local clocking boundaries determine if clock sign reversal is needed and control the next Slave down the chain through a DC line
- Correct functionality is guaranteed because within local clocking regions clock skew must be small by design
- Same scheme automatically supports clock slow-down functionality

Conclusions

- New BSD concept (several patent applications) provides a most efficient and flexible method for clock distribution on large VLSI chips
- Theoretically, the BDS system performance is superior to active trees in terms of speed, skew, jitter, and power dissipation, mostly due to passive serial wave guide transmission
- BDS is a driven wideband system, easy to start/stop or operate at arbitrary frequencies within a wide range
- The simplest and most efficient BDS implementation uses sinusoidal signaling and analog multipliers for clock extraction
- Pulsed BDS is possible using conventional PLL/DLL circuit technology
- BDS: a new paradigm in clock distribution simplicity and capability for automatic implementation by a CAD tool.