Survey of Emerging Memory Technologies

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Agenda

- The Search for a Universal Memory
- Ferroelectric Memory (FeRAM)
- Magnetoresistive Memory (MRAM)
- Phase Change Memory (PCRAM)
- Other Emerging Memory Technologies
- Concluding Remarks

Contemporary Memory Options

	DRAM	SRAM	Flash
Relative Density	6 - 12 F^2	50 to 80 F^2	7 - 11 F^2
Nonvolatility	No	No	Yes
Read Cycle Time	< 60 ns	< 10 ns	< 80 ns
Write Cycle Time	< 60 ns	< 10 ns	> 5 µs
Endurance	"Infinite"	"Infinite"	$< 10^6$
Compatibility with CMOS	Awkward (Requires extra cost and/or performance compromises)	Yes	Yes (But with a high voltage and not at the latest node)

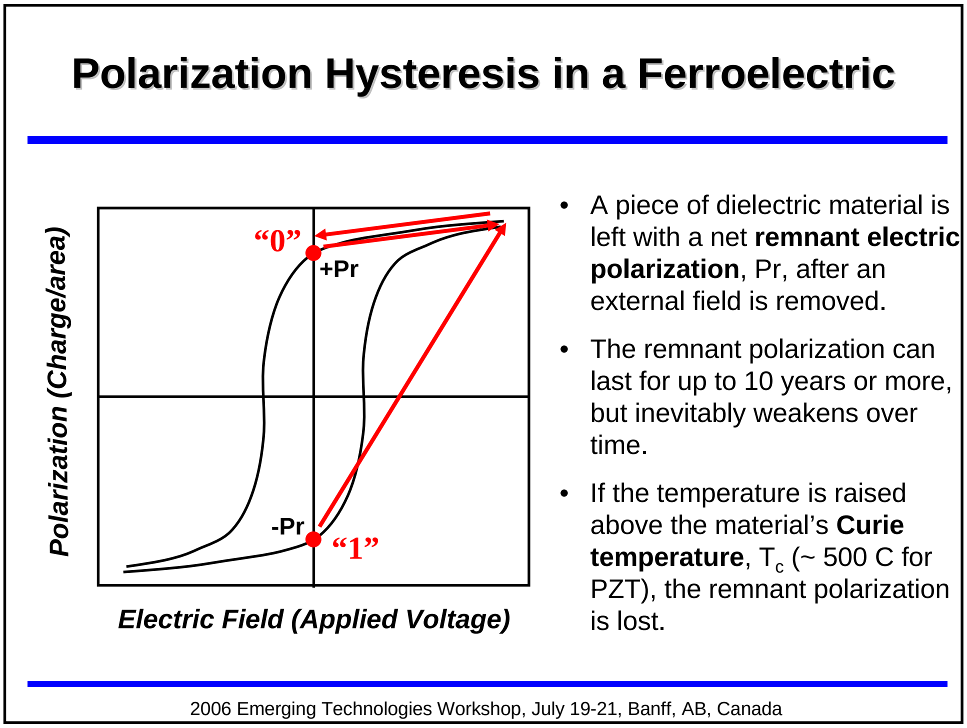
The Search for a Universal Memory

Large financial rewards await any company that can deliver a "universal" memory technology that has:

- ***Density*** approaching that of DRAM (e.g. 6 - 12 F^2)
- ***Speed*** approaching that of SRAM (e.g. < 35 ns)
- ***Nonvolatility*** with at least 10 years retention at 85C
- ***Endurance*** exceeding 10^{12} write-erase cycles
- ***Embeddability***, at reasonable additional cost, in a standard foundry CMOS logic process
- ***Scalability*** for several more process generations

Ferroelectric Memory (FeRAM)

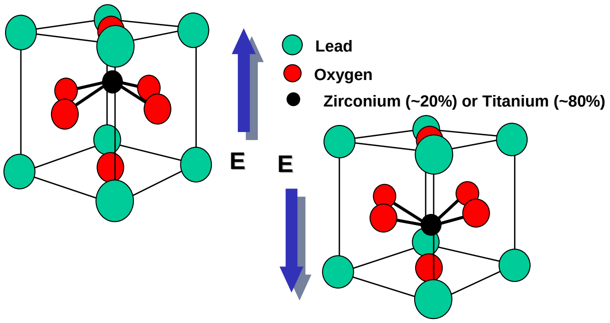
- Exploit the **polarization hysteresis** property of ferroelectric materials.
- The ferroelectric material is deposited as a thin film forming part of a capacitor's dielectric.
- Two polarization states can be written and read.
- Various materials have been considered, e.g.:
  - lead zirconate titanate (PZT): $Pb(Zr,Ti)O_3$
  - strontium bismuth tantalate (SBT): $SrBi_2Ta_2O_9$
  - barium strontium titanate (BST): $Ba_xSr_{1-x}TiO_3$



Polarization Hysteresis in a Ferroelectric

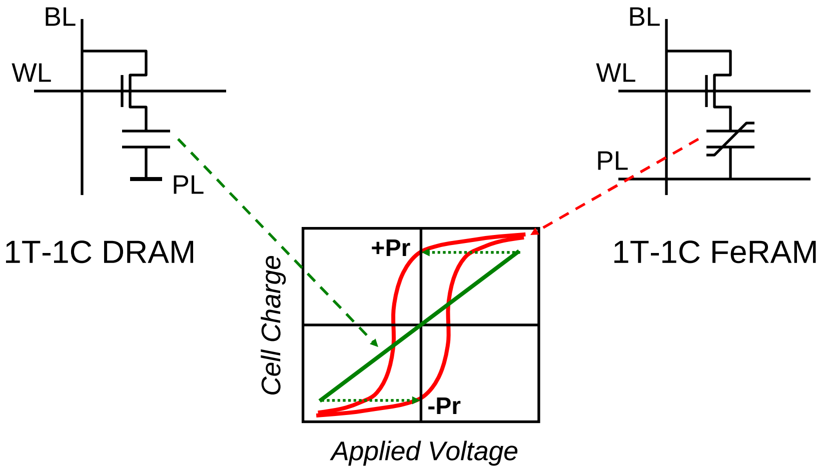
- A piece of dielectric material is left with a net **remnant electric polarization**, Pr, after an external field is removed.
- The remnant polarization can last for up to 10 years or more, but inevitably weakens over time.
- If the temperature is raised above the material's **Curie temperature**, T_c (~ 500 C for PZT), the remnant polarization is lost.

Polarization Hysteresis in PZT

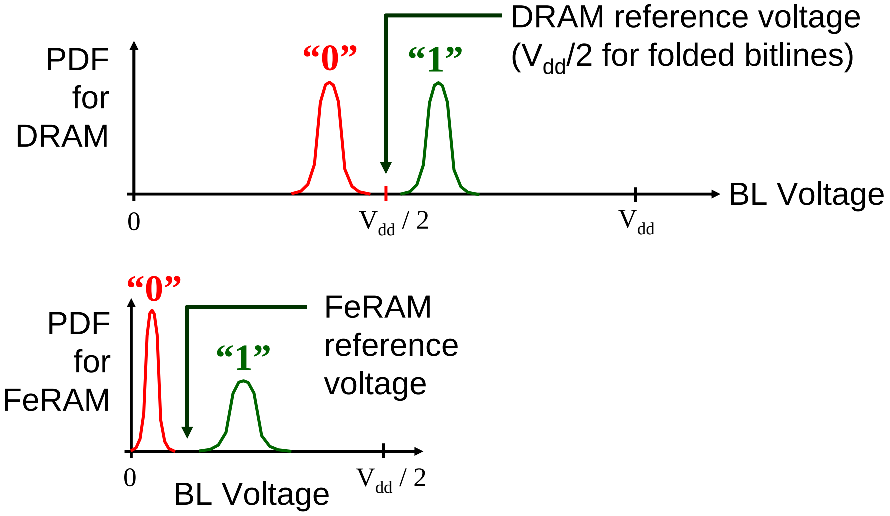


- Each cell of the cubic crystal lattice has an inherent electric dipole, which is the lowest energy state.
- The cells in a domain have aligned electric dipoles.

1T-1C DRAM and FeRAM Cells

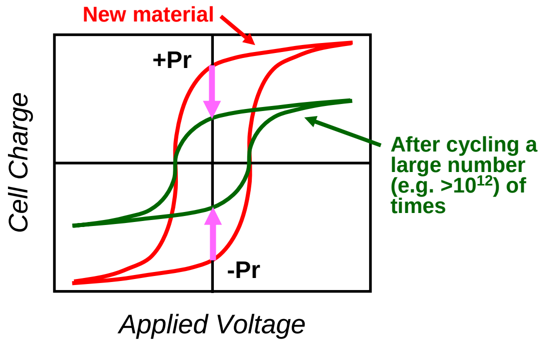


Bitline Signals in DRAM and FeRAM



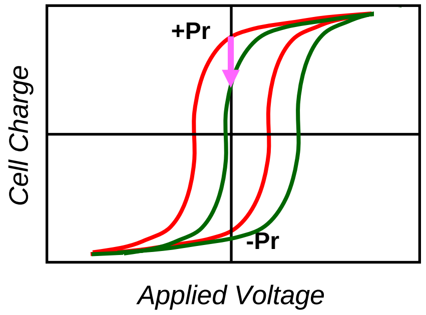
Fatigue in FeRAM

- **Fatigue:** **loss in polarization strength after many polarization reversals. The read signal from the Fe capacitor becomes weaker for both 0s and 1s.**



Imprint in FeRAM

- **Imprint:** **distortion/shift in hysteresis loop with fixed data. After a 0 (1) has been stored or repeatedly written for a long time, the signal produced by a newly written 1 (0) is weaker than it was in the original Fe cap.**



"1" stored in a cell for a long Time ⇒ "0" is recorded with a weak signal.

Recent Production FeRAMs

Feb. 2000: Ramtron FM1808 256-Kbit byte-wide 2T/2C
- 70 ns access time; 130 ns cycle time
- 10 year data retention
- 10^{10} write-erase endurance

Dec. 2001: Ramtron FM24C256-SE 256-Kbit serial 1T/1C
- data accessed over two-wire, 1-MHz serial bus
- 10 year data retention

Nov. 2004: Fujitsu MB85R1001&2 1-Mb, 128Kx8 & 64Kx16
- 100 ns access time, 250 ns cycle time
- 10^{10} write-erase endurance
- >10 years retention up to 85C

Recent 1T/1C FeRAM Prototypes

Year	*Density*	*Speed*	*Process*	*Company*
1998	**1 Mbit**	**?**	**0.6 μm**	**Ramtron & Fujitsu**
1998	**1 Mbit**	**< 80 ns**	**0.5 μm**	**Toshiba**
2000	**4 Mbit**	**?**	**0.4 μm**	**Samsung**
2001	**8 Mbit**	**< 70 ns**	**0.25 μm**	**Toshiba**
2002	**32 Mbit**	**45 ns**	**0.25 μm**	**Samsung**
2002	**32 Mbit**	**50 ns**	**0.2o μm**	**Infineon & Toshiba**
2003	**64 Mbit**	**30 ns**	**0.13 μm**	**TI & Ramtron**
2005	**4/8 Mb**	**?**	**0.13 μm**	**TI & Ramtron**

Magnetoresistive Memory (MRAM)

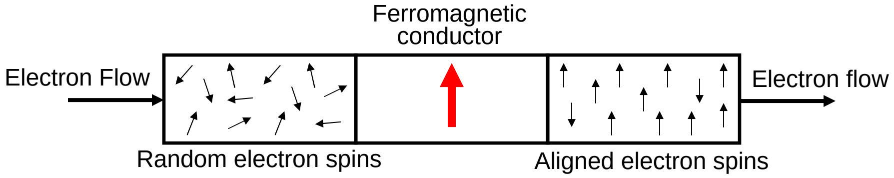
- Magnetism has been used for many years as the basis for nonvolatile data storage devices:
  - Core memory (early mainframes, the space shuttle, etc.)
  - Tape drives
  - Hard and floppy magnetic discs
  - Magnetic bubble memory
- Magnetoresistive memory (MRAM) is a new generation of much faster magnetic memory that is compatible with semiconductor integrated circuit technology.
- MRAM technology is being developed by several companies: Freescale, IBM & Infineon, Honeywell, STMicroelectronics, Samsung, etc.

Magnetic RAM Technologies

- Several different magnetic RAM technologies have been proposed over the years:
  - Anisotropic MRAM
  - Spin Valve MRAM
  - Pseudo-Spin Valve MRAM
  - Magnetic Tunnel Junction (MTJ) MRAM
  - Toggle-mode MTJ MRAM
- Toggle MTJ MRAM seems to have the best potential.
- Understanding MTJ MRAM operation requires understanding of some basic properties of spin-polarized current.

Spin-Polarized Current

- The spin of the electrons making up the current in most electronic devices is irrelevant to circuit operation.
- However, spin is a property that can potentially be controlled and exploited to make useful new devices
  ⇒ an emerging field called “spintronics”
- The spin of the moving electrons tends to line up with an environment of aligned spin, like the magnetic field present in a piece of polarized ferromagnetic material.



Ferromagnetic conductor

Electron Flow

Electron flow

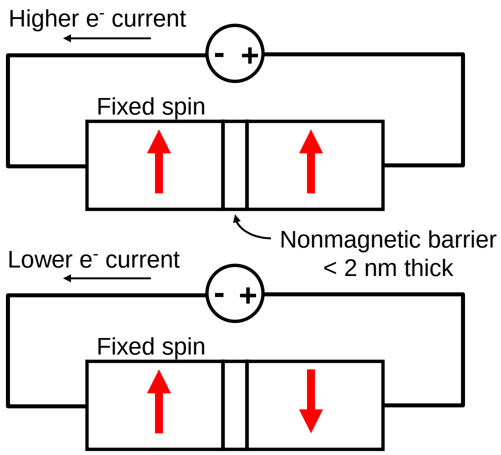
Random electron spins

Aligned electron spins

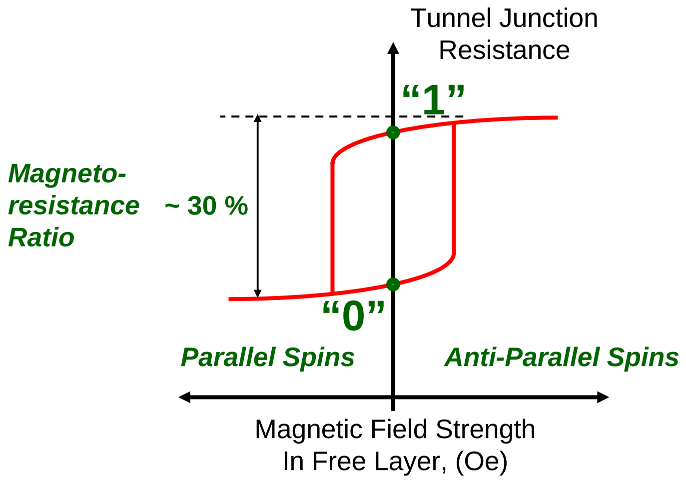
The Magnetic Tunnel Junction

1) Parallel Spins
   - lower barrier to tunneling current
   - > 30% resistance drop
   - higher current

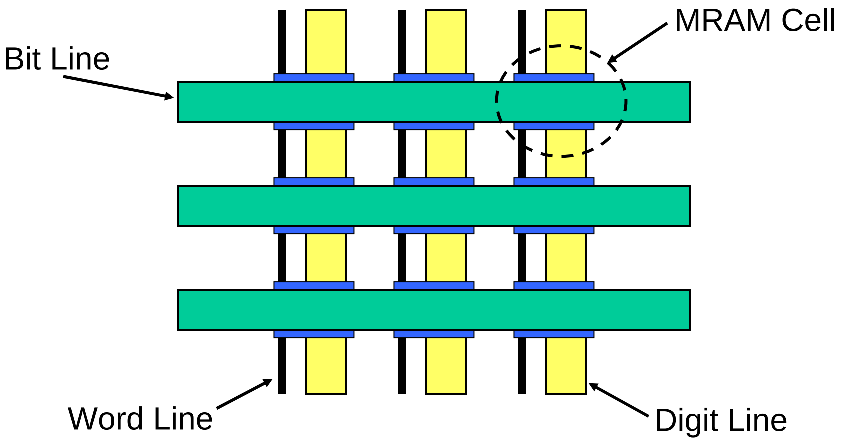
2) Anti-parallel Spins
   - higher barrier to tunneling current
   - lower current



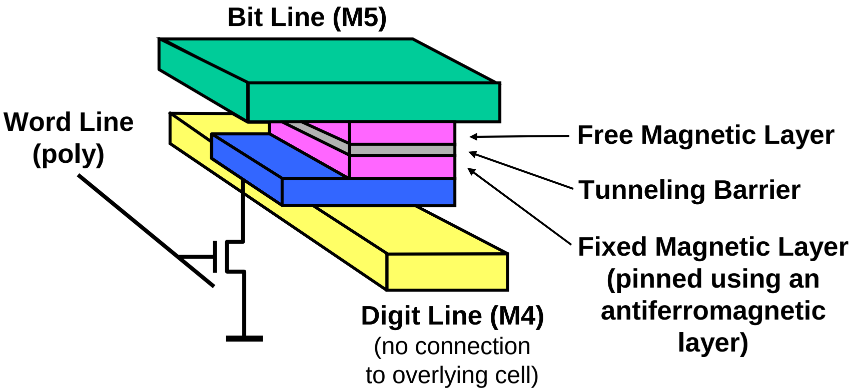
MRAM Cell Hysteresis



MRAM Cell Array

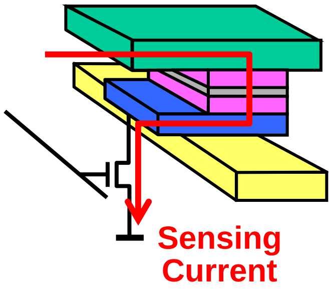


Structure of Freescale's MRAM Cell

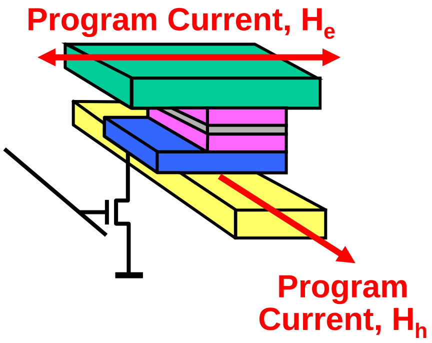


Basic Cell Operations

Cell Sensing

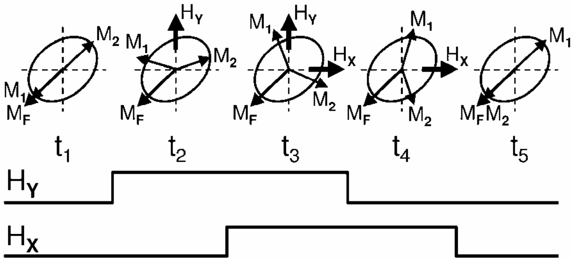


Cell Programming



Toggle-mode MTJ MRAM

- A toggle mode cell is shaped to allow magnetizations only along an axis at 45° to the orthogonal control currents.
- The free layer is formed using as a synthetic anti-ferromagnet with roughly antiparallel magnetizations M_1 and M_2.



M_F = magnetization of fixed layer
M_1 = magnetization in 1st free layer
M_2 = magnetization in 2nd free layer
H_X = magnetic field produced by I_Y
H_Y = magnetic field produced by I_X

Reported MJT MRAM Prototypes

Year	*Density*	*Speed*	*Process*	*Company*
2000	**512 bit**	**14 ns**	**0.6 μm**	**Motorola**
2000	**1 Kbit**	**3 ns**	**?**	**IBM**
2001	**256 Kbit**	**< 50 ns**	**?**	**Motorola**
2002	**1 Mbit**	**50 ns**	**0.6 μm**	**Motorola**
2003	**4 Mbit**	**35 ns**	**0.18 μm**	**Freescale**
2004	**256 Mbit**	**?**	**0.13 μm**	**IBM & Infineon**
2004	**16 Mbit**	**30 ns**	**0.18 μm**	**Altis**

Major Challenges Facing MRAM

- Creating uniform, ultrathin (< 2 nm thick) tunneling barriers in a mass production environment.
- Integration of new magnetic materials into a standard CMOS logic process.
- Reliability concerns related to possible disturb interactions among adjacent cells.
- Relatively high currents (e.g. 3.44-mA rd; 6.56-mA wr).
- Relatively large cell size (comparable to an SRAM cell).

Phase Change Memory (PCRAM)

- PCRAM exploits thermally reversible changes in the crystal structure of chalcogenide glass, with chemical structure $Ge_xSb_yTe_z$.

  Note: chalcogens = Group VI elements
  = { O, S, Se, Te, Po }

- A variety of applications of chalcogenide glass have been developed over the past 30 years.
- Chalcogenide glass is a recording medium widely used in re-writeable CDs and DVDs.

Properties of Chalcogenide Glass

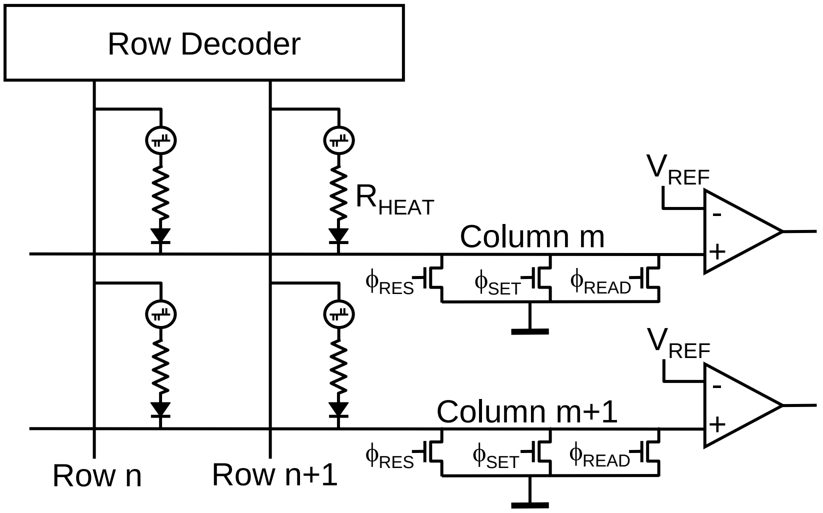
Heat to >600 C (melting point), then cool rapidly to avoid crystallization.

⇒ high-resistance amorphous state

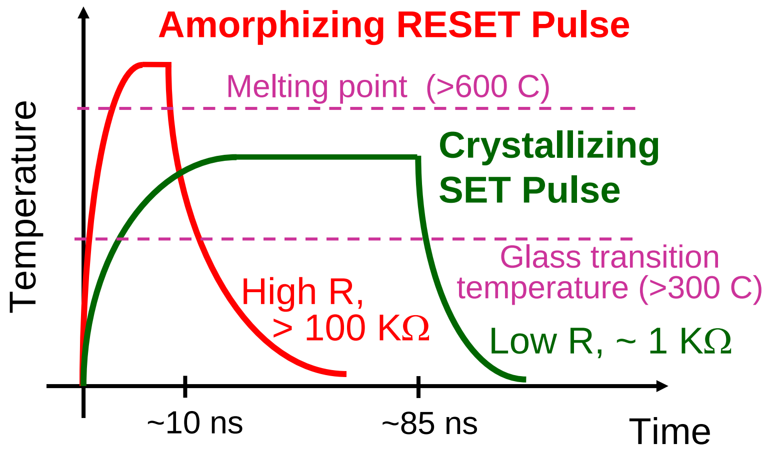
Heat to >300 C (glass transition temp.) and <600 C, then cool more slowly to permit crystallization.

⇒ lower-resistance (100 x) polycrystalline state

PCRAM Cell Array



Time-Temperature Relationship



Major Challenges Facing PCRAM

- Materials selection and cell design to ensure fast and reliable switching using minimum-sized transistors.
- Integration of chalcogenide and other new materials into a standard CMOS logic process.
- Reliability concerns related to possible thermal disturb due to read operations to the addressed cell and due to operations directed to nearby cells.

Other Emerging Memory Technologies

- Polymer memory
- 3-D holographic memory based on organic dyes
- Micromechanical memories (e.g. micro-stylus)
- Nanotechnology-based memories (e.g. nanotubes)
- Thyristor-based memory (requires refresh)
- Memories that exploit the floating body effect in SOI

Concluding Remarks

- All of the candidates for “universal memory” face a difficult challenge making headway against the incumbent combination of DRAM, SRAM and flash memory.
- The new memories must solve technical challenges (e.g. integration of new materials) with much smaller R&D budgets against the still-improving incumbent RAMs.
- As with previous “disruptive” technologies, the new memories must find a profitable niche where their properties give them a compelling advantage against the established technologies that offsets their higher cost.
- Potential niche markets: low power, metering, automotive, high-speed SRAM replacement, SOC universal memory

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FeRAM, MRAM & PCRAM Prototypes