



All Digital Spread Spectrum Clock Generator For EMI Reduction

Presenter: Simon Damphousse
Kelowna Design Center
July 2006

ESS Technology, Inc



Audio



Video



Imaging





Outline

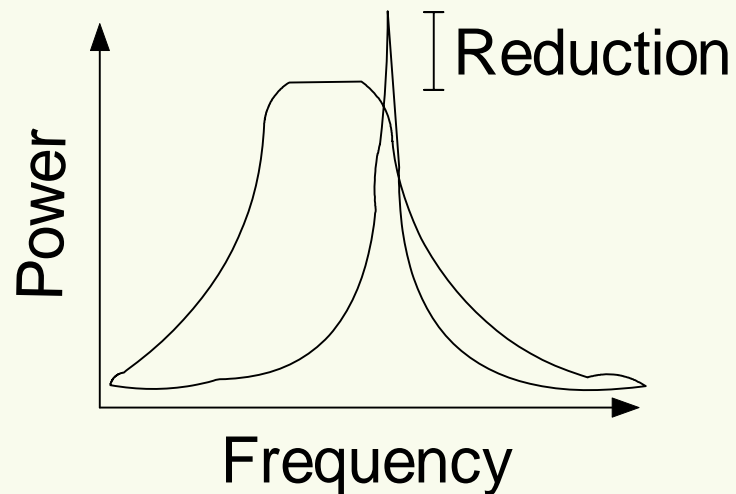
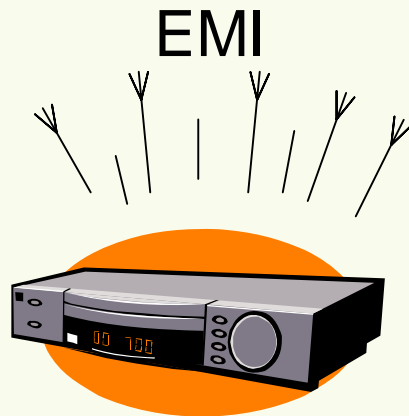
- Introduction on the purpose of the SSCG circuit.
- Commonly used methods for design.
- Proposed method to generate the SSCG.
- Details on implementation of the SSCG.
- Typical implementation and advantage.
- Measured results of the SSCG.
- Conclusion and acknowledgements.





Purpose of the SSCG Circuit

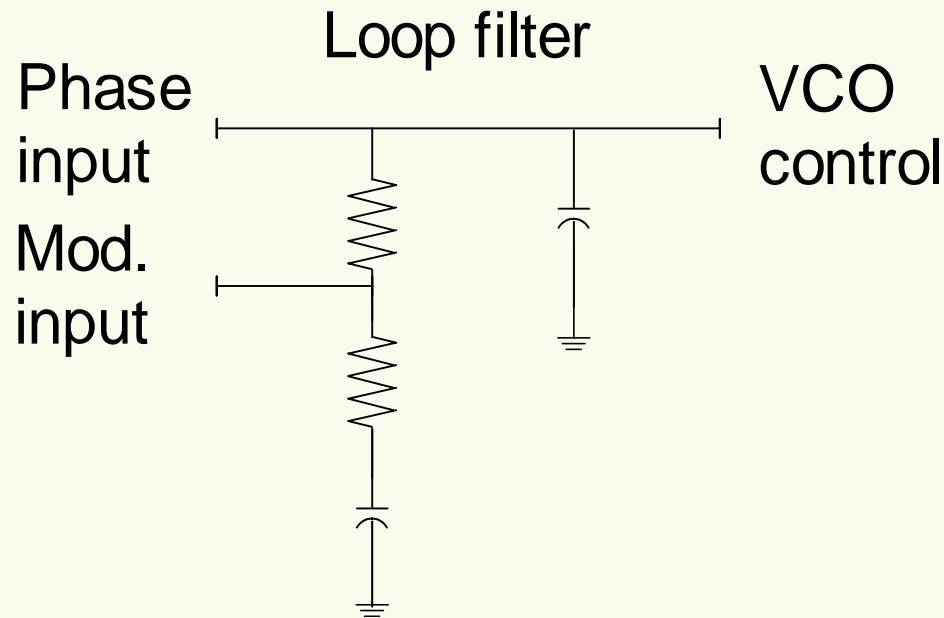
- Reduce the EMI of a circuit by modulating the system clock and hence decrease the power per bandwidth...





Commonly Used Methods for Design.

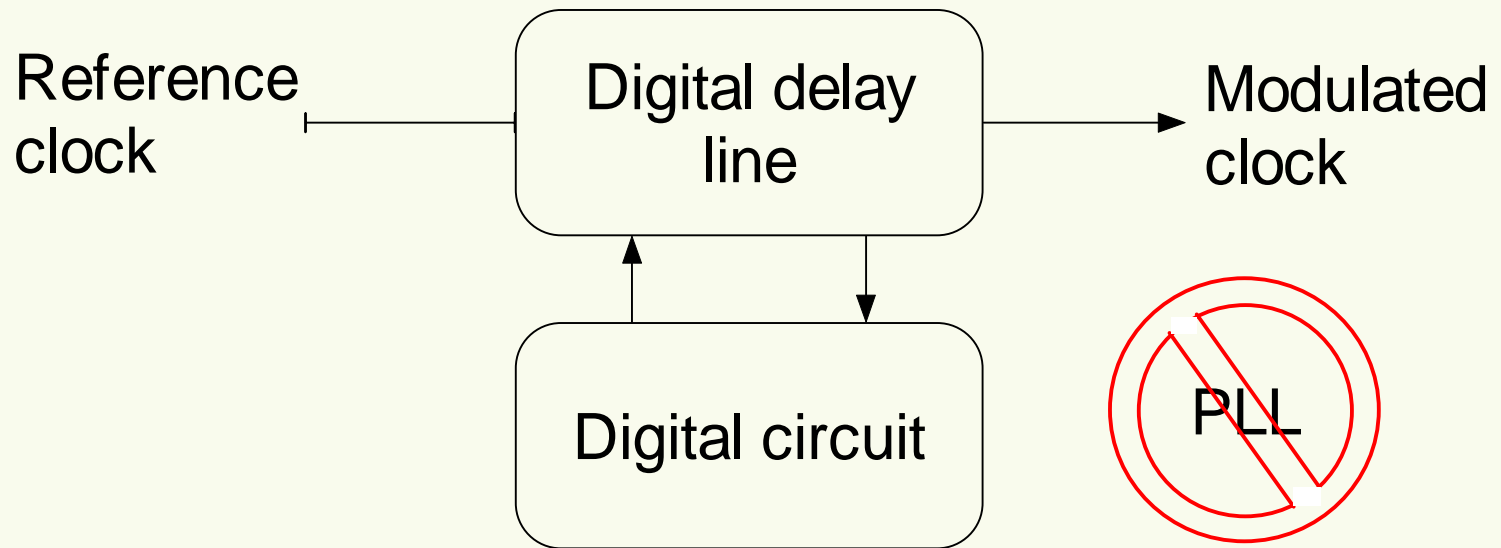
- Most of the methods used produce the modulation by changing the system PLL.





Proposed Method to Generate the SSCG.

- Use only a digital delay line and a digital circuit to generate the modulated clock.





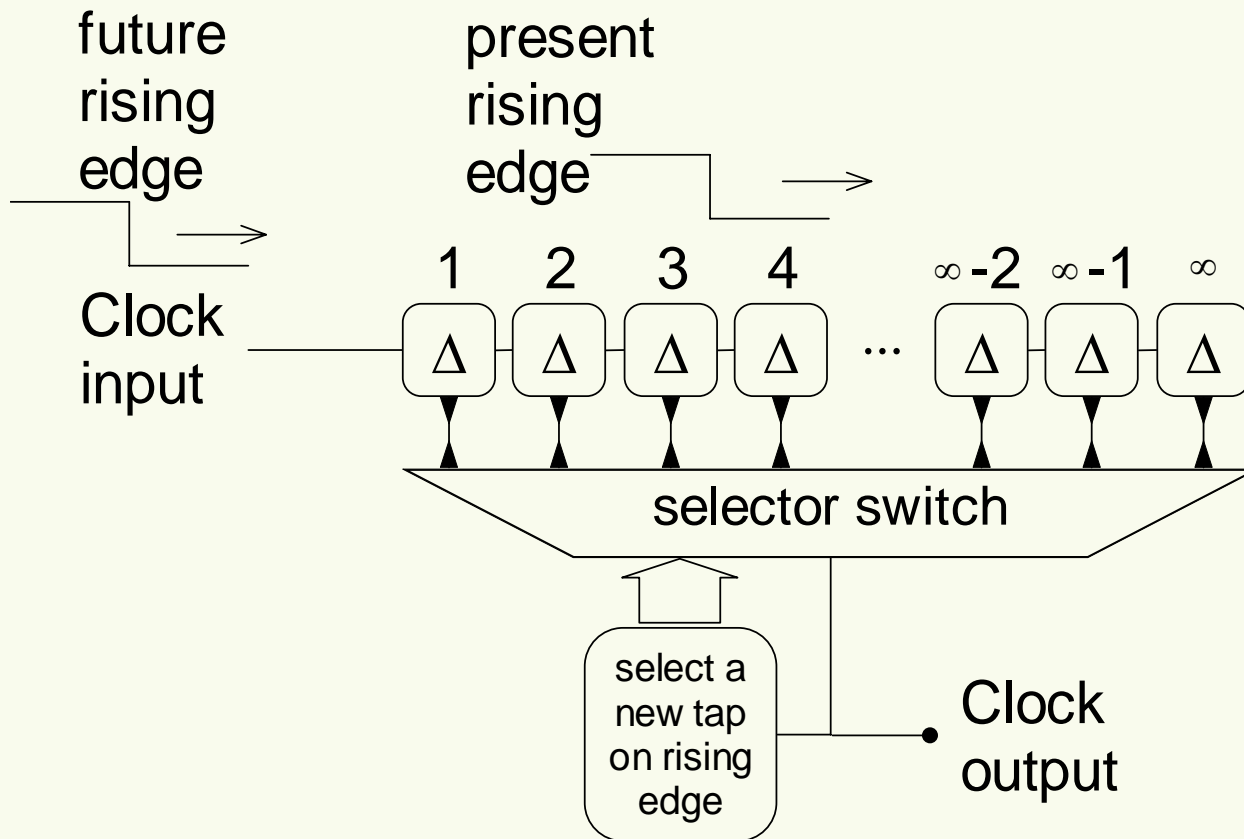
How Do We Generate the SSCG in This Case?

- Concept used in SSCG:
 - Modulating the frequency with an infinitely long digital delay line...
 - Emulating an infinitely long digital delay line while modulating a clock.
 - Calibration over process and temperature.
 - Up spread modulation mode for SSCG.



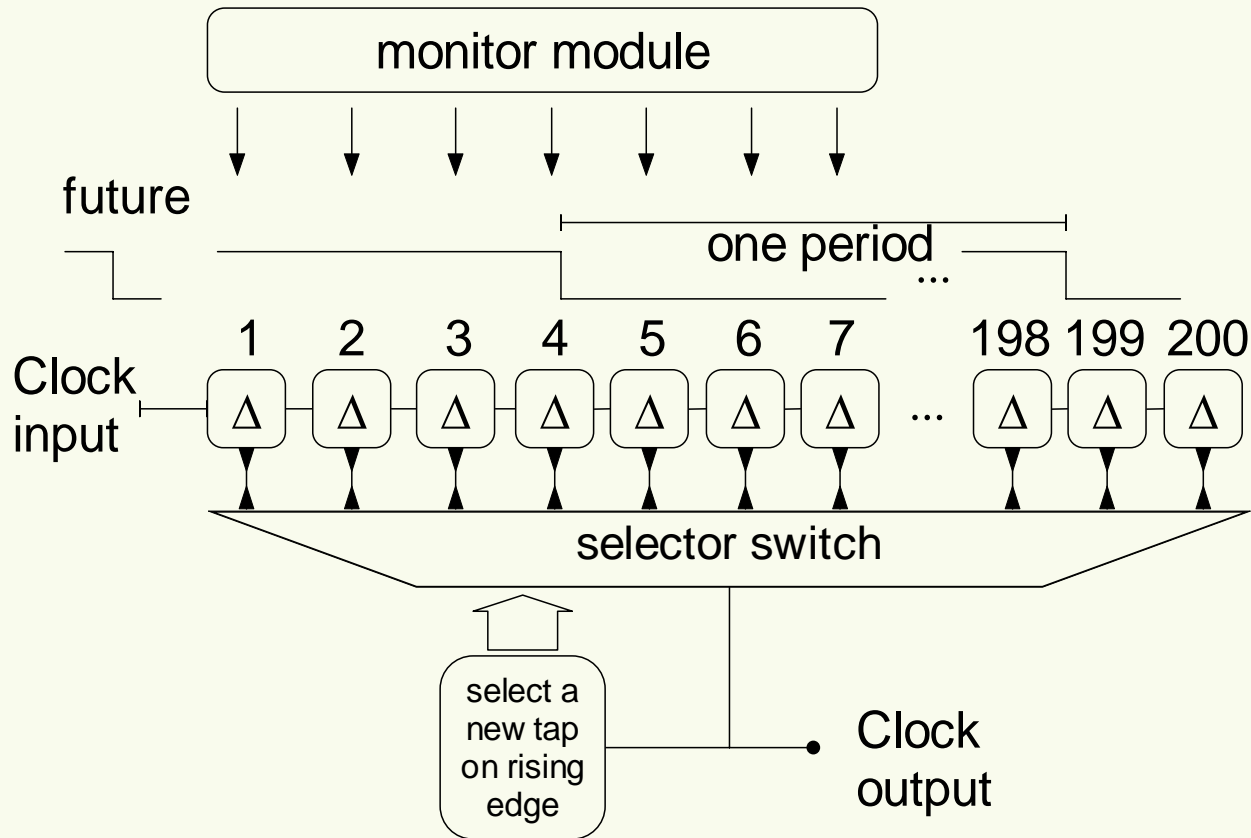


Modulating the Frequency With an Infinitely Long Digital Delay Line...





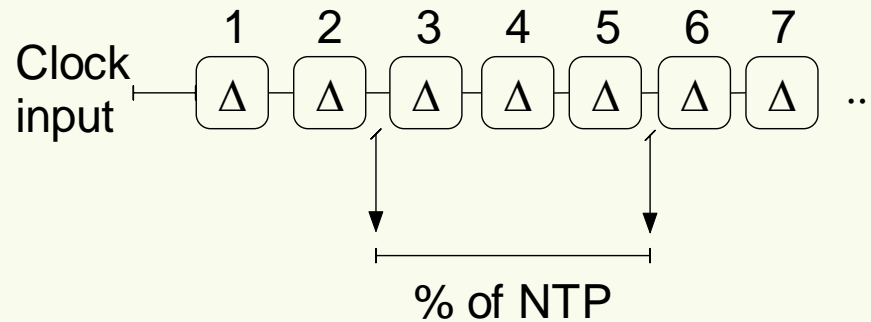
Emulating an Infinitely Long Digital Delay Line While Modulating a Clock.





Calibration Over Process and Temperature.

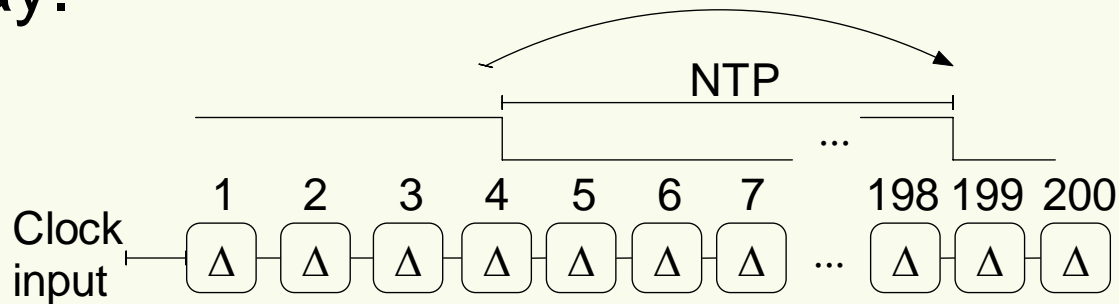
- Knowing the number of tap per period (NTP), we can perform the desired frequency deviation without knowing the absolute tap delay.





Up Spread Modulation Mode.

- One can reduce the tap number for each cycle as opposed to increase it!
- When close to the beginning of the delay line and knowing the number of tap per period (NTP), one can return toward the end of the delay line and create one period delay.





Concept Review

- Modulate the frequency with a digital delay line.
- The digital delay line should be at least one period long of the clock for modulation.
- No absolute tap delay information needed for calibration.
- UP or DOWN spread can be performed.





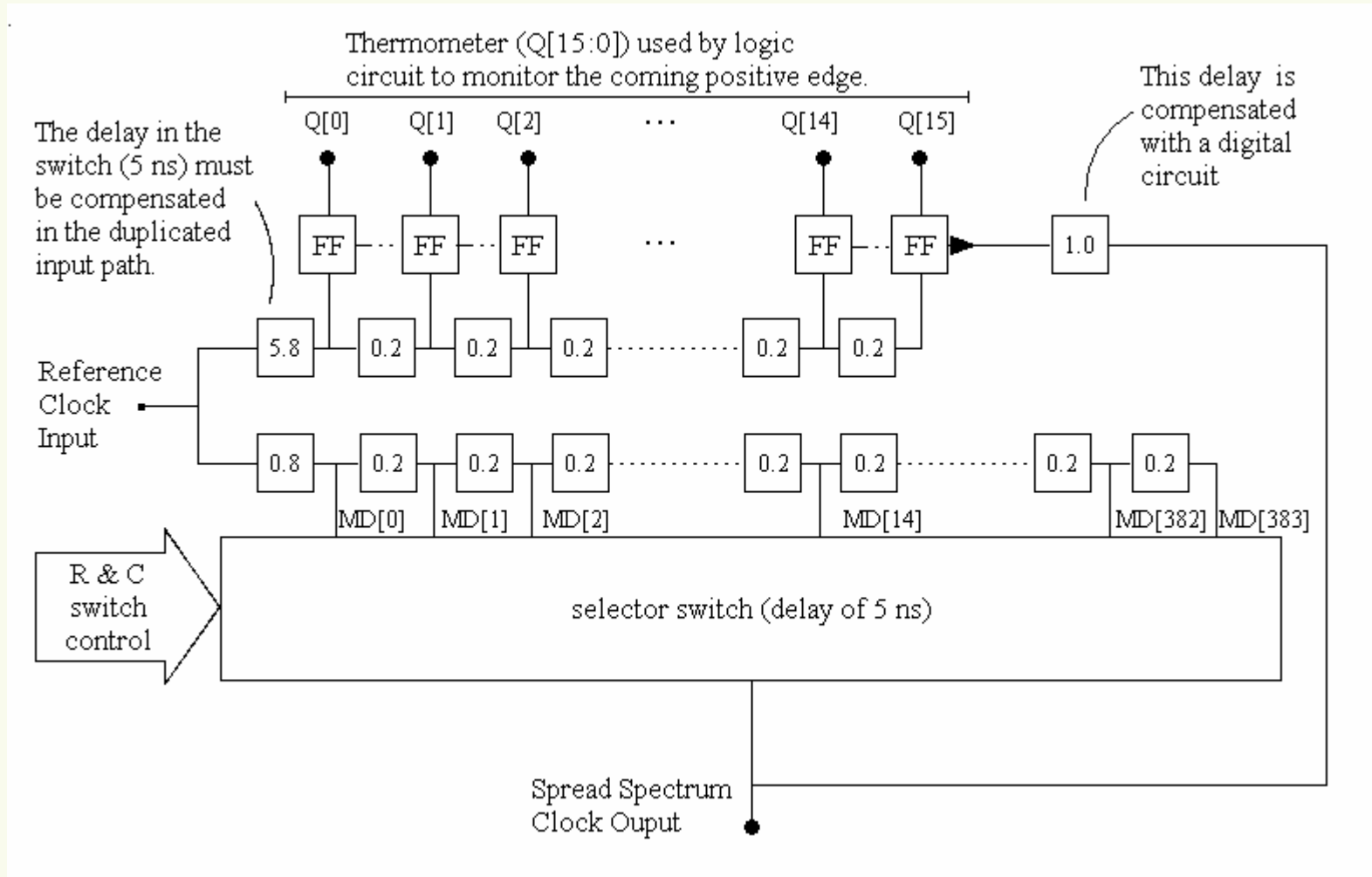
Some Details on Implementation

- Digital delay line
 - Thermometer decoder
 - Delay of the selector switch
 - Delay of the clock to FF of the thermometer decoder
- Digital circuit
 - Triangular wave generator with integrator
 - Wrap around circuit
 - NTP for self calibration
 - Adaptive circuit to compensate for the clock delay





Digital Delay Line

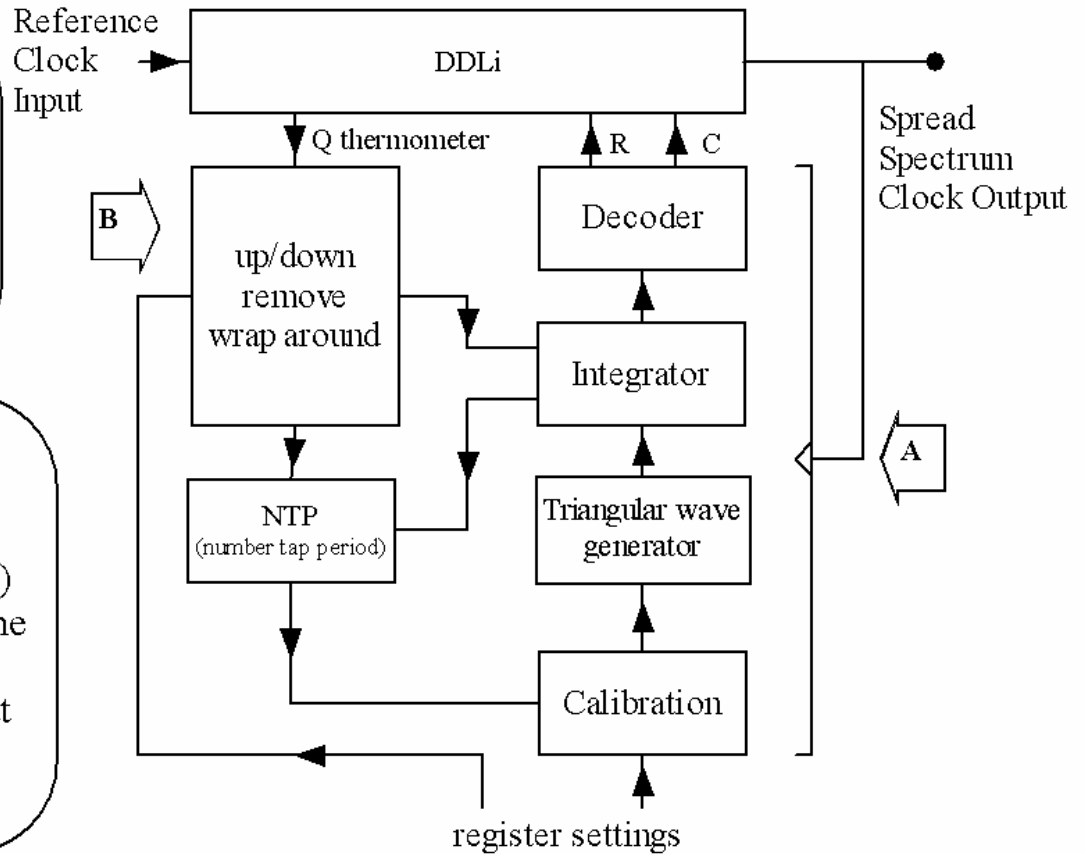




Digital Circuit

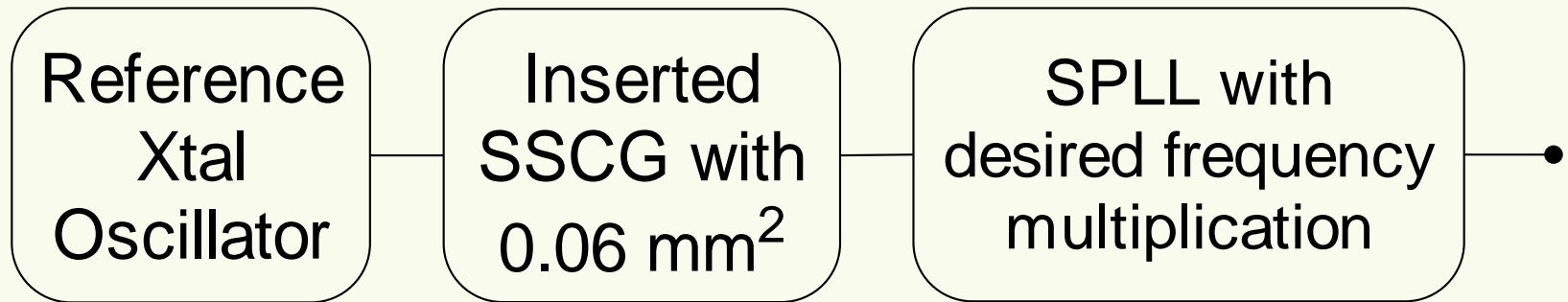
A
A positive clock edge triggers the logic to change the delay tap point. As a result, the location of the next positive edge will be moving forward or backward from the nominal value.

B
When the selected tap is such that the total delay is longer than one period of the signal, the coming (future) rising edge is detected with the Q thermometer and the next tap delay is selected such that we are removing one period of delay in the delay line.





Typical Implementation and Advantage

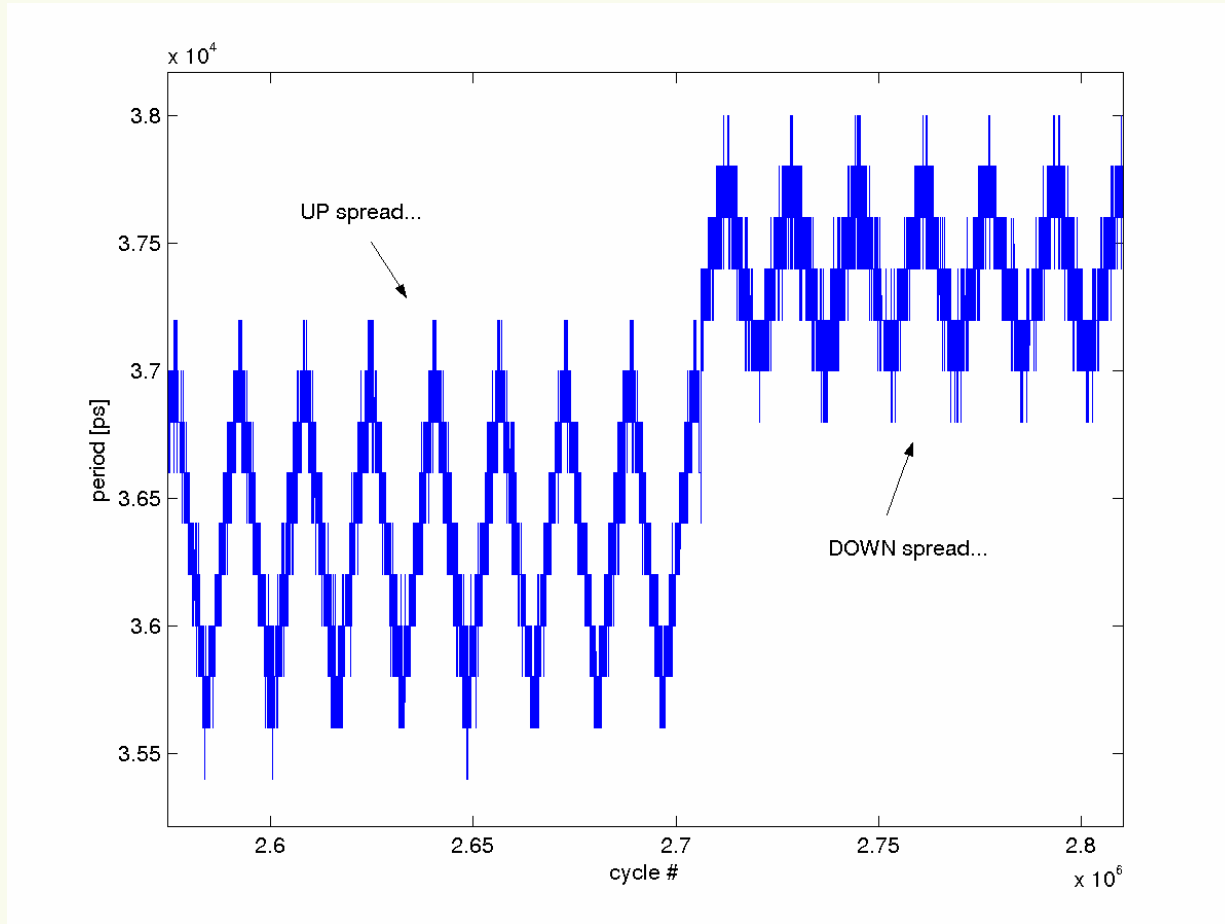


- No modification required to SPLL for fast integration !





Simulated Results of the SSCG



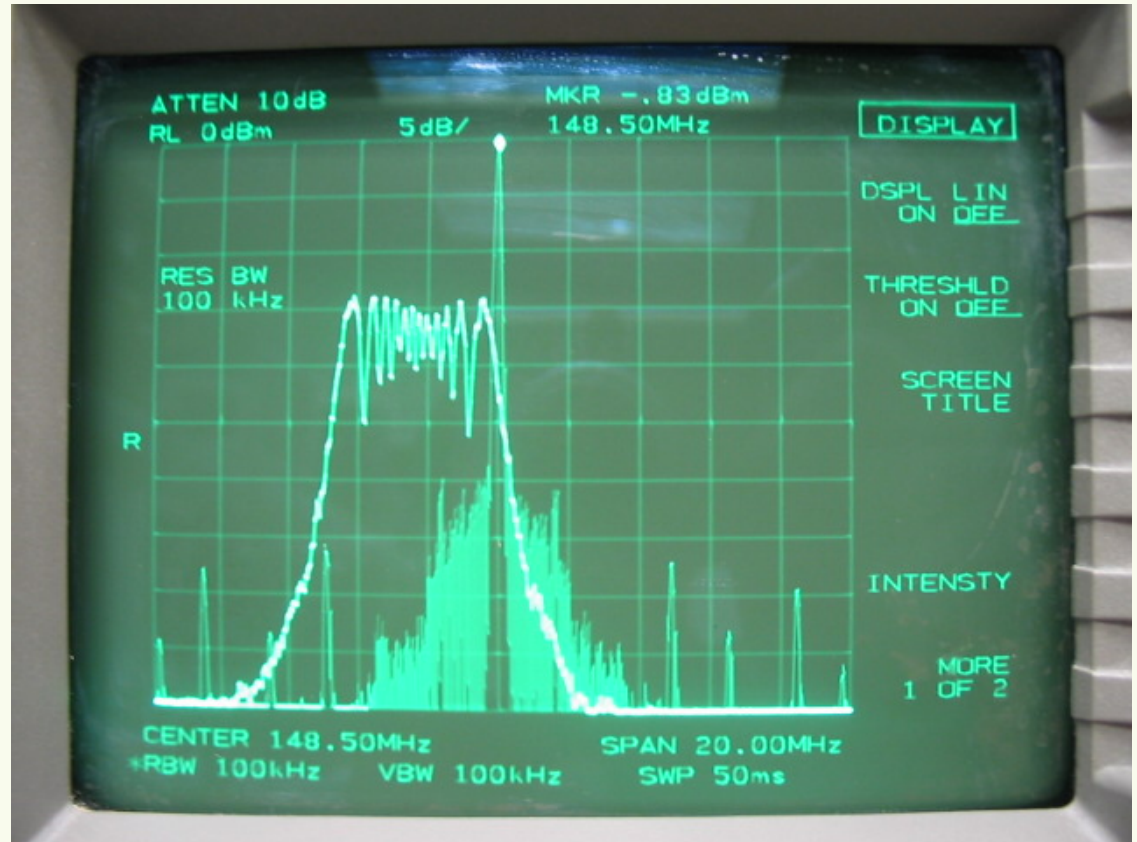
- Simulated results of up and down spread SSCG:





Measured Results of the SSCG

- $F_m = 100 \text{ KHz}$.
- $F_{\text{dev}} = 3.0 \%$.
- $\text{PPR} > 13 \text{ dB}$.
- $F_{\text{pll}} = 5.5 * F_{\text{ref}}$



- Spectrum analyzer view with and without SSCG:





Conclusion

- We presented an “all digital” SSCG.
- UP or DOWN spread can be generated.
- More than 13 dB of peak power reduction can be achieved with 3% deviation.
- Circuit is 0.06 mm² on 0.15 um CMOS process.
- No modification to system PLL required.





Acknowledgements

- The team at ESS Technology Kelowna!

