

DRP™ – Digital Radio Processing

*System-On-Chip Solutions for
Mobile Devices*

Oren Eliezer

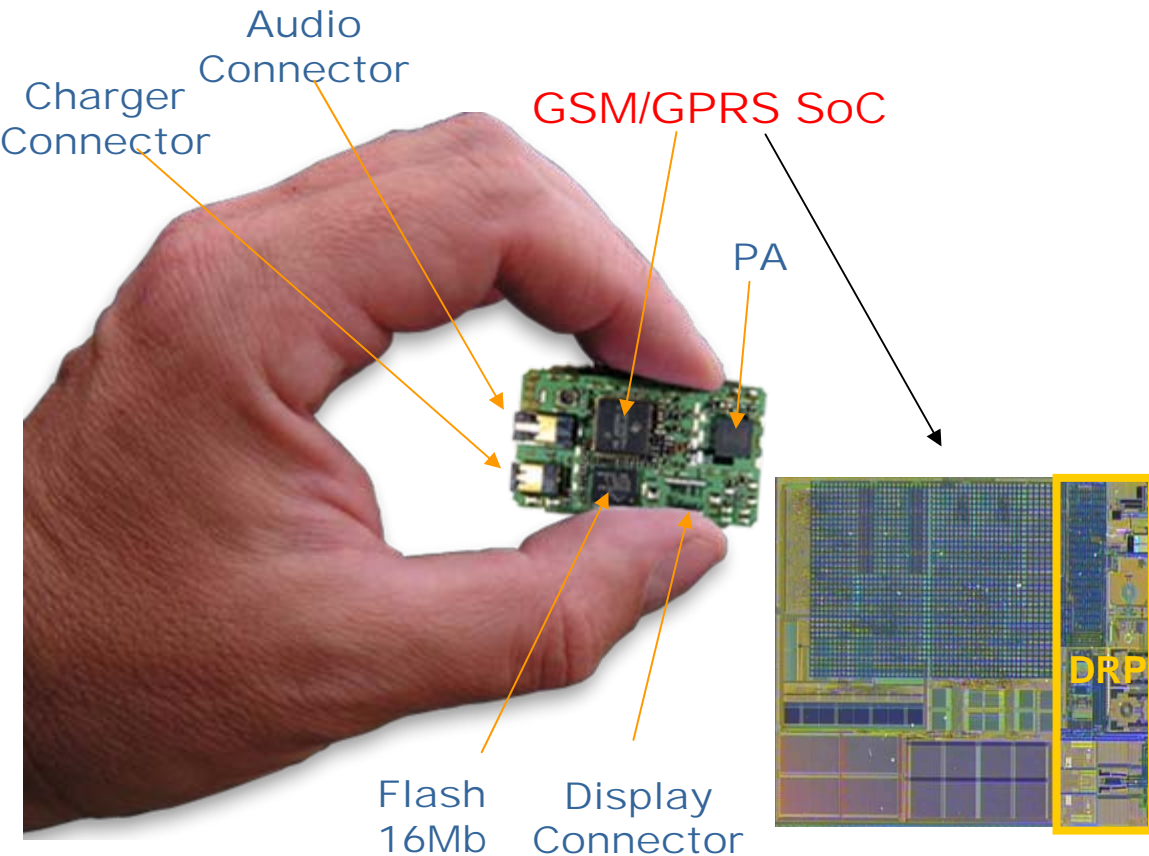
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Outline

- ◆ **Motivation for CMOS SoCs in Mobile Devices**
- ◆ **Integration approaches (SoC vs. SiP)**
- ◆ **Integration trends in mobile devices**
- ◆ **Fundamentals of the DRP Technology**
- ◆ **Methodology for Design, Simulation and Testing**
- ◆ **Summary**

TI's GSM SoC - Key Milestones



- ◆ February 2004 –
1st phone call on DRP test chip
- ◆ March 2005 –
1st phone call on fully functional single-chip solution
- ◆ 2006 –
characterization completed.
- ◆ **Ramping up in mass-production!**

Press coverage...

Motivation (Markets...)

Application Rich

- Cameras, TV, Games,
- Video, Audio, etc.



Emerging Markets Growth vs. Industry Standard of 23%

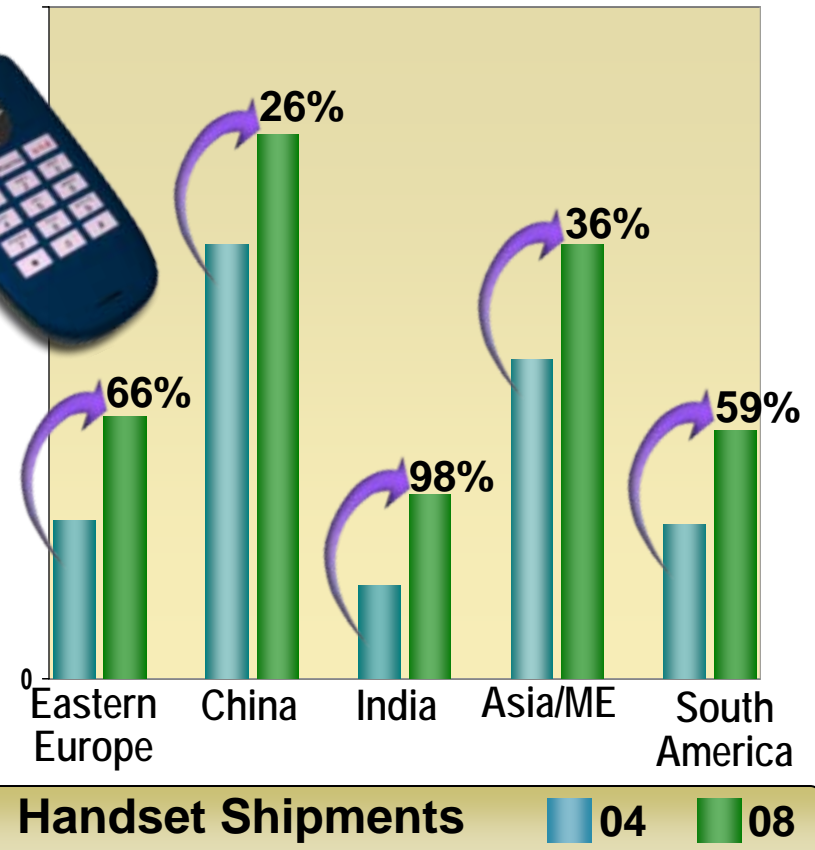
Multiple Air Interfaces

- Cellular
- Bluetooth
- WLAN
- GPS
- mDTV

Multi-band and Multi-mode

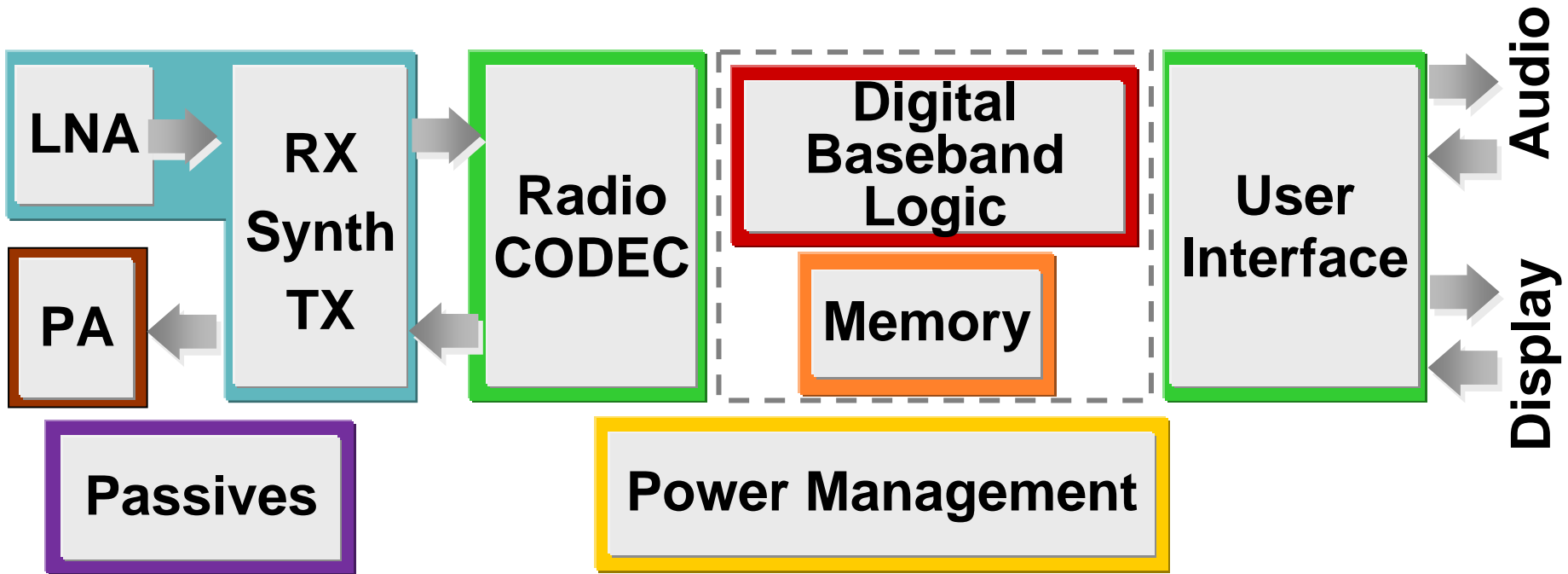
- GSM, GPRS, EDGE, UMTS...
- 800, 900, 1800, 1900, 2100 MHz...








Both low-end and high-end phones benefit from integration!



Source: Forward Concepts, Global Cellular Handset & Chip Markets, April 2005

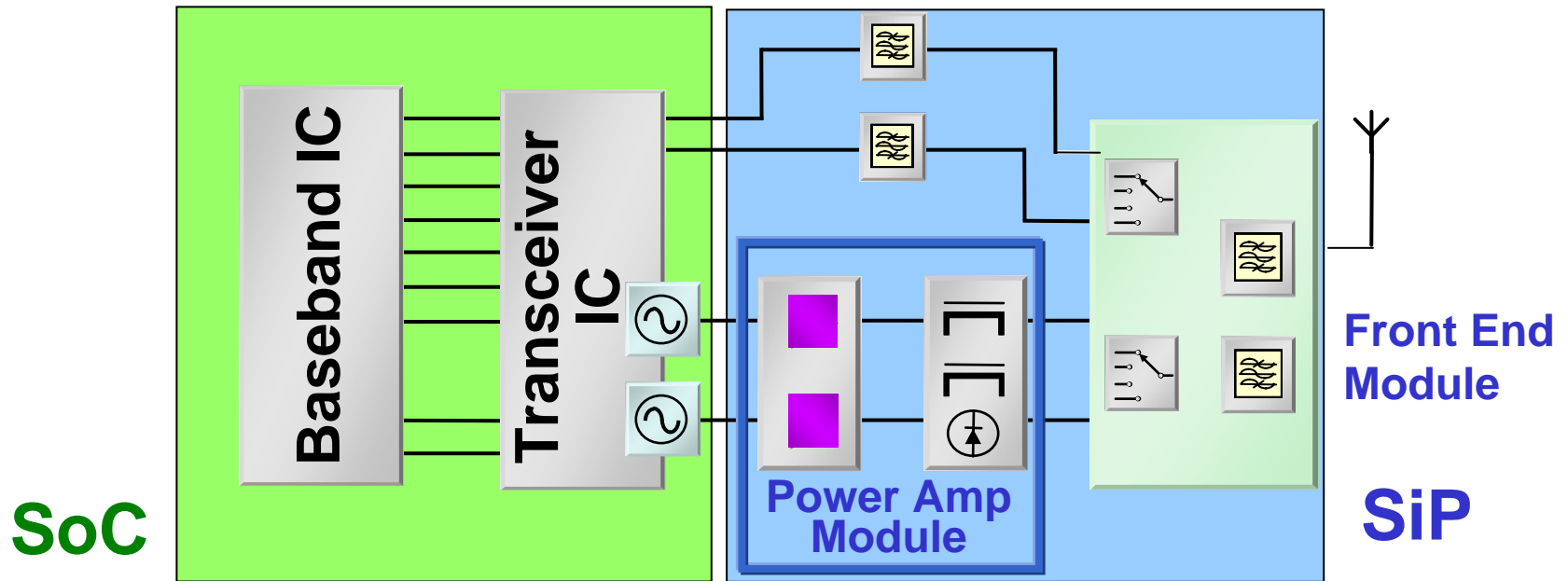
Typical Cell-Phone Block Diagram



 SiGe BICMOS	 High voltage	 DSM Digital
 Discrete Passives (SAW Filters, etc.)	 Analog CMOS	 FLASH EEPROM
	 High-power (typically GaAs)	

Area and cost must be reduced → integrate !

SoC vs. SiP Integration



SoC (System on Chip):

- ◆ Reduction in power, cost, board area, testing costs
- ◆ Improved performance, phone manufacturability and yield
- ◆ Higher development cost, requires broad mix of expertise

SiP (System in Package):

- ◆ Reduction in external components and board space
- ◆ Allows package integration of different technologies (e.g. SiGe/GaAs + CMOS)
- ◆ Simplified development (modular)

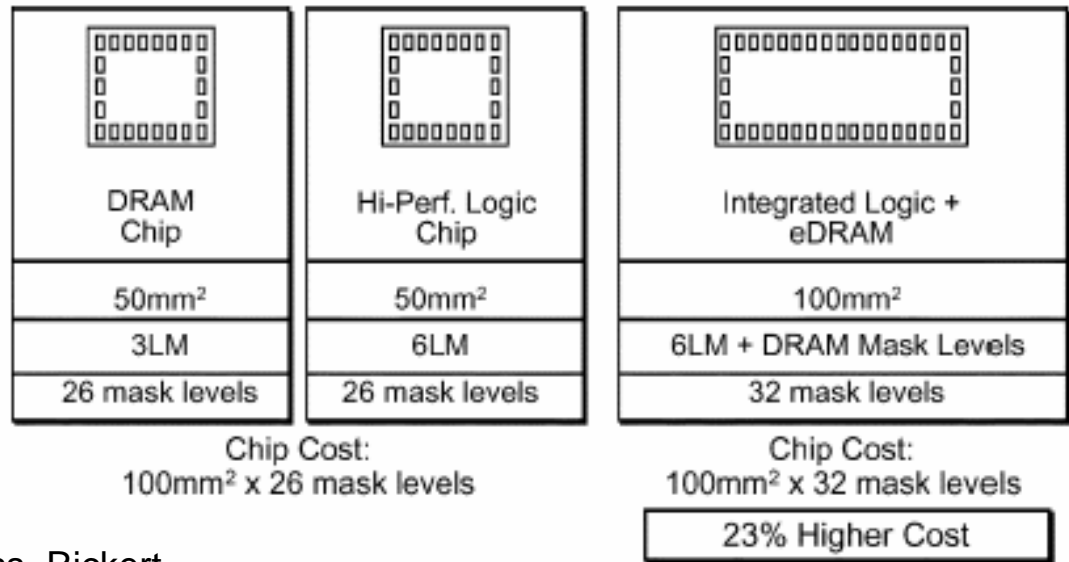
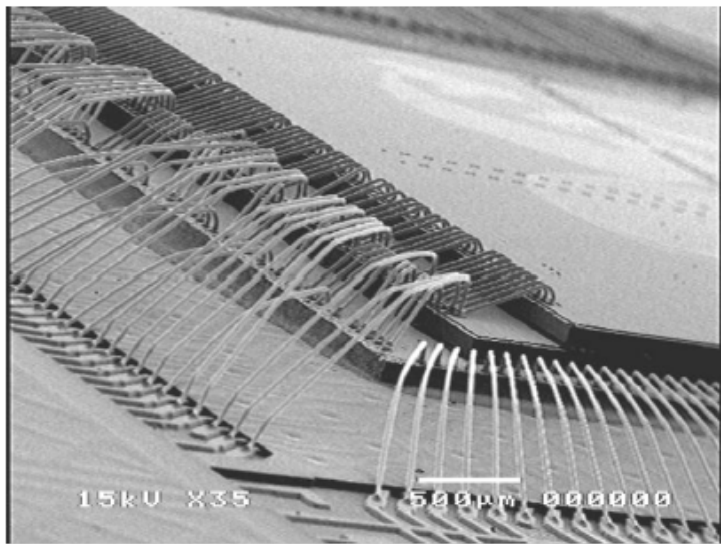
When integrating the radio with the CMOS baseband processor and logic, the SoC integration solution is most competitive!

SiP Also For DRAM Integration

- ◆ Monolithic integration of DRAM would result in significant cost increase due to the need for additional mask levels.
- ◆ Memory modules are highly reusable so modularity makes sense.
- ◆ No yield impact issue due to in-package integration of memory.

❖ Stacked die

❖ Embedded DRAM can increase total cost...



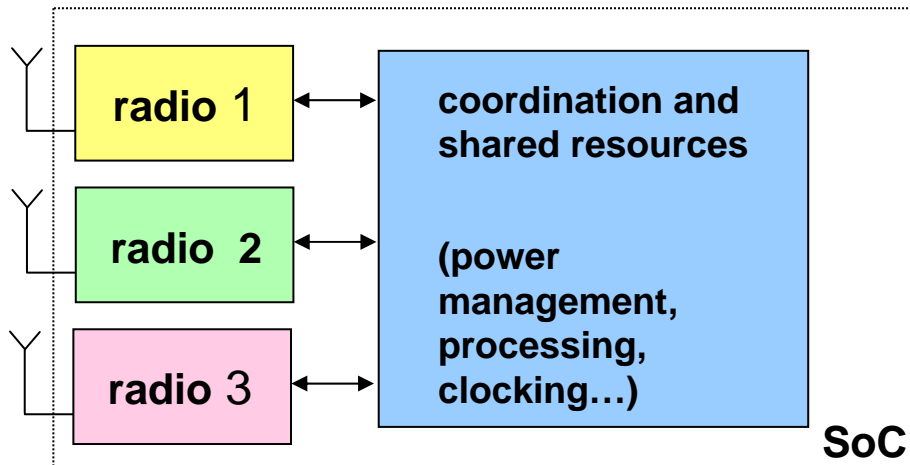
Ref.: [2] Krenik, Buss, Rickert

But... For Radio Integration – **only SoC** !

- ◆ The modularity approach (separate radio) does not make sense for handsets since the **high volumes justify dedicated integration** exercises for each product (e.g. different flavors of TI GSM SoC).
- ◆ Might not be intuitive since radios traditionally required analog-friendly processes.
→ SiP was a more straightforward development towards integration and was therefore implemented by some in the industry.
- ◆ The **DRP** (**D**igital **R**adio **P**rocessor) technology for CMOS radios is revolutionizing the handset market, by simplifying the monolithic integration of **transceivers** with **digital logic and baseband processors** in the most aggressive process nodes (currently designing on 65nm).

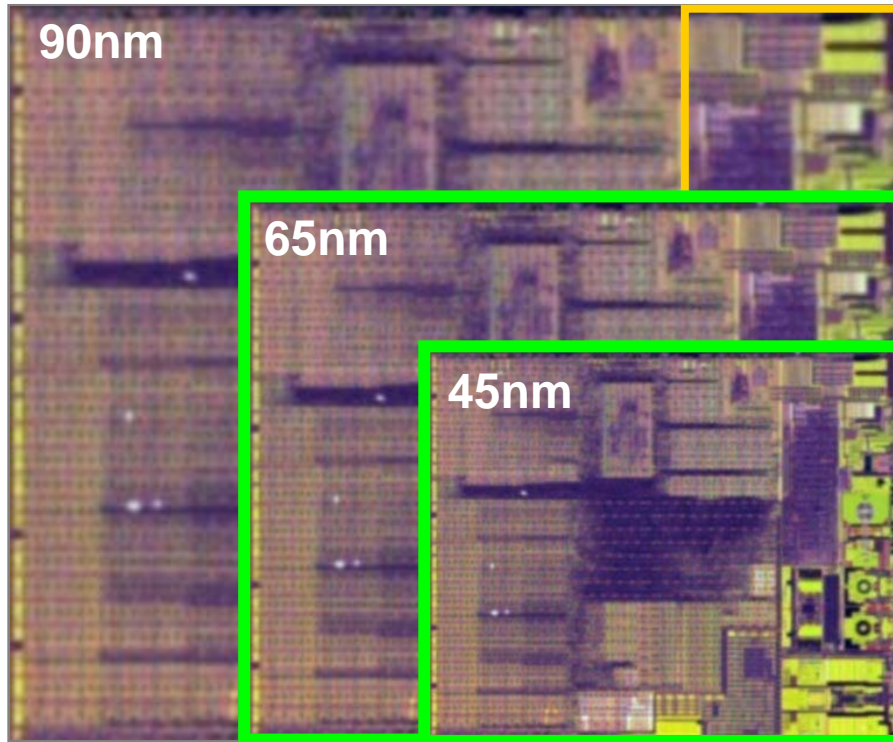
Additional Factors to Consider...

- ◆ An analog radio integrated with a digital processor in **SiP will adversely impact yield and cost**, since its parametric testing can typically only take place once packaged (a failure in the radio requires discarding the SiP).
- ◆ Contrarily - in a DRP based SoC, an **on-chip-radio built-in-tester (ORBIT™)** actually leverages on the integration for test-cost reduction!
→ **Most RF testing can take place before packaging (at “probe”)**!
- ◆ What about the integration of **multiple radios**?...
SiP – too many bondwires creating **excessive coupling** between radios...
SoC – simpler sharing of SoC resources,
simpler interconnect & coordination between the multiple radios



Multiple radio SoC
(no internal bondwires)

SoC Drives Cost Reduction



- ◆ **SoC Integration Includes:**
 - ❖ Digital baseband
 - ❖ SRAM
 - ❖ Power management
 - ❖ Analog
 - ❖ RF
 - ❖ Processors & Software
- ◆ **The DRP technology enables digital implementation of traditional analog RF functions in standard CMOS**
- ◆ **Most advanced process technology used to maximize integration while minimizing cost**
 - ❖ 90nm (shipping)
 - ❖ 65nm (mature design)
 - ❖ 45nm and beyond (preliminary)

DRP/SoC Proven Across Many Products

1/2 the silicon

1/2 the power

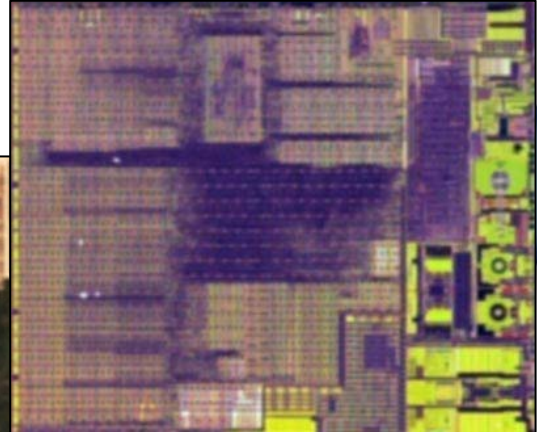
1/2 the board area

**"LoCosto"
GSM/GPRS**

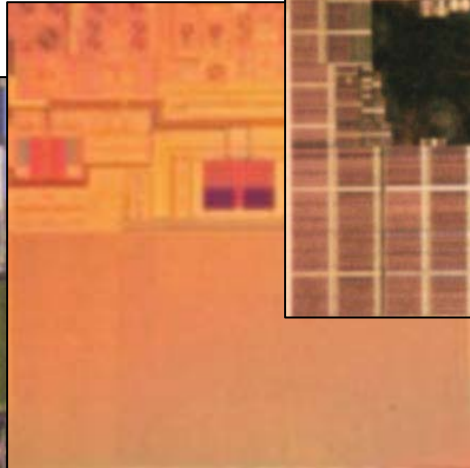
**More
to come...**



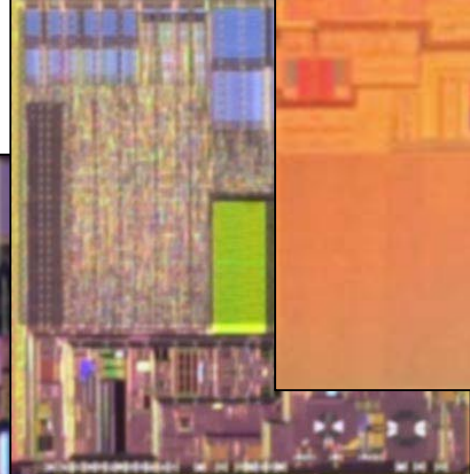
Hollywood™
mDTV



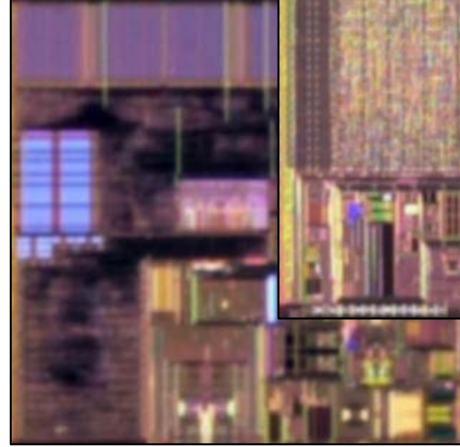
WiLink™
Wi-Fi



NaviLink™
A-GPS



BlueLink™
Bluetooth

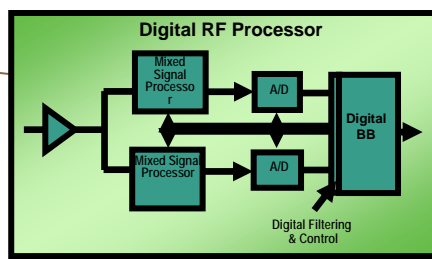


Multi-Disciplinary Technology



System Architecture
(GSM, Bluetooth, WLAN, mDTV)

Circuit Design
(LNA, ADPLL, DAC, ADC, Logic)

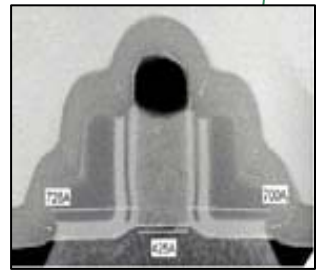


DRP

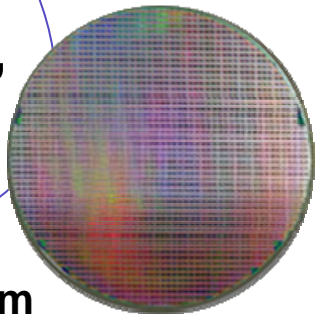


Silicon Process Technology
(90nm, 65nm, 45nm digital RF processes)

Manufacturing Expertise
(300mm, self-test, DD limited yield)



65nm transistor



300mm

Integration Trend in Mobile Devices

Technology Legacy

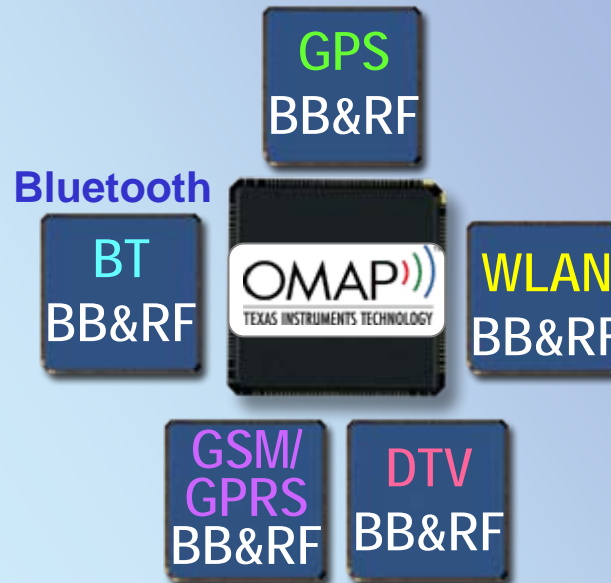


130nm

2003

2004

DRP Migration Across Multiple Standards



90nm

2005

2006

Flexible Integration Options



65nm

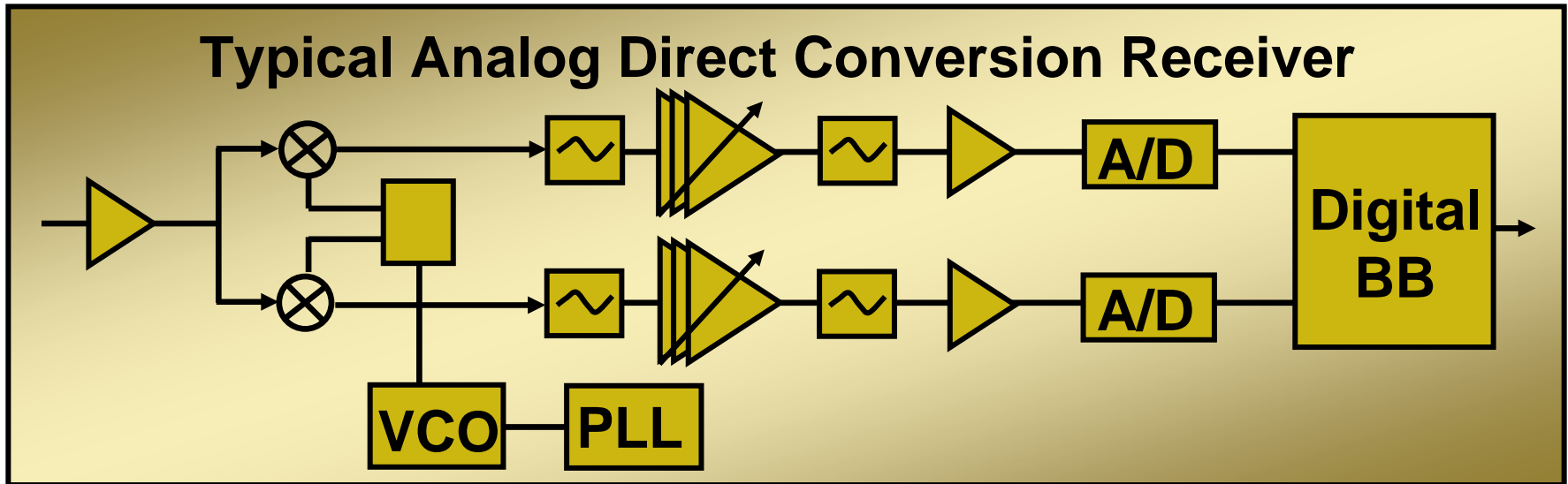
2007

2008

How is the radio made suitable for the CMOS digital process?

Some DRP Fundamentals...

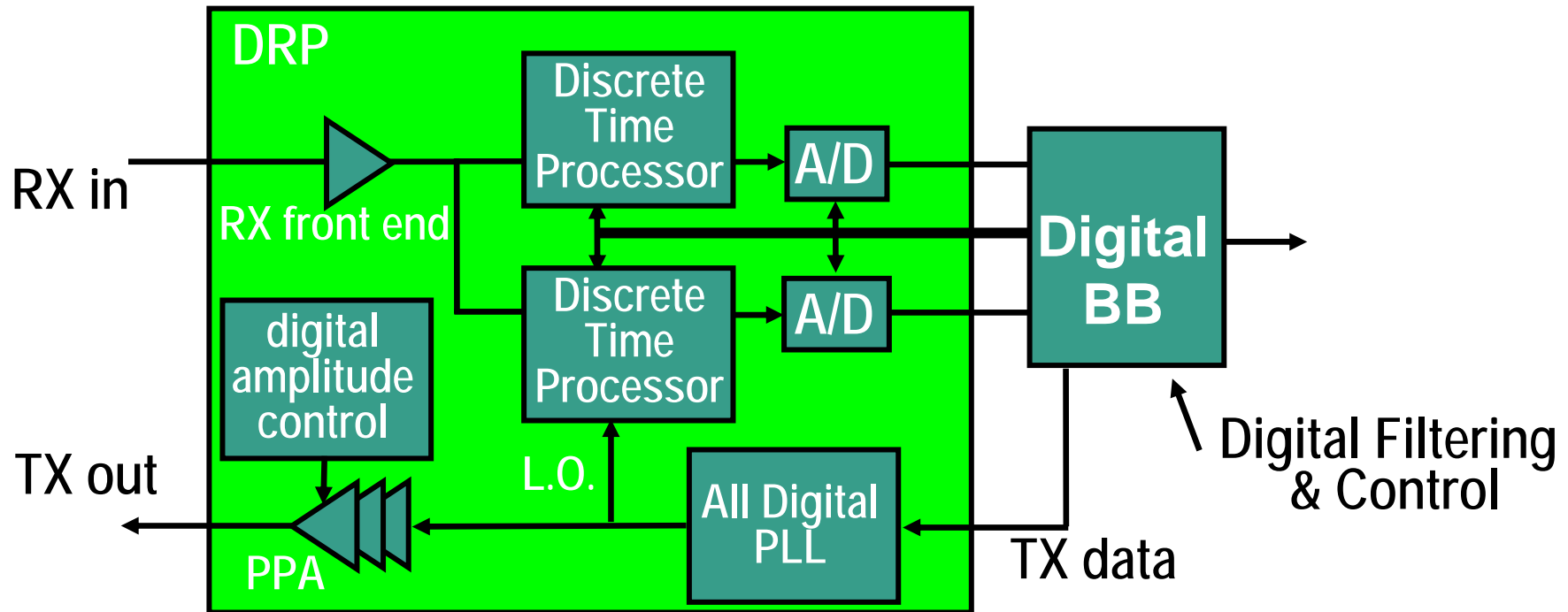
Analog RF Challenges in DSM CMOS



- Power supply voltage overhead – must scale to ~1 Volt
- Passives – need high quality inductors, caps, etc.
- Noise/clock coupling – time-align to avoid interference
- Development time – should not delay node migration of digital baseband processor portion.
- Cost – need to minimize multiple pass testing and yield loss

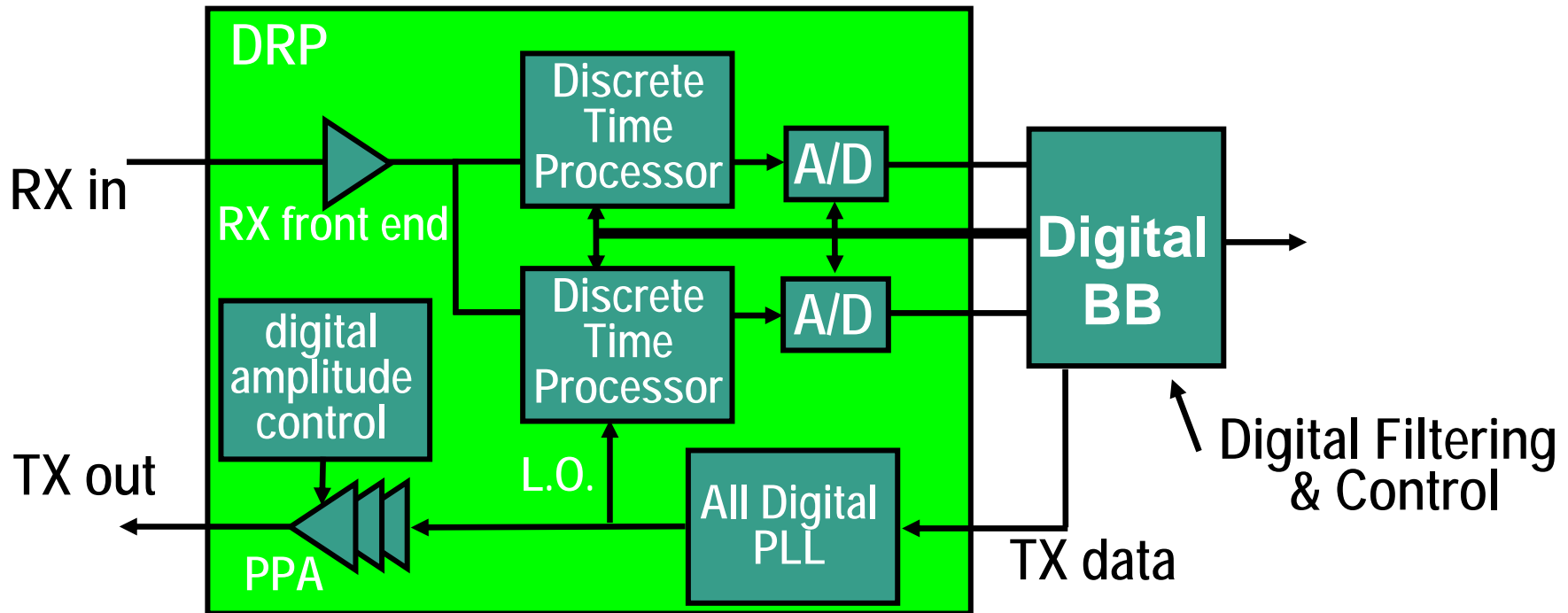
Reference [4] – Khurram Muhammad

The DRP Approach for Transceivers



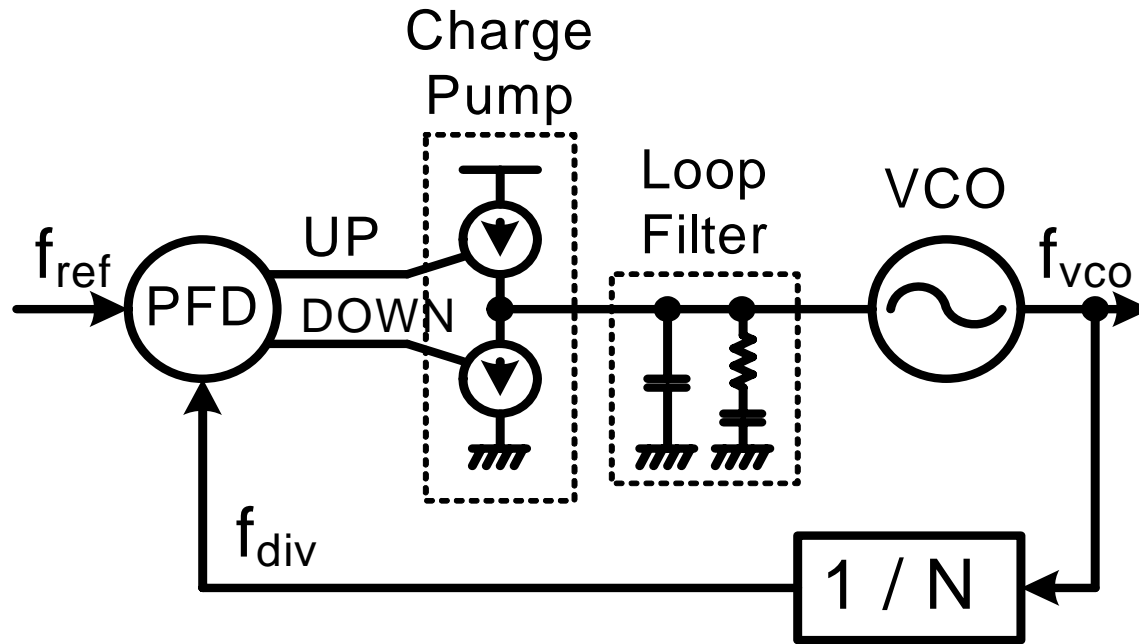
- **Minimize analog and RF circuitry**
 - Self-calibrate remaining analog (with dedicated processor)
 - Relax passive requirements as much as possible
- **Digital approach speeds debug and development**
- **Self-test and calibration made possible**
- **Production yield dominated by silicon defect density**

The DRP Approach (continued)



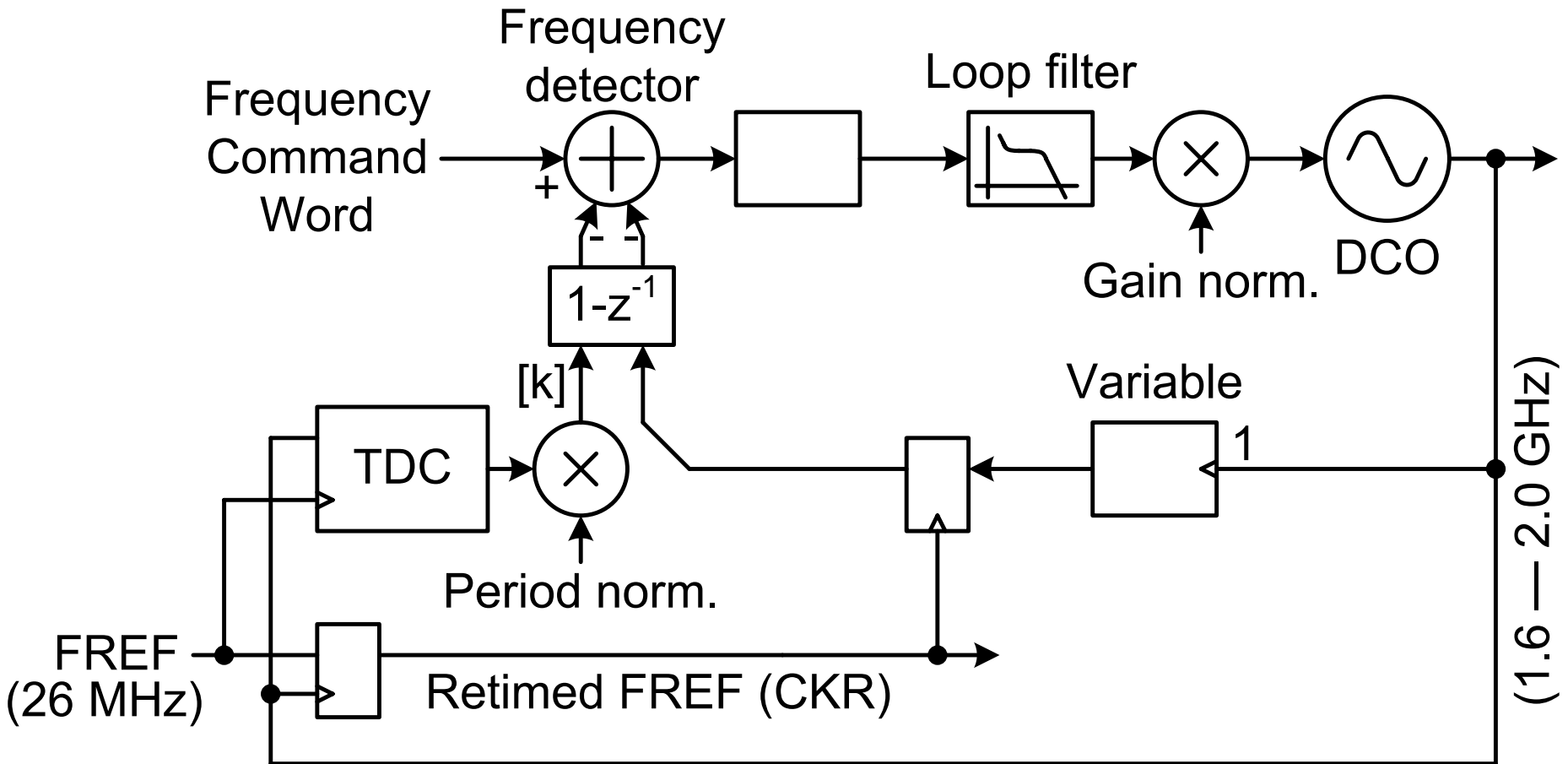
- **Move functions to domains of CMOS-process strengths**
 - Operate in fine time resolution, avoid fine voltage resolution
 - Inductor area could be equal to ~100K gates (use digital!)
 - Use switched cap techniques – excellent matching in DSM CMOS (not sensitive to process variations)
 - Logic and switched cap circuits can work well at low voltage

Drawbacks of Conventional Analog PLL



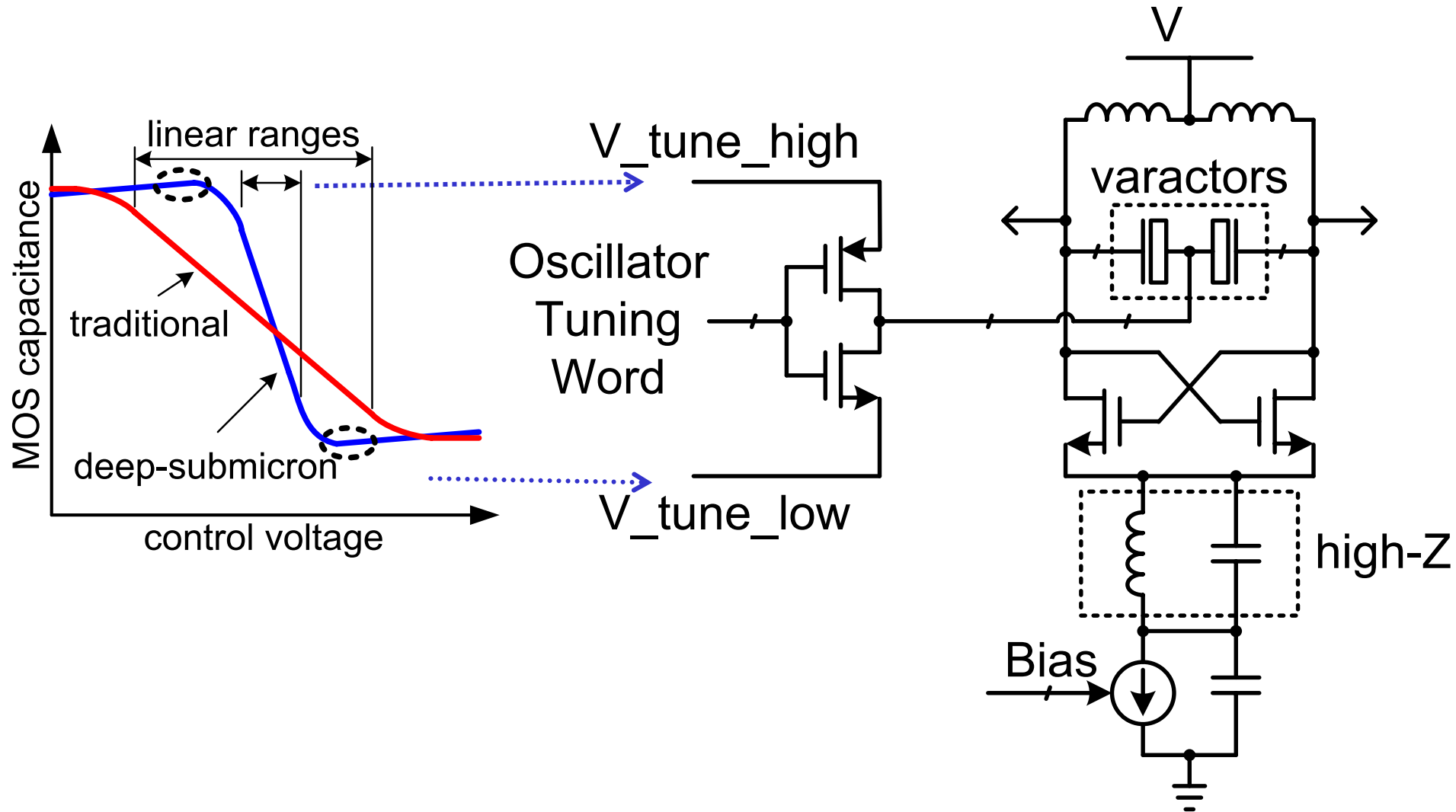
- Many analog functions = multiple noise sources
- Varactors in VCO are sensitive (high tuning factor, i.e. KVCO)
- Loop filter may be large, leaky capacitors (for open loop “freeze”), variances in passives...
- Hard to calibrate
- Lock times can be long ($>100\mu\text{sec}$)

All-Digital PLL (ADPLL)

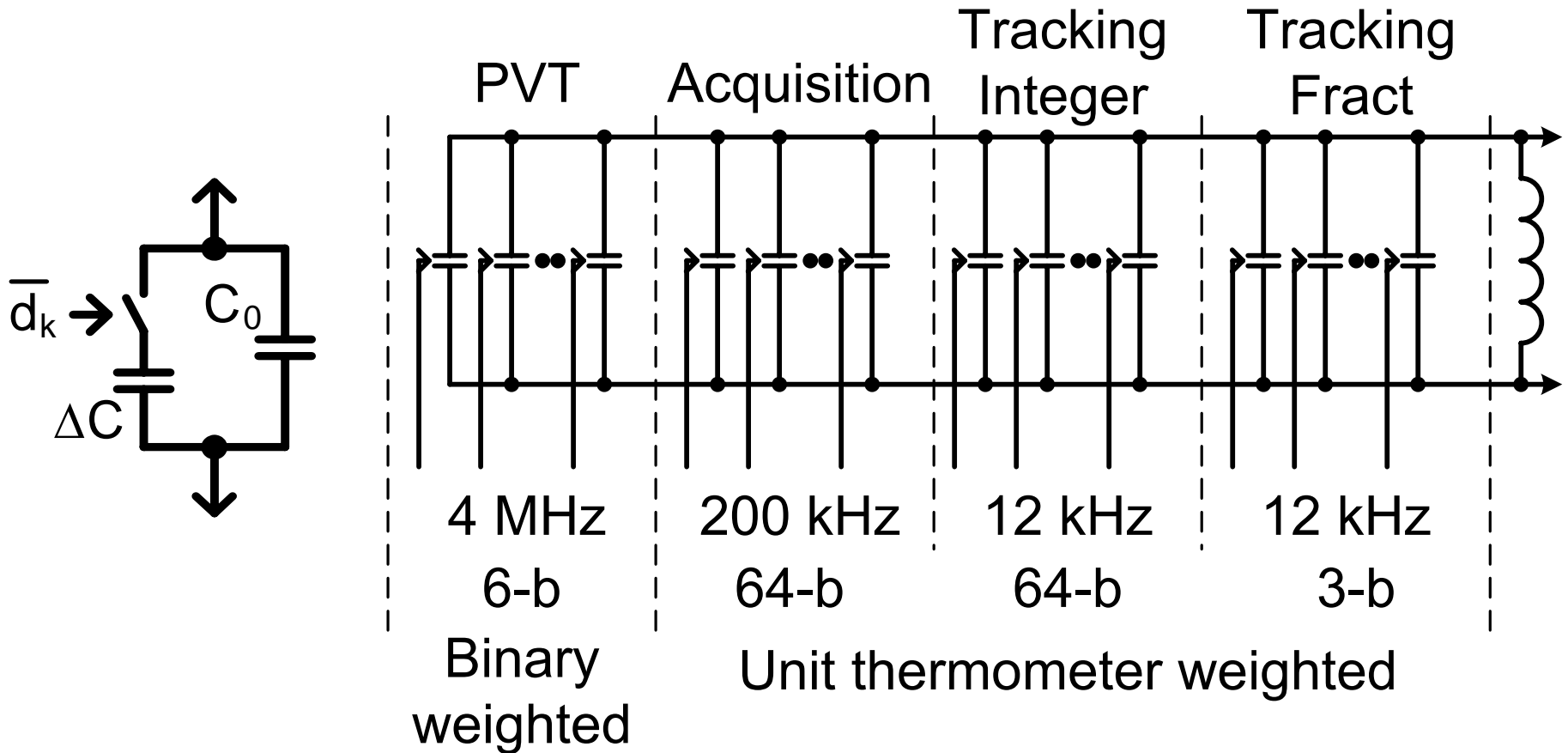


References [1], [3] - **Bogdan Staszewski, John Wallberg**

Digitally-Controlled Oscillator Core



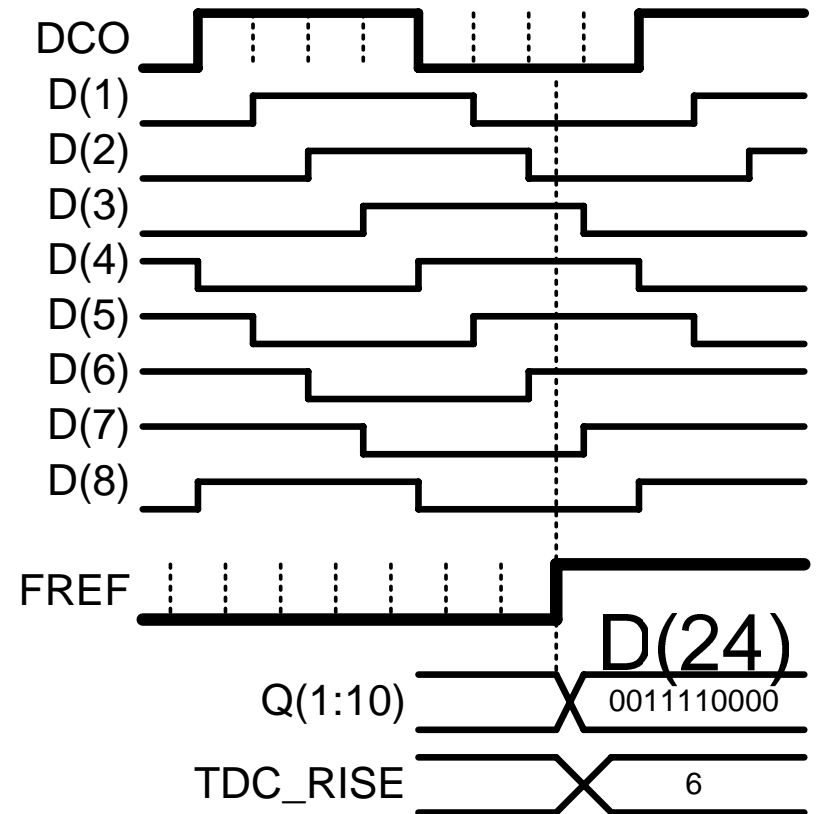
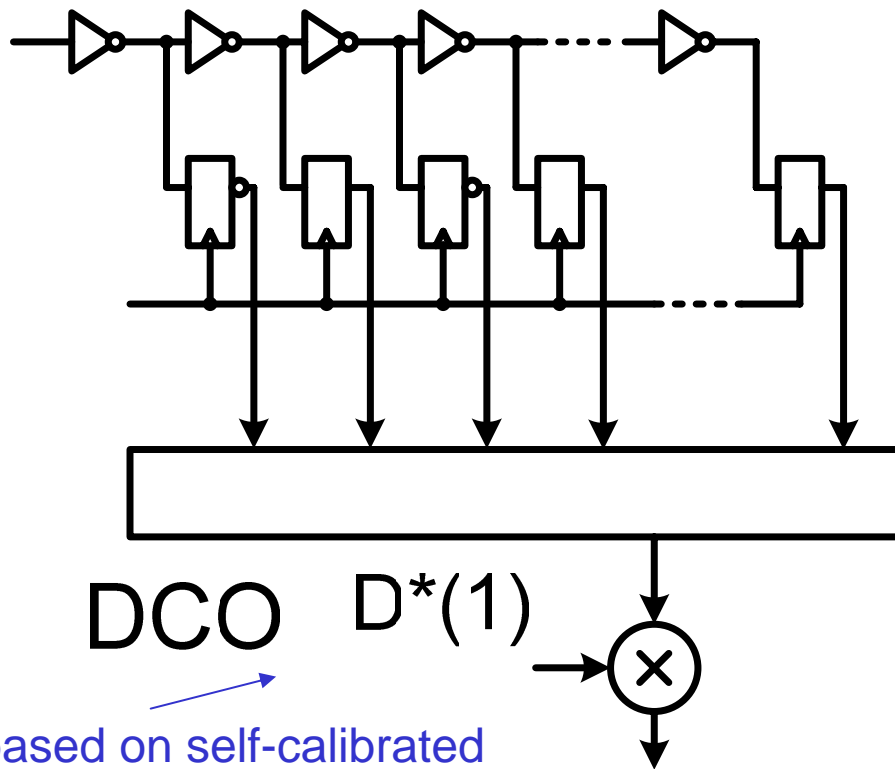
DCO Varactor Banks



High-speed dithering and dynamic element matching are used to achieve high resolution (LSB = $\sim 1.5\text{Hz}$).

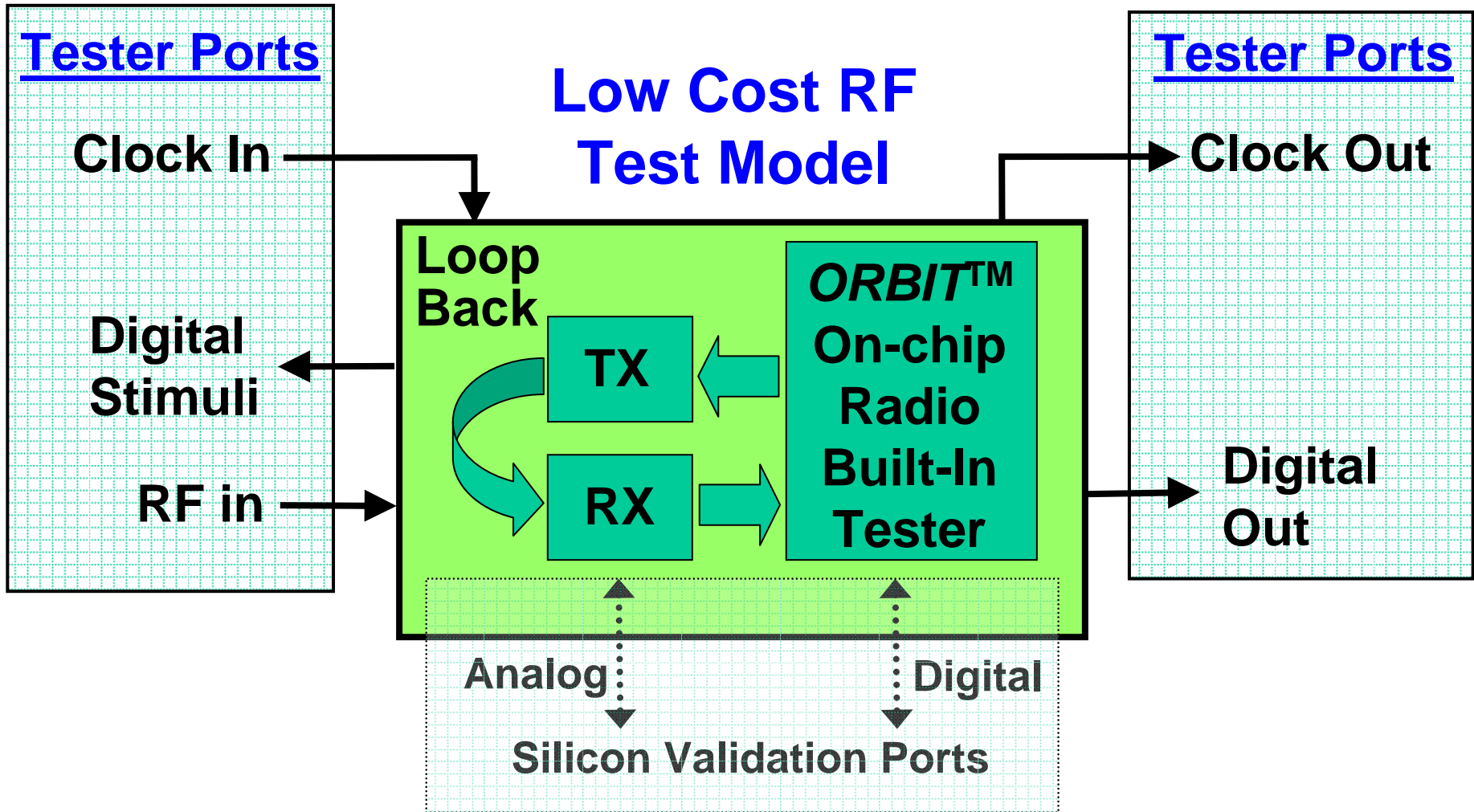
Time-to-digital Converter (TDC)

- ◆ Quantized phase detector with resolution of about 20 ps
- ◆ DCO clock passes through the inverter chain
- ◆ Delayed outputs are sampled by FREF



Production Testing Simplification

- Extensive use of built-in-testing capabilities to reduce test costs.
- Tester is simple (low cost) and test time is minimal.



The DRP Technology - Summary

Process Capability

- **Advanced CMOS processes allow clocking logic at radio frequencies.**

Node Migration

- **Analog content minimized to reduce development time and re-design efforts when migrating to next node.**

Performance

- **Robust (extensively digital), low noise, low power.**

Cost

- **Reduced silicon area (standard process)**
- **Reduced board area in product**
- **Lower analog content → higher yield**
- **Built-in self test and calibration**

References / Acknowledgement

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Thank you!

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