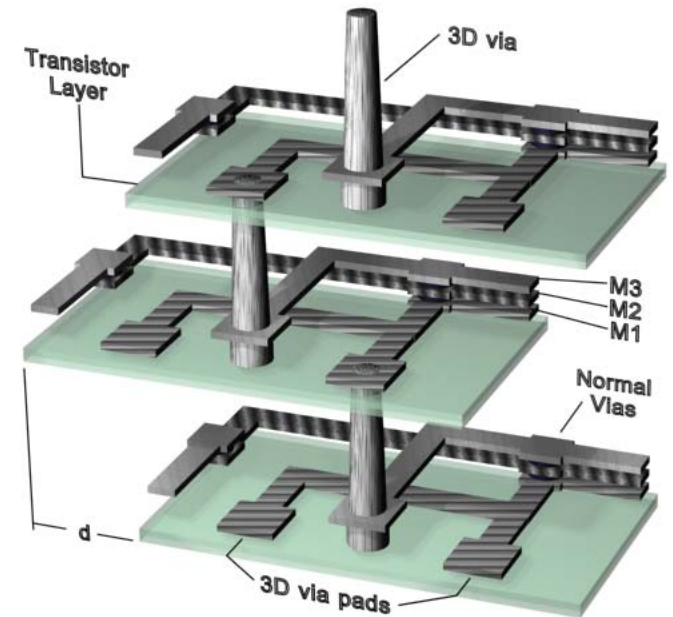
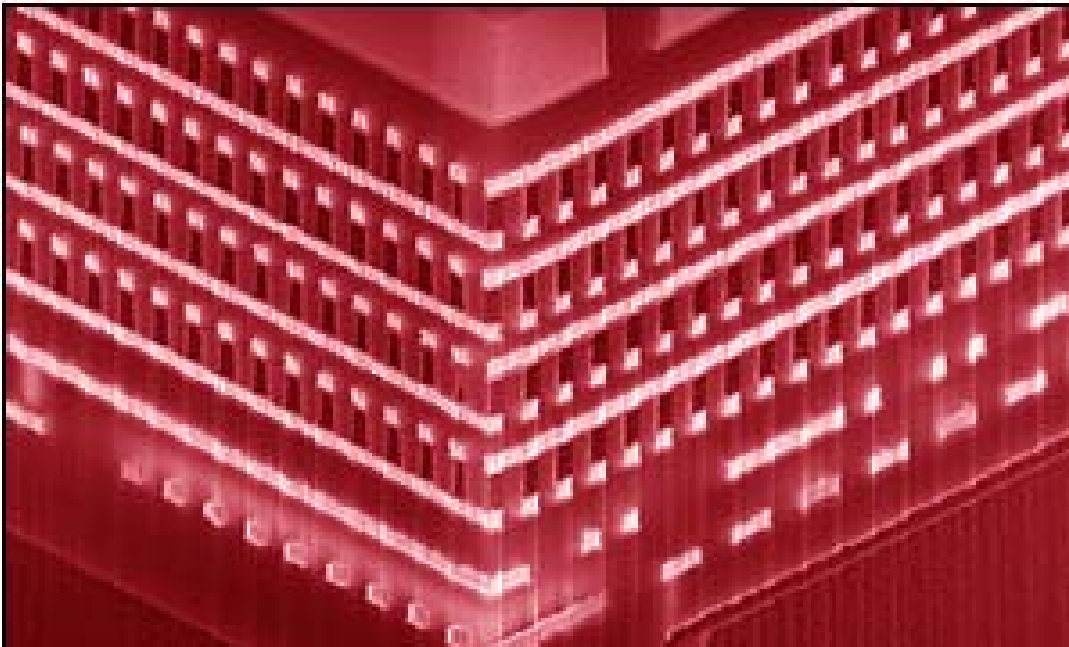


Duncan Elliott

John Koob, Tyler Brandon, Bruce Cockburn

Department of Electrical and Computer Engineering

University of Alberta, Edmonton, Alberta, Canada

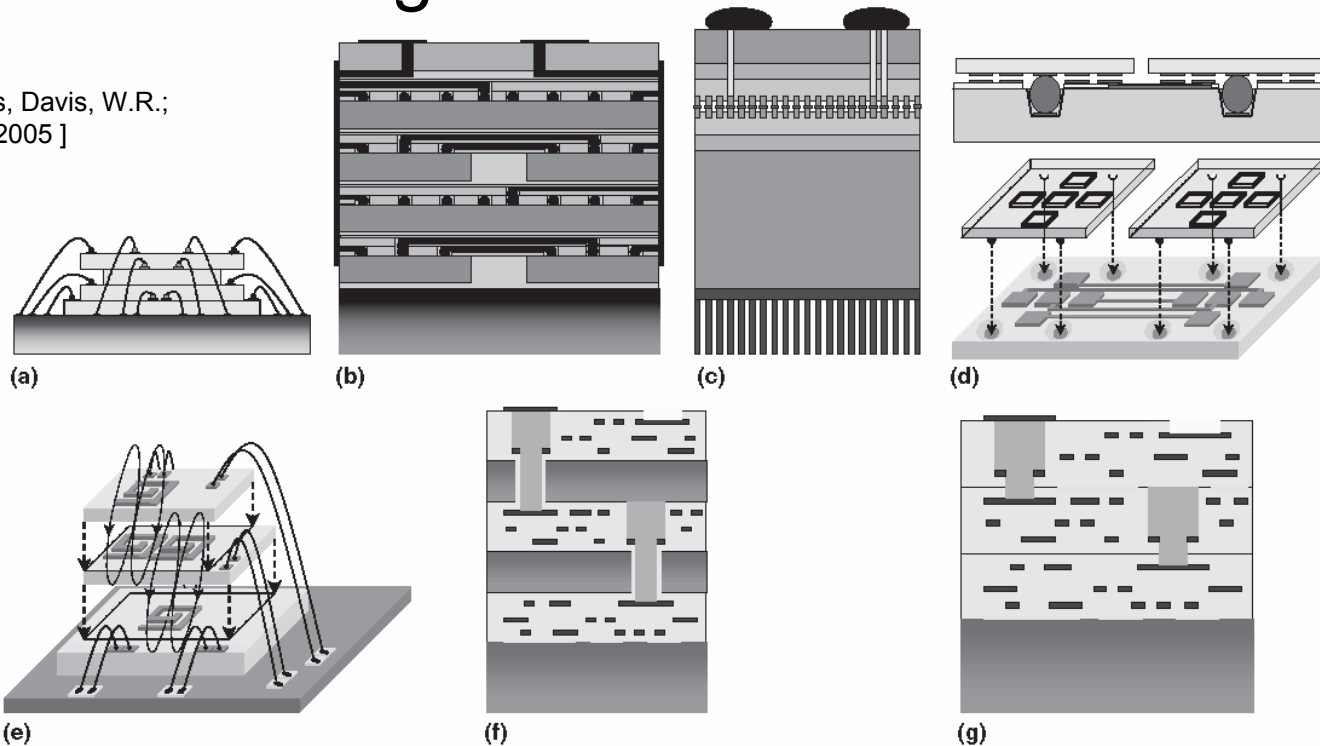


CMOS Emerging Technology Workshop, Banff 2006

What is 3D Si – a time-variant view

- ◆ Second metal layer
- ◆ 3D DRAM process: stacked or trench capacitor
- ◆ Die packaging
- ◆ Wafer stacking (“back end”)
- ◆ Monolithic 3D integration

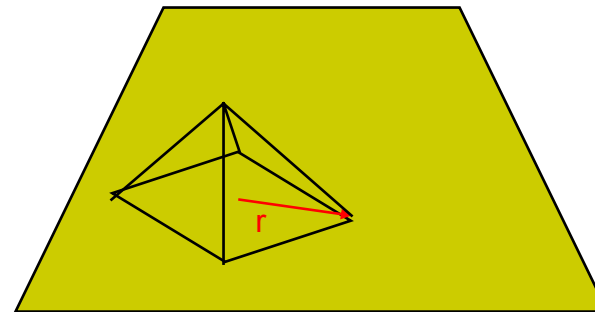
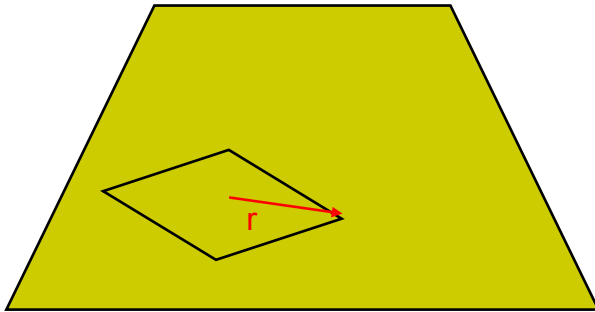
[Demystifying 3D ICs, Davis, W.R.;
Design & Test Dec. 2005]



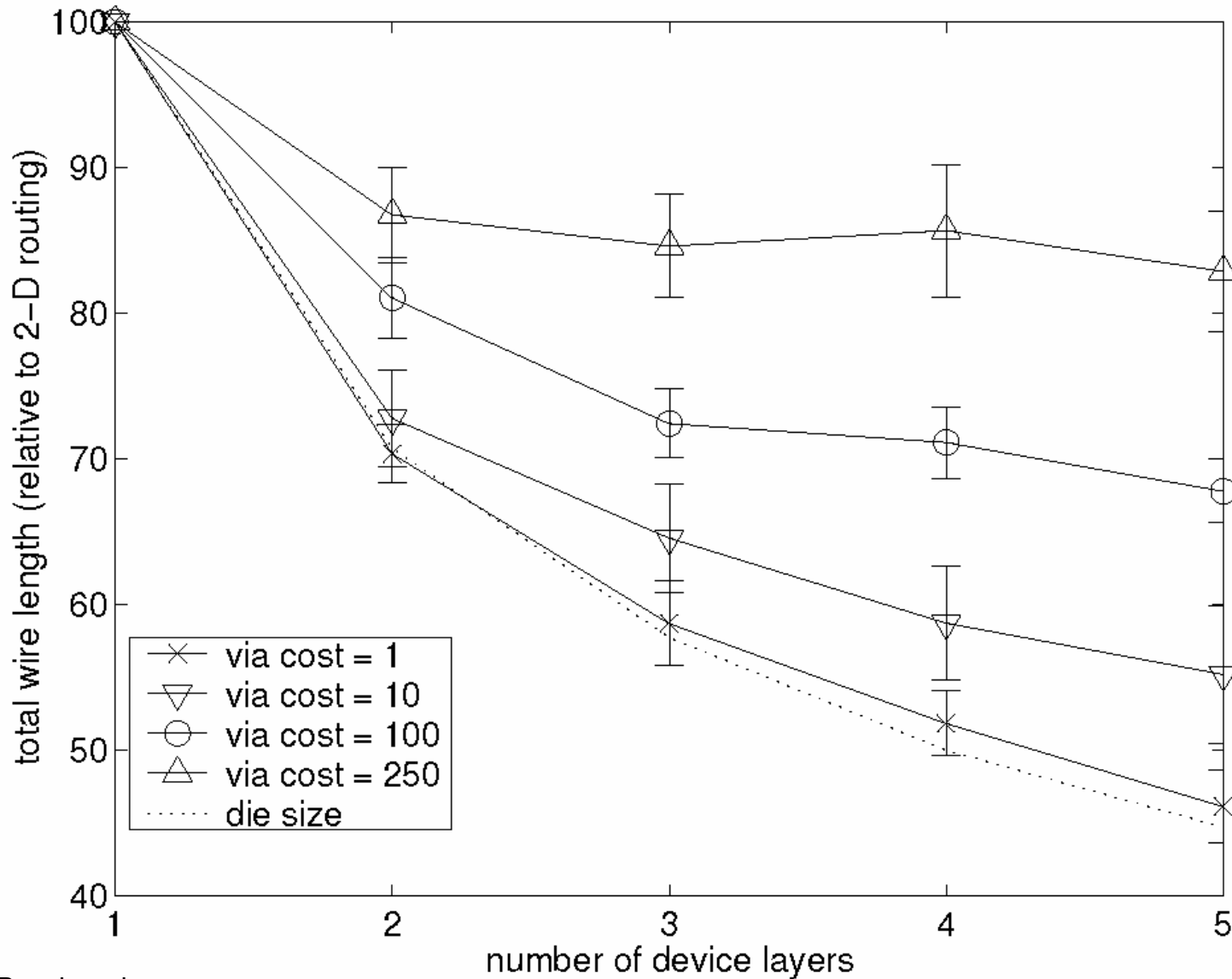
- ◆ What are the advantages
- ◆ 3D Technology
- ◆ System integration
- ◆ Challenges

3D Advantage

- ◆ Higher density, smaller, lighter
- ◆ Heterogeneous processes
- ◆ Shorter interconnect => Faster
 - ❖ e.g. 1mm wire, 10 micron interlayer pitch
50x as many gates within 3D reach in a *thick* stack



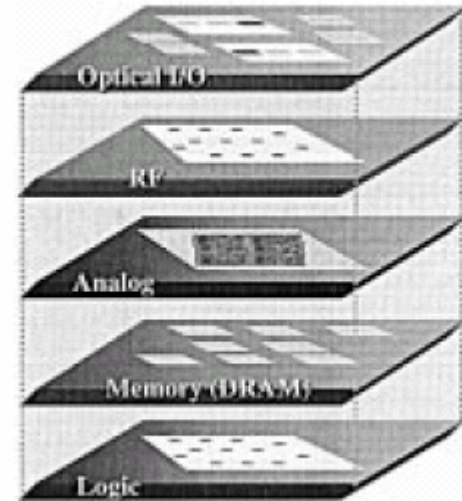
3D Meets Standard Cell Place & Route



ISPD'98 Benchmarks

Heterogeneous Processes

- ◆ DRAM & logic
- ◆ FPGA: fast logic & SRAM
- ◆ Photodiodes & CMOS



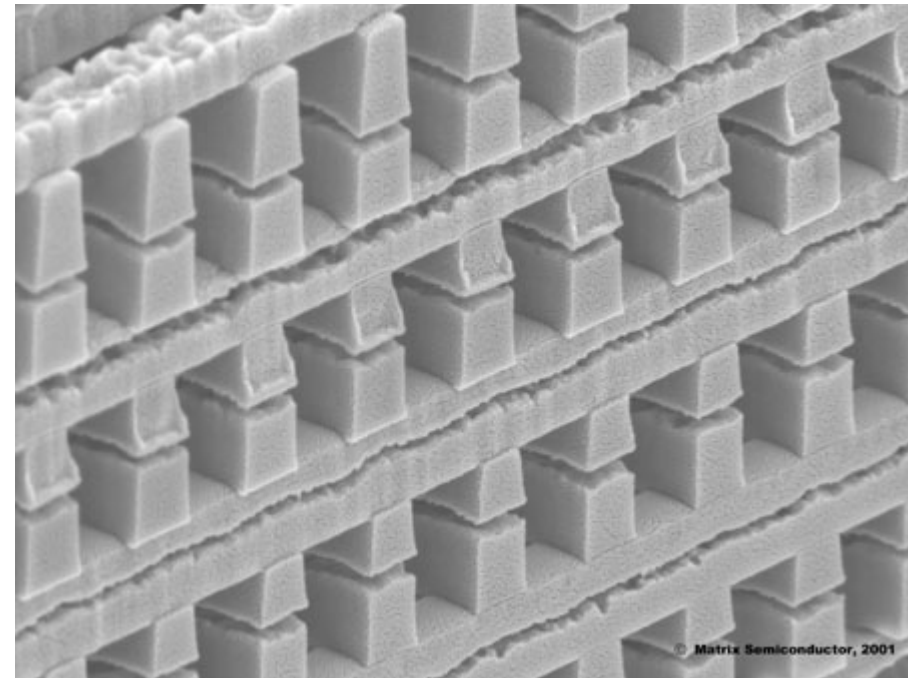
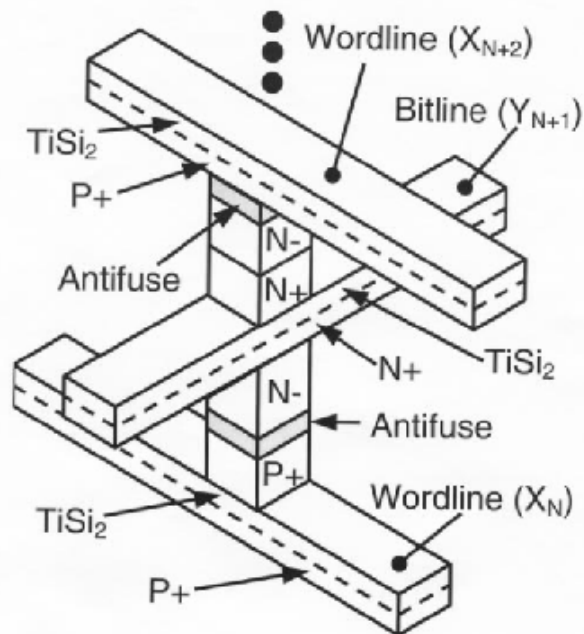
The Monolithic Dilemma

- ◆ Easy to build any number of layers of thin film transistors, but
 - ❖ Ok for LCD displays
 - ❖ Used as 4T SRAM load devices in 1990
- ◆ High f_T transistors have needed single crystal Si
 - ❖ Restricts us substrate or epi layers
- ◆ Solutions:
 - ❖ Use multiple substrates (lost any cost advantage)
 - ❖ Don't use fast transistors
 - ❖ Don't transistors

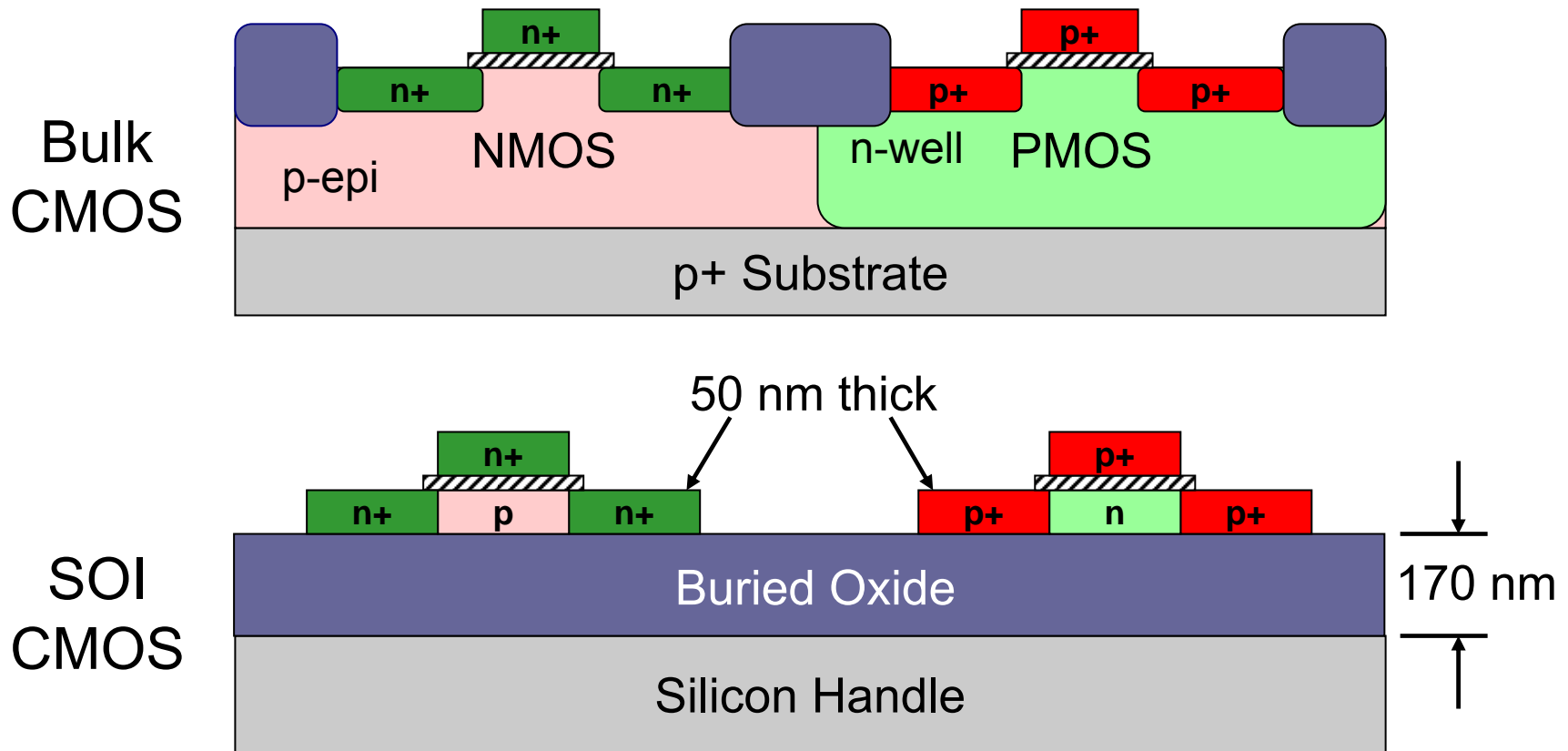
Matrix Semiconductor 3D 512Mb PROM

- ◆ Diodes only
- ◆ Bitlines and wordlines serve cells above & below
- ◆ Acquired by SanDisk Oct 2005

[512-Mb PROM with a three-dimensional array of diode/antifuse memory cells
Johnson, M. JSSC, Nov. 2003]



3D SOI Technology

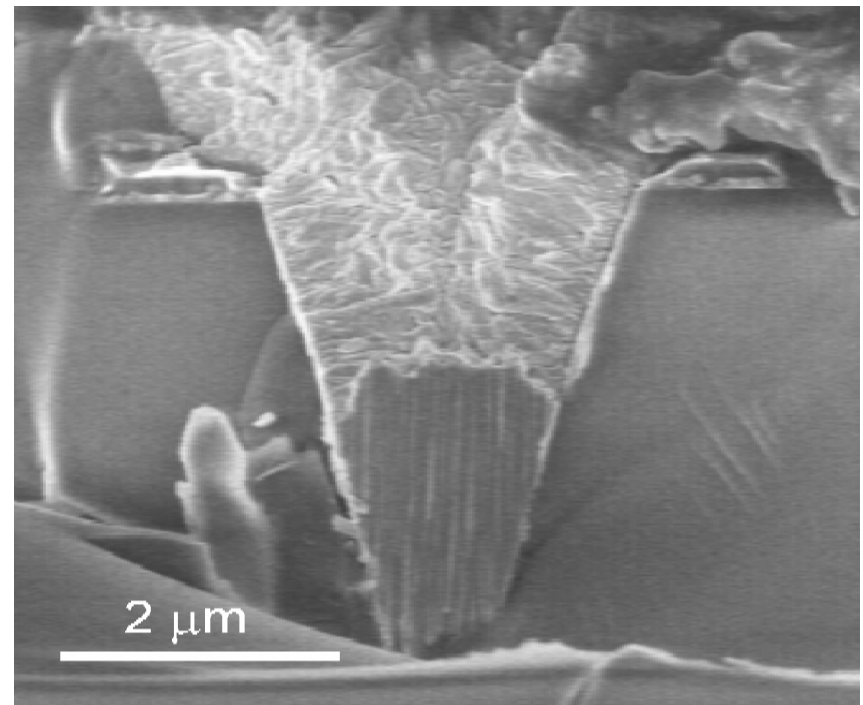
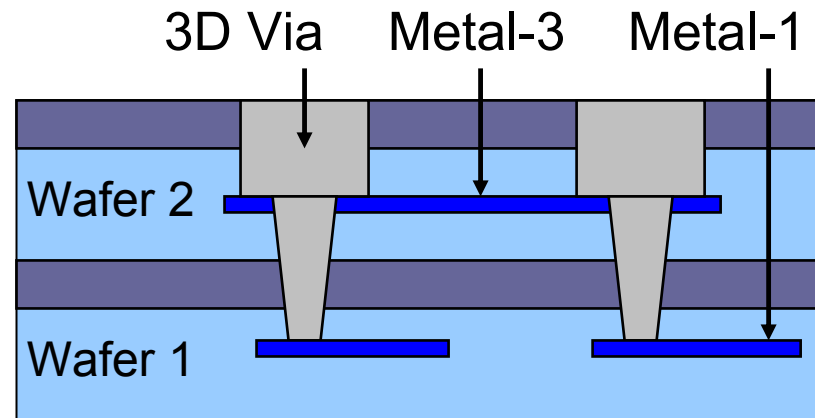


- ❖ In SOI, buried oxide provides adequate etch stop
- ❖ Mesa etched SOI requires no insulation for through wafer vias
- ❖ Feasible to fuse FD-SOI wafers together

3D SOI Technology

- ❖ Compact vertical connectivity between wafers achieved with a 6- μm -deep 3D via
- ❖ 3D vias use tungsten CVD fill
- ❖ Designs with a regular structure are suitable for extending in third dimension
- ❖ The “Glue” as evolved

[Burns, J., *ISSCC*, 2001]



3D SOI Process Flow



FIRST FD-SOI WAFER

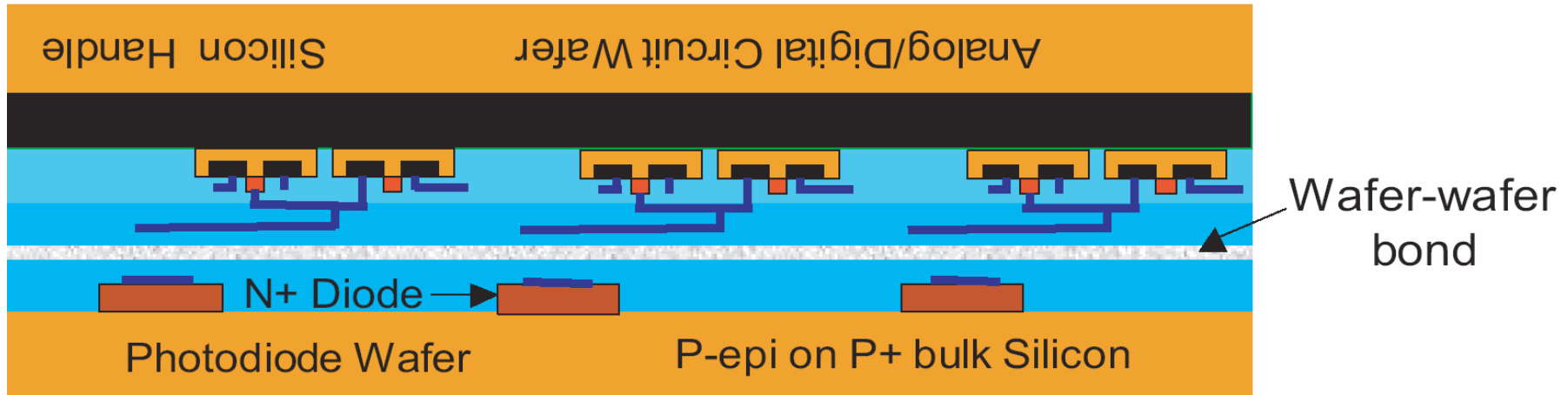


SECOND FD-SOI WAFER

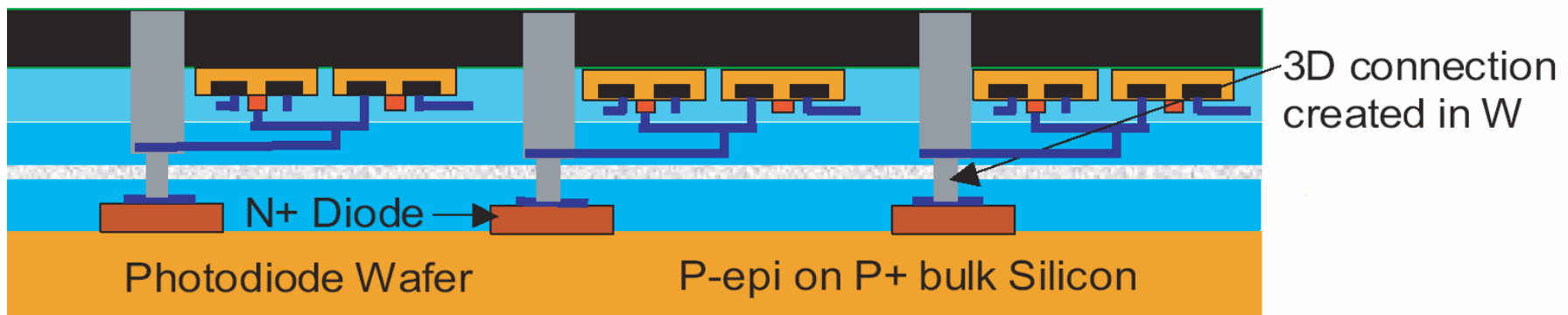


BULK PHOTODIODE WAFER

3D SOI Process Flow

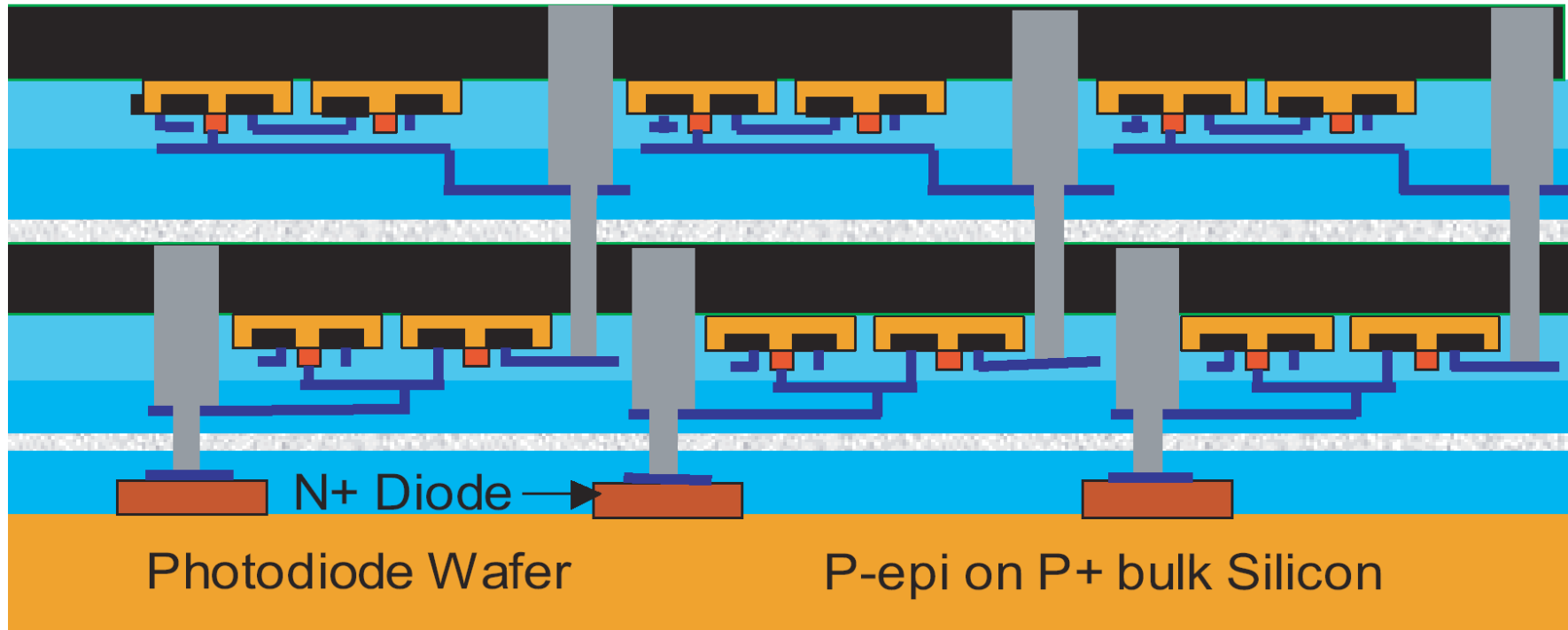


- ❖ Invert, align and bond tier 2 wafer to bulk silicon wafer



- ❖ Remove substrate from tier 2 wafer and etch 3D vias

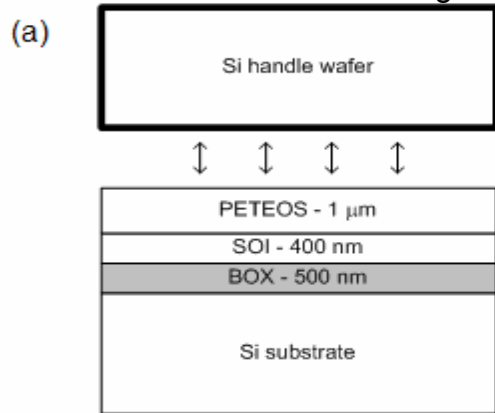
3D SOI Process Flow



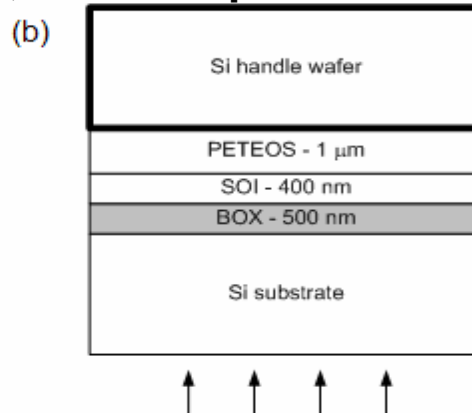
- ❖ Invert, align and bond tier 3 wafer to tier 1 - tier 2 assembly
- ❖ Remove silicon substrate from tier 3
- ❖ 3D vias connect top level metal of tier 3 to metal-1 of tier 2

Back-to-Face Silicon Layer Stacking

[C.S. Tan, A. Fan, K.N. Chen, and R. Reif, "A Back-to-Face Silicon Layer Stacking for Three-Dimensional Integration," SOI, October 2005.]

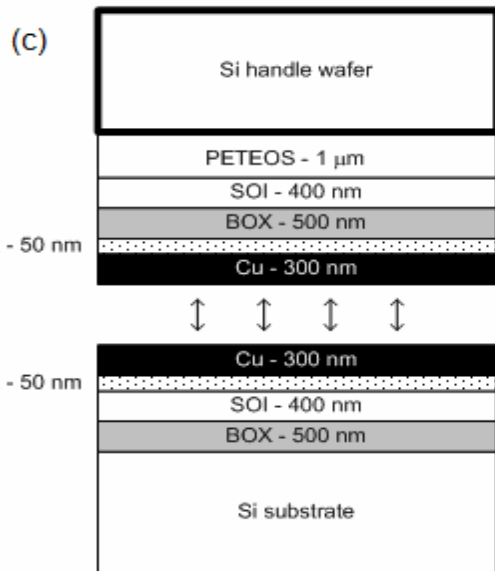
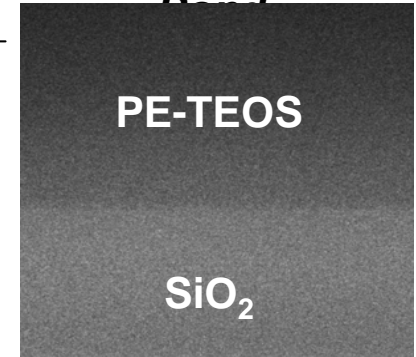


Donor wafer is bonded to handle wafer (PETEOS-to-thermal oxides bonding).

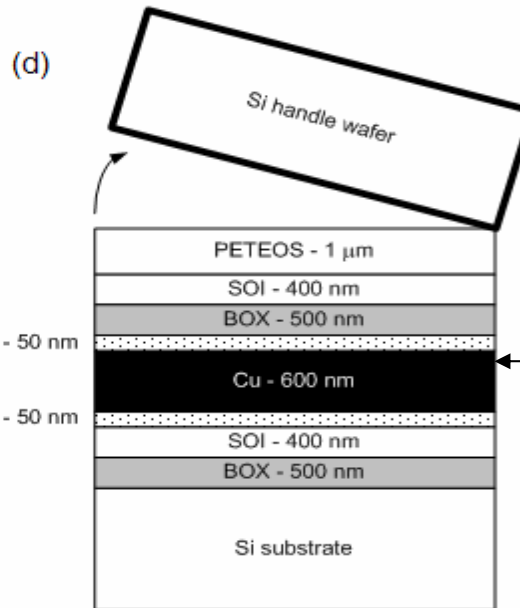


Si substrate mechanical grinding and TMAH selective strip.

Temporary Mechanical Bond

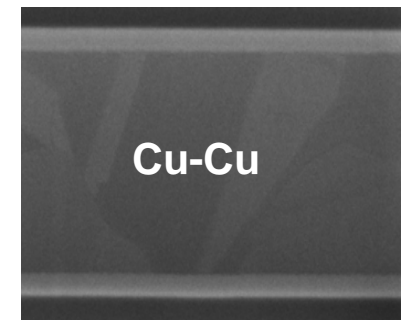


Cu-to-Cu thermocompression bonding.



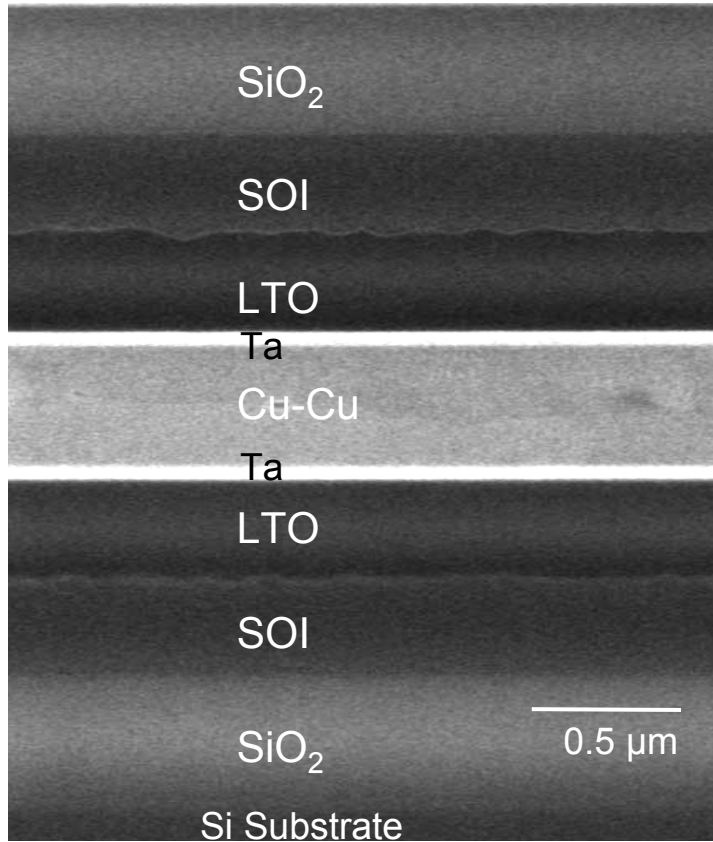
Handle wafer release.

Permanent Electrical Bond

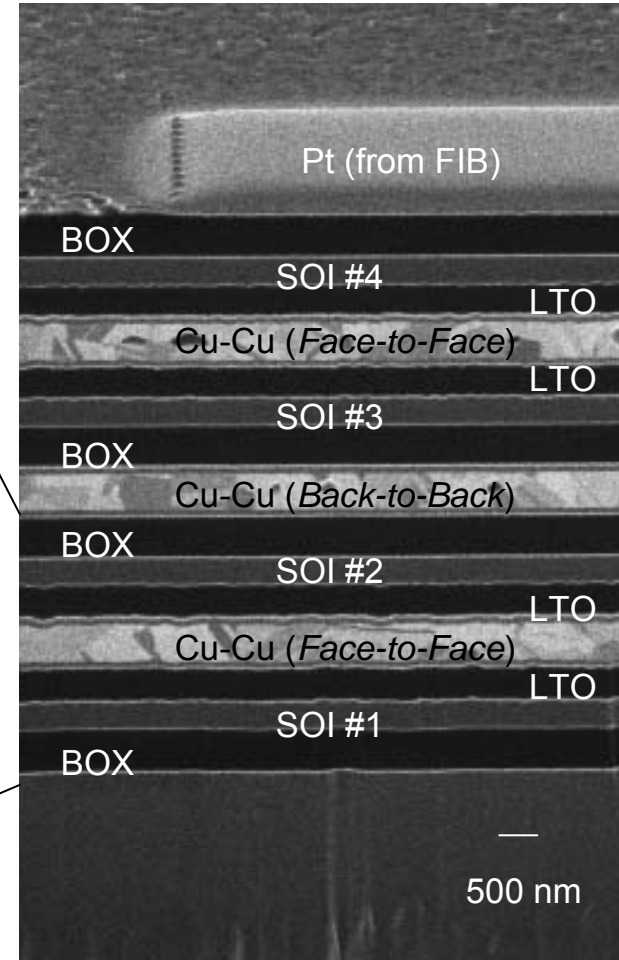


Alternative Approach: Face-to-Face Stacking

(2-Layer and 4-Layer Stack)

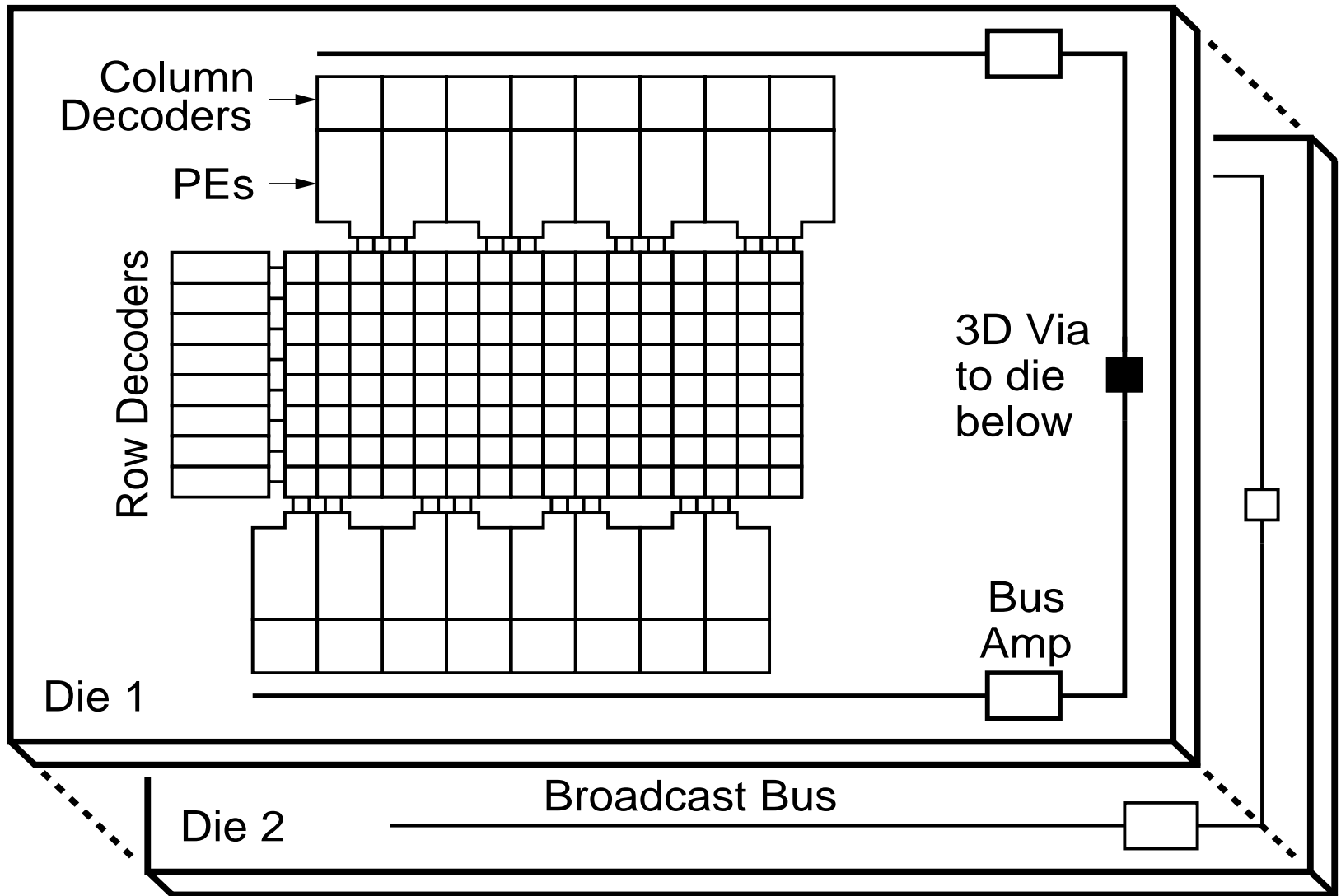


Face-to-Face bonding of two wafers and etch-back.



Bonding of two 2-layer wafers and etch-back.

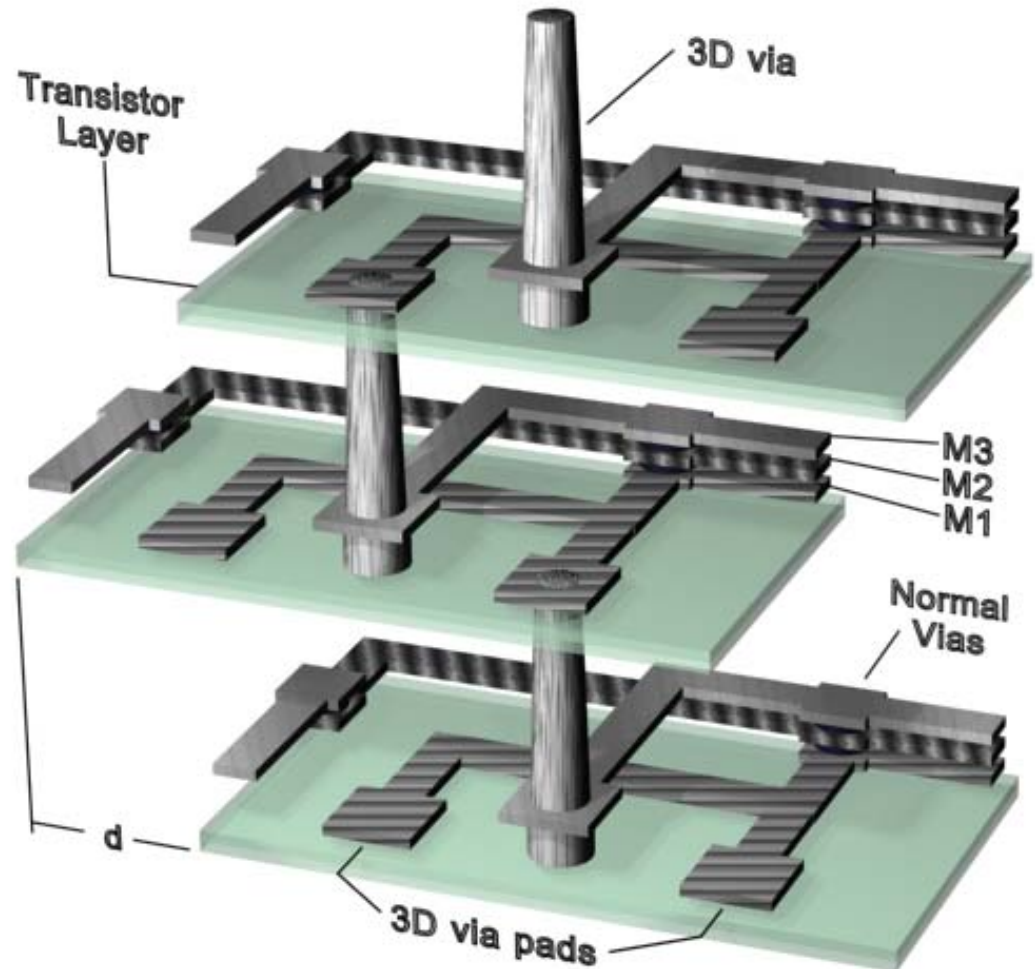
3D Computational•RAM Architecture



Stack of two identical C•RAM dies

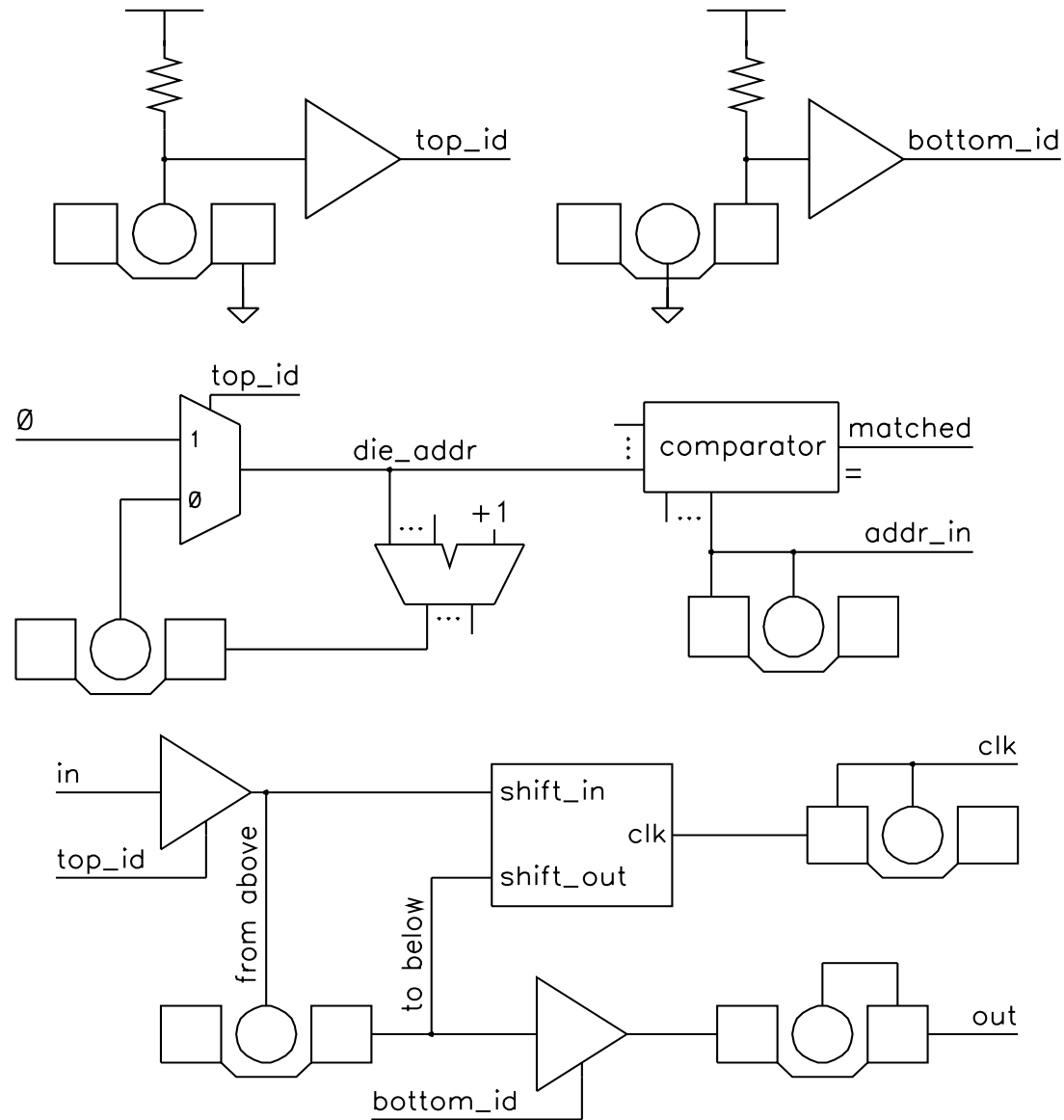
3D Interconnect Architecture

- ◆ Use identical design for all stacked dies
 - ❖ Single mask set
 - ❖ Scalable
 - ❖ Lower design and verification effort
- ◆ Pair two 3D via pads with every 3D via
- ◆ Offset every other die by distance d
- ◆ Die self-identification



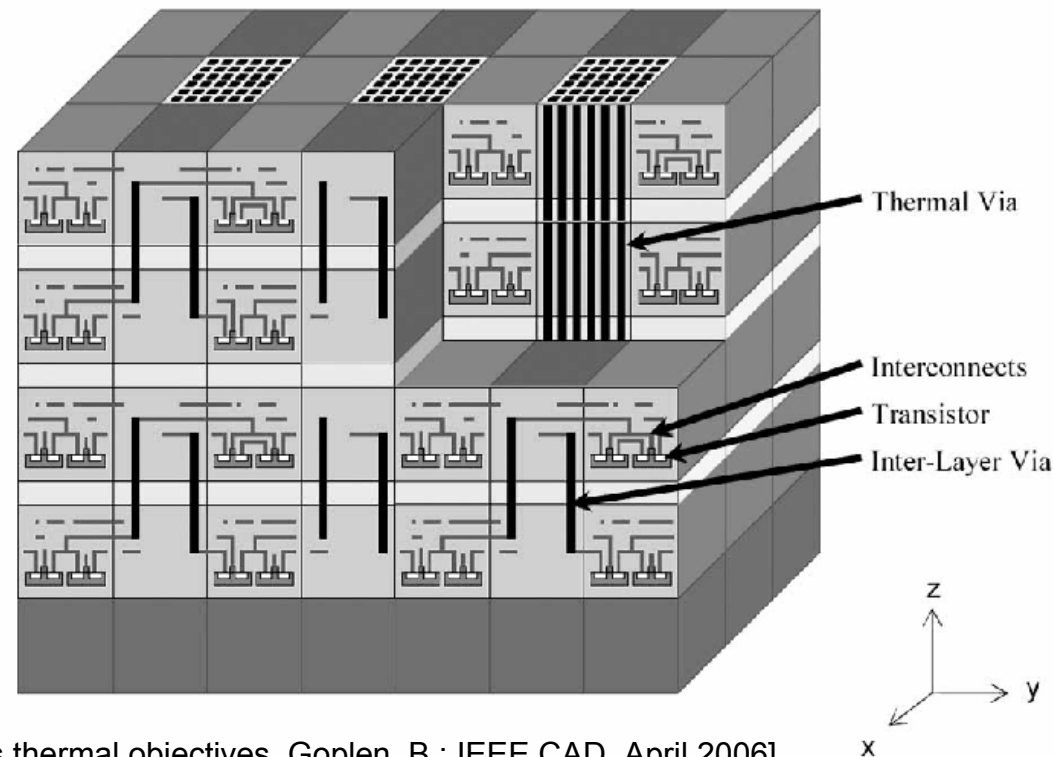
3D Interconnect Tool Box

- ◆ Simple STD cells
- ◆ Automatic die self-identification
- ◆ Pre-computed wafer addresses to permit fast address resolution
- ◆ Transfer data and state information from one wafer to an adjacent wafer



Challenges

- ◆ When stacking wafers instead of known good dies, yield falls off exponentially with # layers
- ◆ Bonding yield
 - ❖ Via resistance
 - ❖ Voids
- ◆ Heat dissipation
 - ❖ Thermal vias



[Placement of thermal vias in 3-D ICs using various thermal objectives, Goplen, B.; IEEE CAD April 2006]

Questions (& references)

- ◆ Demystifying 3D ICs: the pros and cons of going vertical, Davis, W.R.; Wilson, J.; Mick, S.; Xu, J.; Hua, H.; Mineo, C.; Sule, A.M.; Steer, M.; Franzon, P.D., Design & Test of Computers, IEEE, Volume: 22 Issue: 6 Nov.-Dec. 2005
- ◆ 512-Mb PROM with a three-dimensional array of diode/antifuse memory cells Johnson, M.; Al-Shamma, A.; Bosch, D.; Crowley, M.; Farmwald, M.; Fasoli, L.; Ilkbahar, A.; Kleveland, B.; Lee, T.; Tz-yi Liu; Quang Nguyen; Scheuerlein, R.; So, K.; Thorp, T. [Solid-State Circuits, IEEE Journal of](#), Volume: 38 Issue: 11 Nov. 2003
- ◆ C.S. Tan, A. Fan, K.N. Chen, and R. Reif, "A Back-to-Face Silicon Layer Stacking for Three-Dimensional Integration," accepted to 2005 IEEE International SOI Conference, Honolulu, HI, October 2005.
- ◆ Design of a 3-D fully depleted SOI computational RAM, Koob, J.C.; Leder, D.A.; Sung, R.J.; Brandon, T.L.; Elliott, D.G.; Cockburn, B.F.; McIlrath, L., Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume: 13 Issue: 3 March 2005
- ◆ Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology, Suntharalingam, V.; Berger, R.; Burns, J.A.; Chen, C.K.; Keast, C.L.; Knecht, J.M.; Lambert, R.D.; Newcomb, K.L.; O'Mara, D.M.; Rathman, D.D.; Shaver, D.C.; Soares, A.M.; Stevenson, C.N.; Tyrrell, B.M.; Warner, K.; Wheeler, B.D.; Yost, D.-R.W.; Young, D.J., Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International, 6-10 Feb. 2005
- ◆ Placement of thermal vias in 3-D ICs using various thermal objectives, Goplen, B.; Sapatnekar, S.S., Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Volume: 25 Issue: 4 April 2006

We thank multiple authors for contributing figures and content.

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