

Impact of (Metal) Interconnect Scaling and Process Variation on Performance

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Interconnect Applications

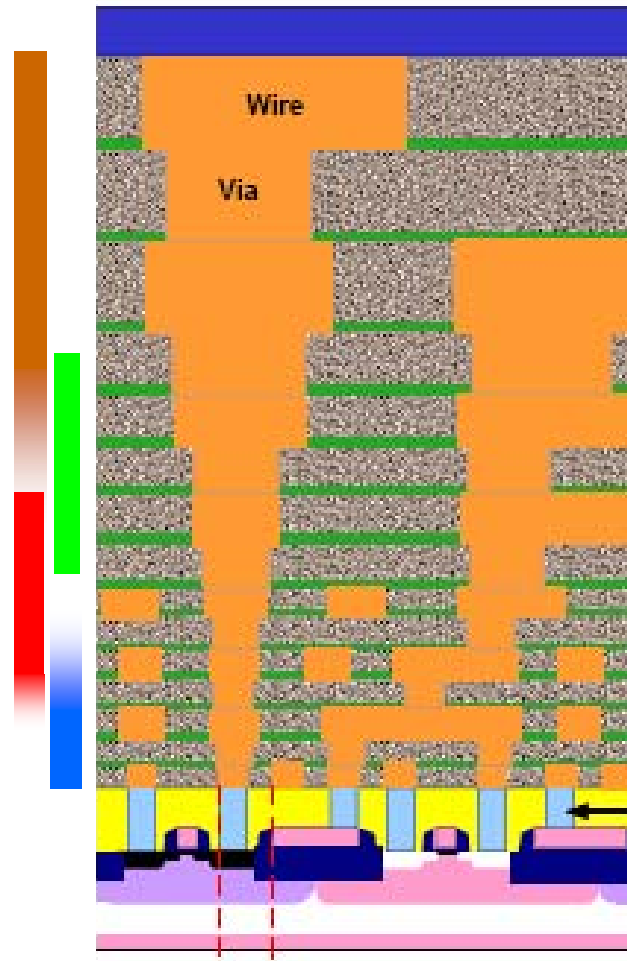
Applications

Global
Inter-Block
Routes,
Top level
power, clock dist

Local
Intra-Block
Routes

Inter-cell routing,
Local power
distribution

Intra-cell
routing



Care Abouts

Low capacitance, Low
resistance,
Moderate route density

Low capacitance,
Moderate resistance,
Moderate route density.

Low capacitance,
high route density

Figure from ITRS

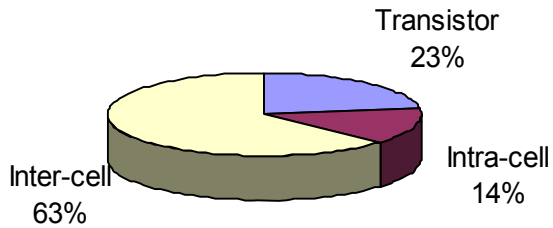
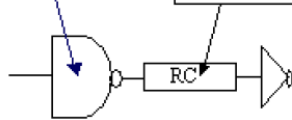


Interconnect Impact on Performance

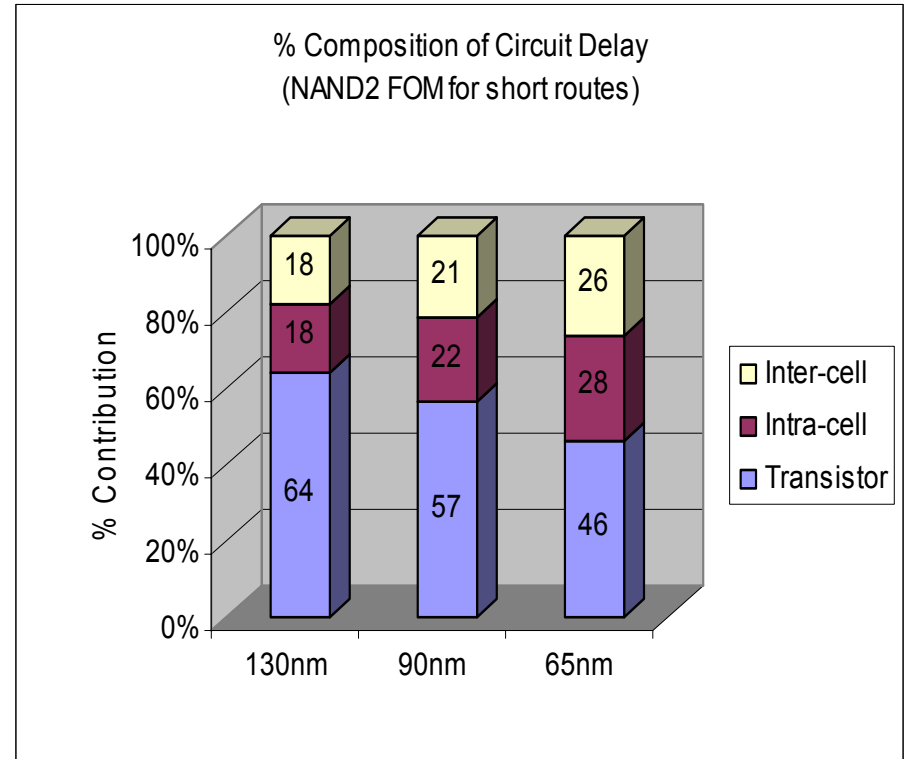
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<p>Intra-Cell (within cell) Parameters Contact, VIA, Diffusion, POLY and metal resistance Contact-to-gate, contact-to-contact, POLY, metal and via capacitance</p>	<p>Inter-Cell (between cells) Parameters Metal and VIA resistance Metal capacitance</p>
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An example of interconnect dominated circuit



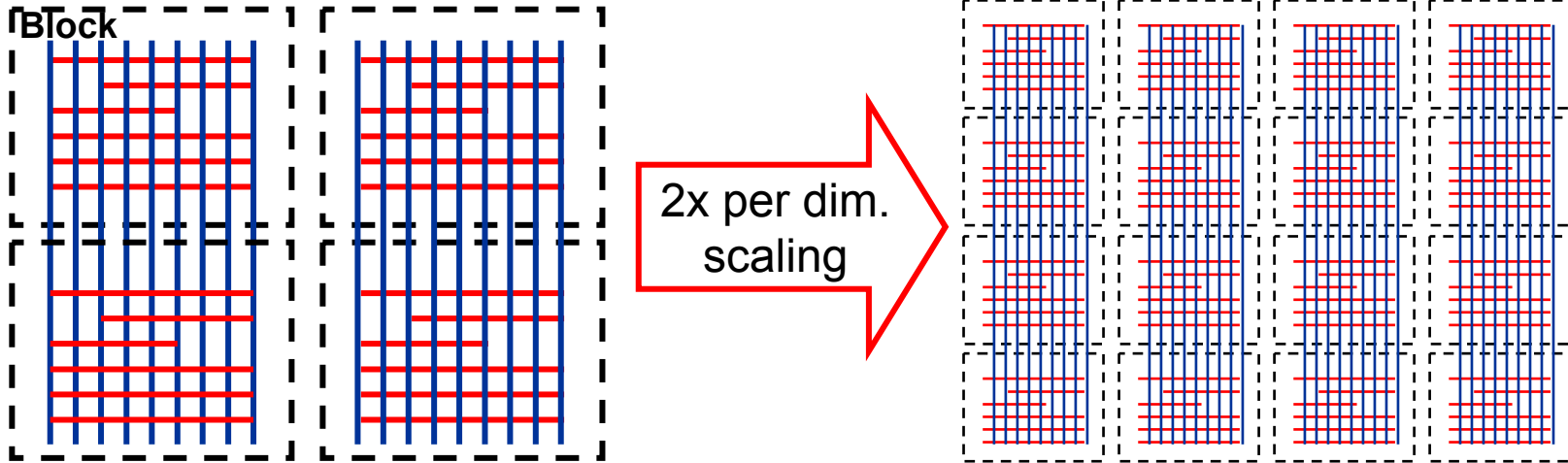
Interconnect significant part of wire delay even for gate dominated paths



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Wire Length Scaling



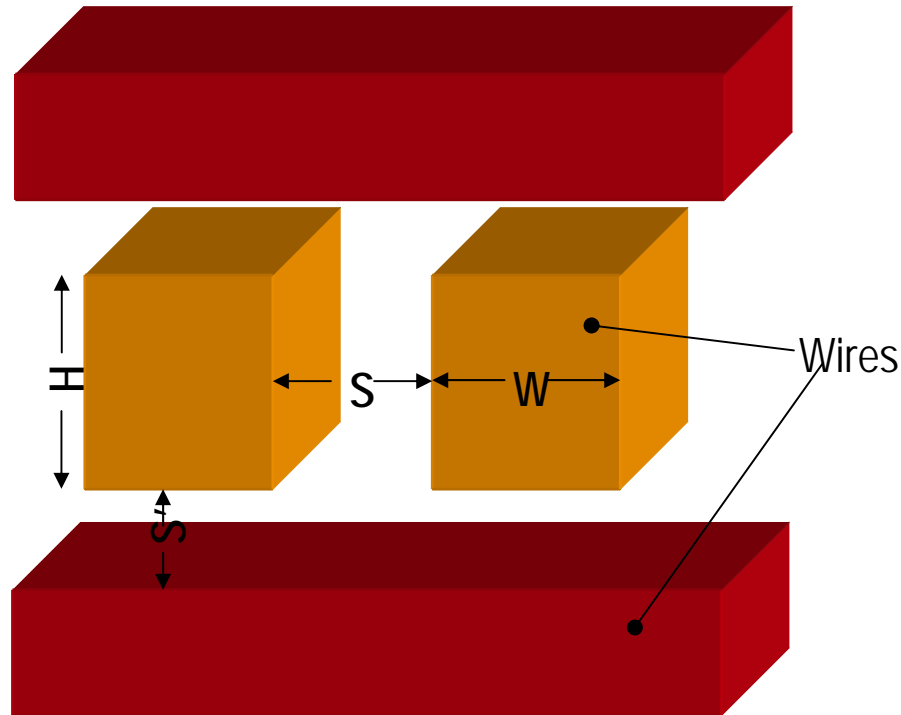
- Global Wires (between blocks)**
 - Length does not scale as more blocks are added to get higher integration
- Intra-Block Wires**
 - Length does scale but it may be less than general scaling due to increasing functionality
- Intra-Cell Wires**
 - Length scales generally but more restrictive design rules could cause problems



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Wire Cross-Section Scaling



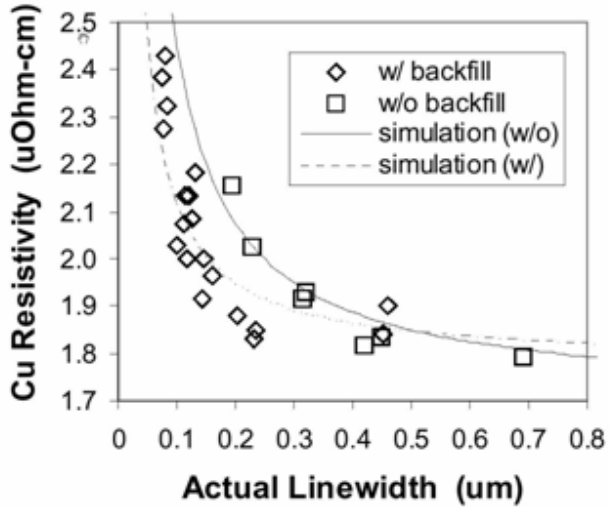
- Wire Cap. per μm (C_w) = $\epsilon_1 \cdot H/S + \epsilon_2 \cdot W/S'$
- Wire Res. per μm (R_w) = $\rho/H \cdot W$, where ρ is resistivity
- If everything is scaled by α (0.7x per gen.),
 - Wire cap. per μm scales by 1
 - Wire res. per μm scales by $1/\alpha^2$ (2x per gen.)
- Dielectric constant is slowly decreasing
- However ...



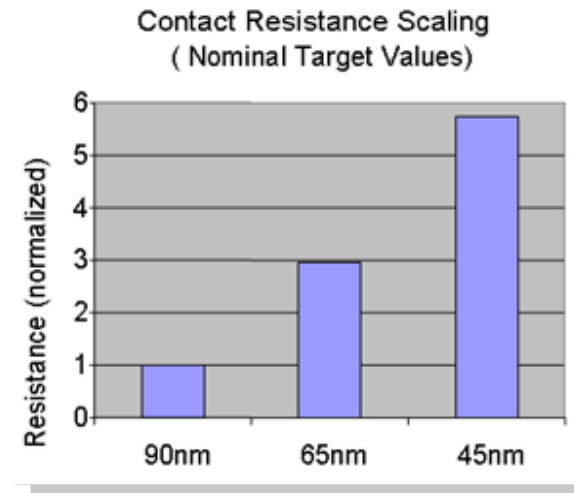
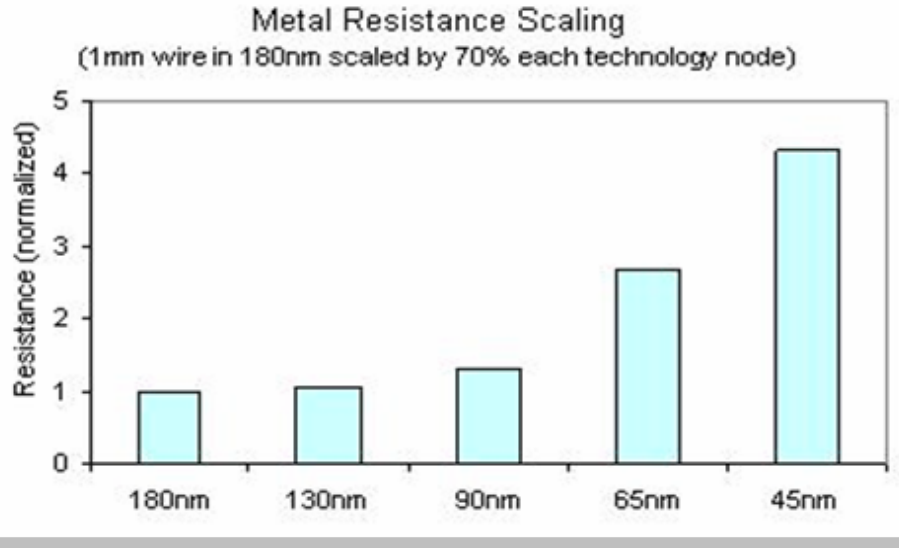
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Resistance is Increasing



Jiang et. al., Proc. IITC, 2001

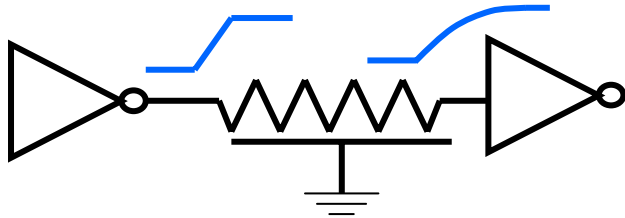


- ❑ Metal resistivity is increasing
- ❑ Via resistance is also increasing



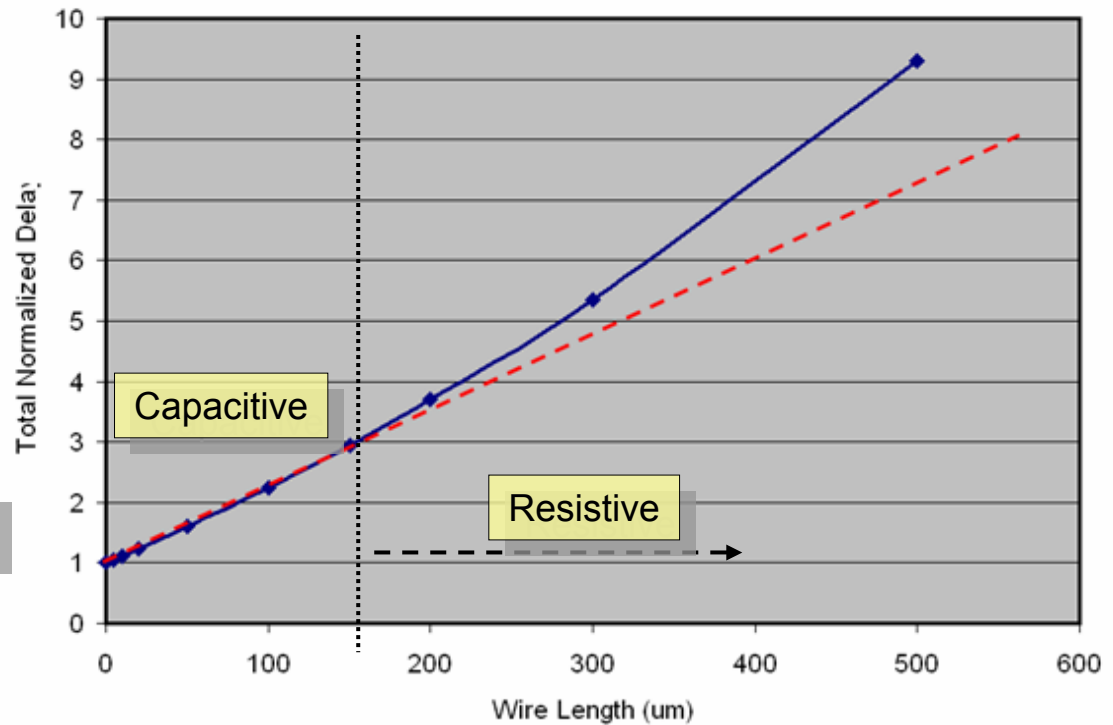
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$$\text{Delay} \sim T_{\text{int}} + R_t \cdot C_w \cdot L + R_w \cdot C_w \cdot L^2$$

Wire Delay vs Length



❑ Short Wires (Local and some Intra-Block Wires)

- Resistance of transistors \gg resistance of wires
- Delay $\sim L$

❑ Long Wires (Some Intra-Block and Global Wires)

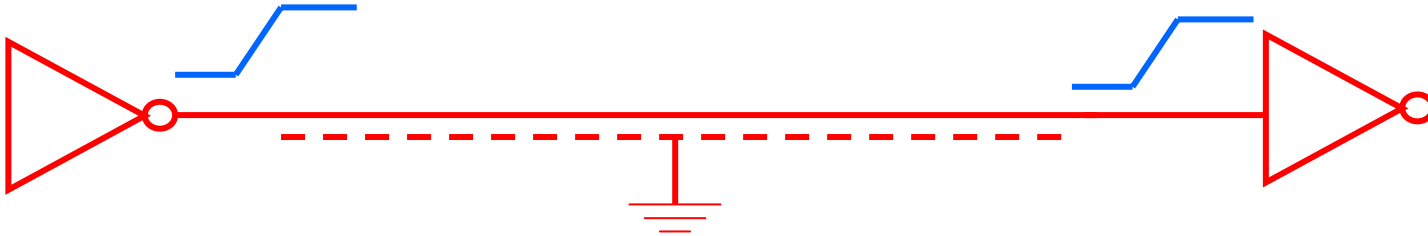
- Resistance of wire is important
- Delay $\sim L^2$



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Short Wire Scaling



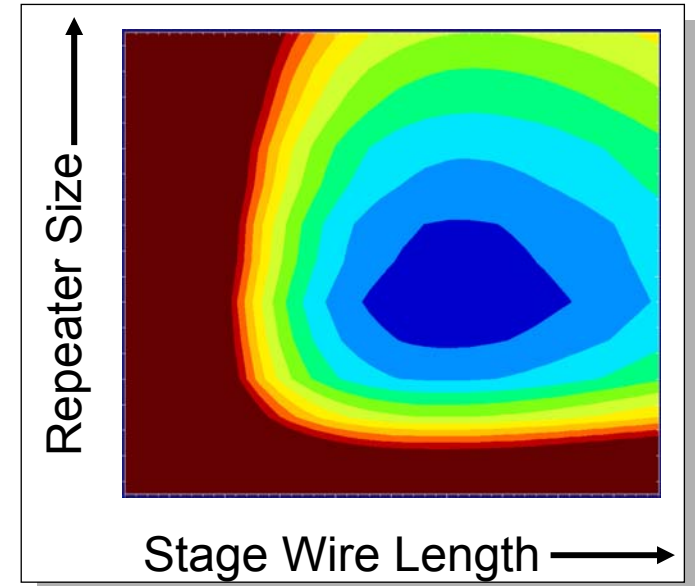
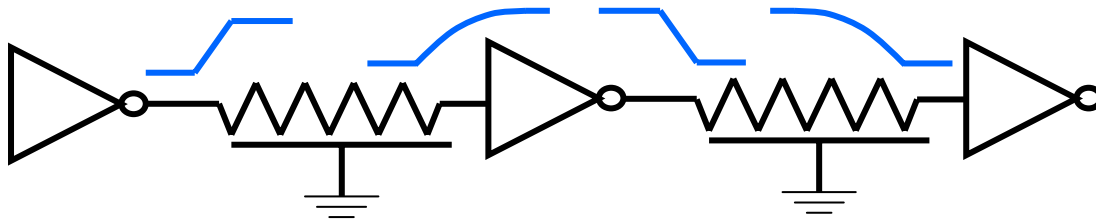
- Wires short enough that wire resistance can be ignored.
- Gate delay is given by: $T_{int} + C_w \cdot R_t \cdot L$
- Intrinsic gate delay scales by α
 - Actually a bit less than α due to process limitations and leakage
- Wire length scales by α (unless block complexity increases)
- For “short” wires (with expected length scaling) we can keep up with the transistors.



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Global Wire Delay Scaling



Transport Delay per unit length contours

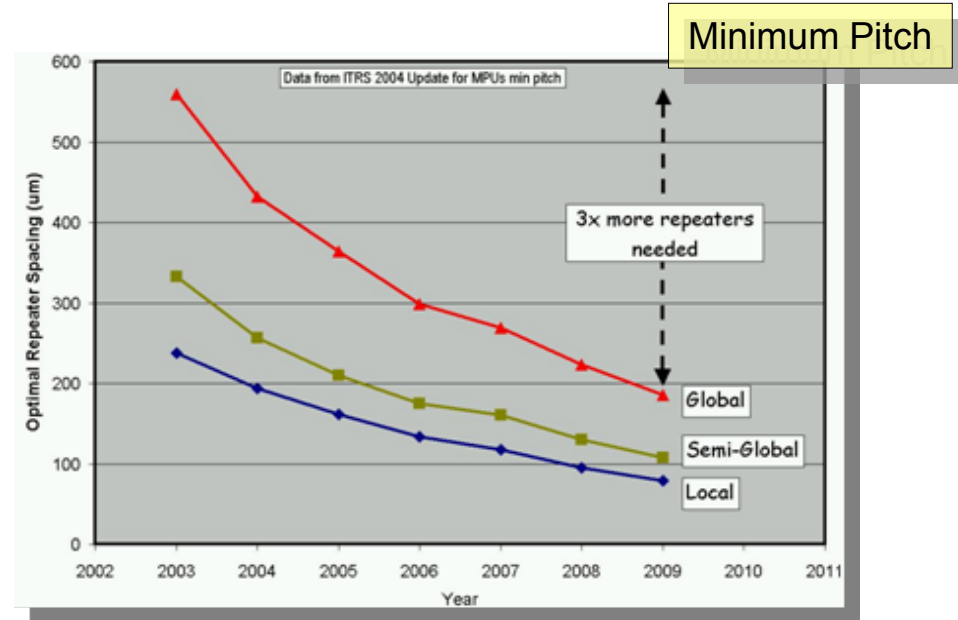
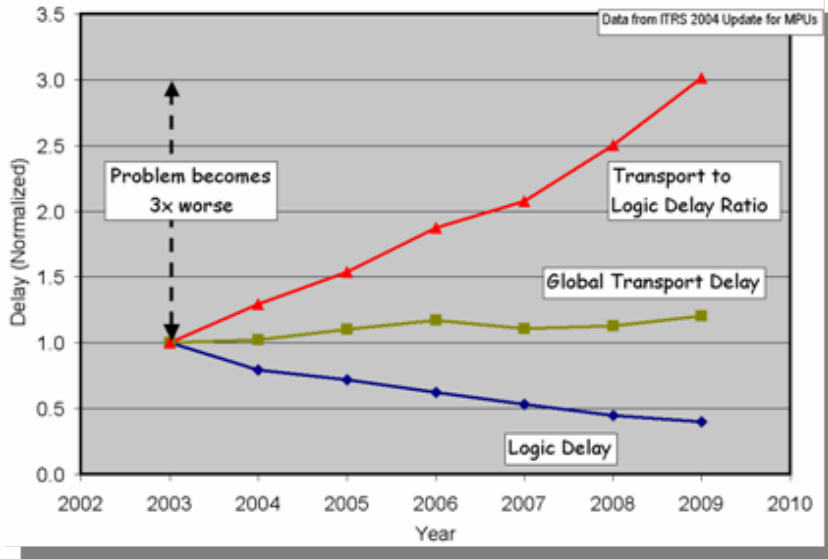
- ❑ There is an optimal repeater size and stage wire length for minimum transport delay
- ❑ Wire delay now scales as L and not L^2



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Optimal Routing Scaling



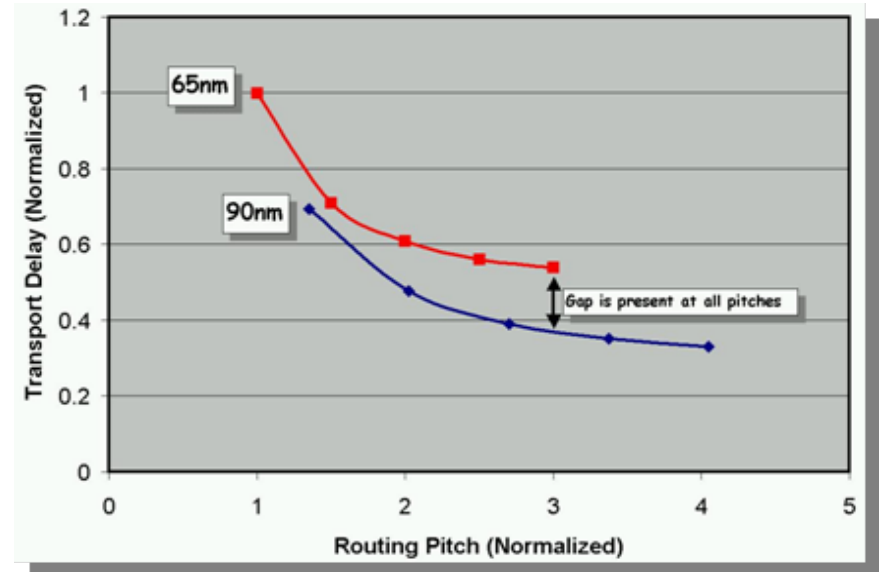
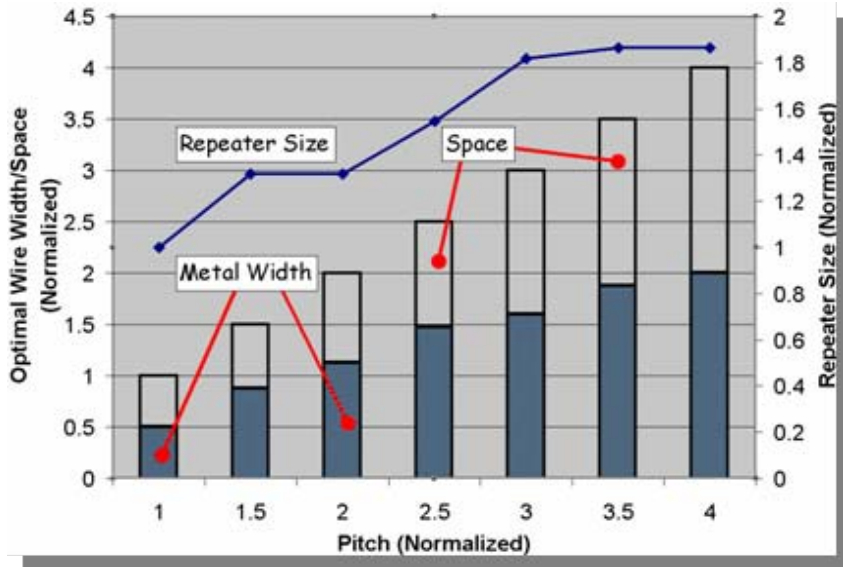
- Optimal wire length per stage is scaling down with technology
- Global wires show reduction in performance with scaling
- Long block level wires are affected too
- More repeaters are needed increasing area and power



Solutions: Architecture & Implementation

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- Route critical signals on a wider pitch**
 - However, for large pitches the gains saturate
 - Transport delay of older processes cannot be matched by newer process at any pitch
- Comprehend transport delay in architecture**
 - Scaling will change number of clock cycles need to communicate between blocks
- Cell placement taking wires into account**

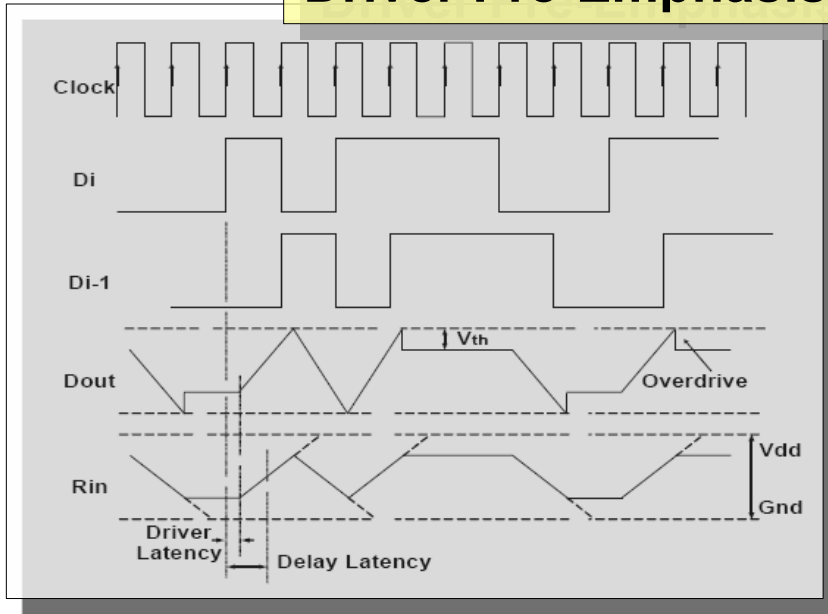


Solutions: Circuit – Some Examples

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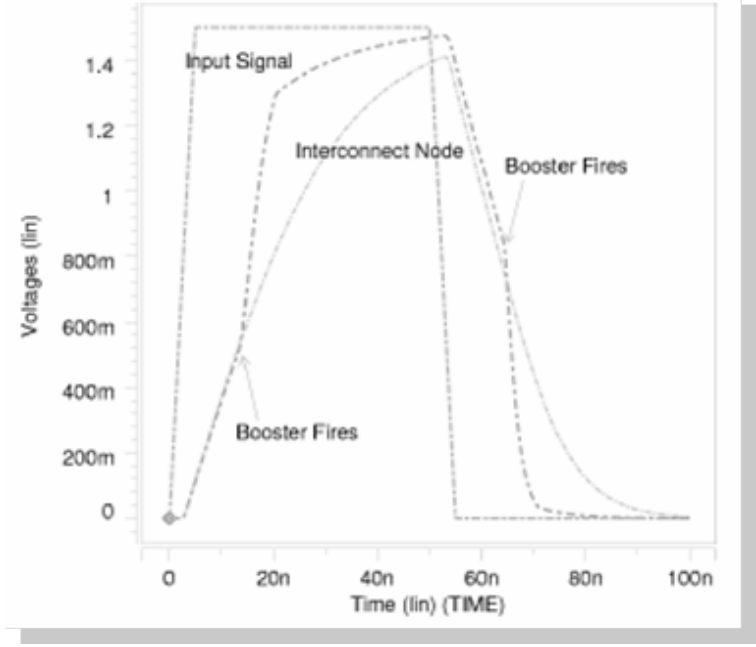
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Driver Pre-Emphasis



L Zhang et al, ISLPED 2005

Boosters



A Nalamalpu et al

❑ Circuit solutions to speed up long wires exists

- ~20-30% reduction in transport delay
- More complexity and unfamiliarity with designers
- Integration challenges

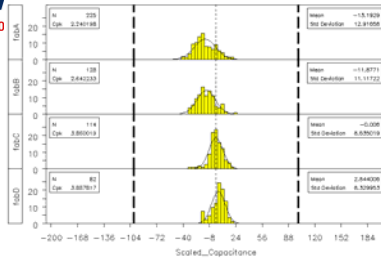


Interconnect Variations

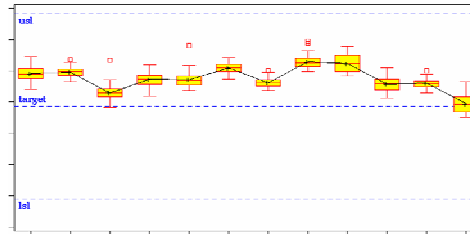
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Fab-to-Fab

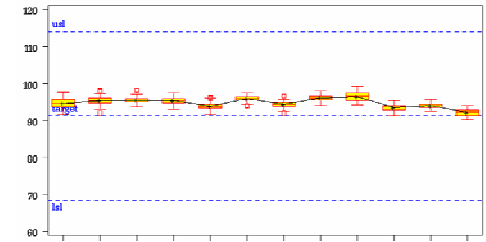


Lot-to-Lot



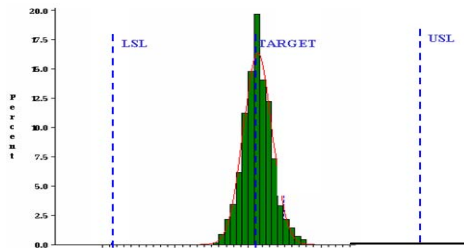
Lot number

Wafer-to-wafer



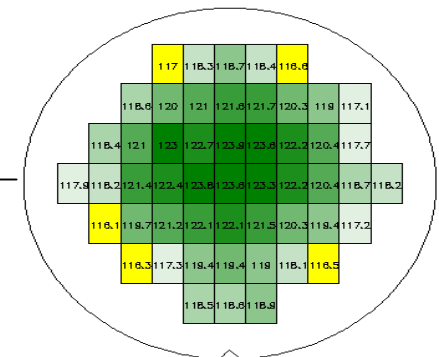
Wafer number

Within-Die

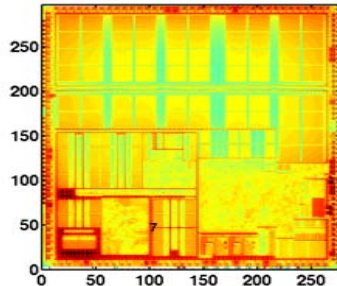


Interconnect Variations

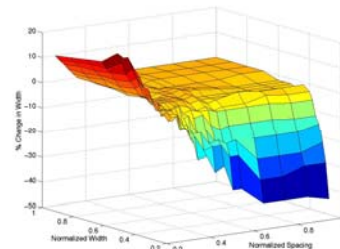
Die-to-Die



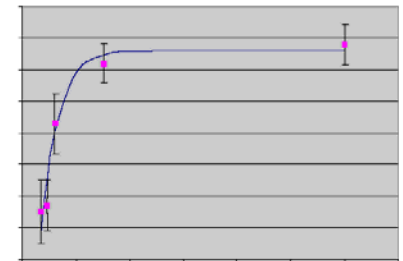
Copper Loss (Chip 10)



CMP



Selective Process Bias



Etch effect

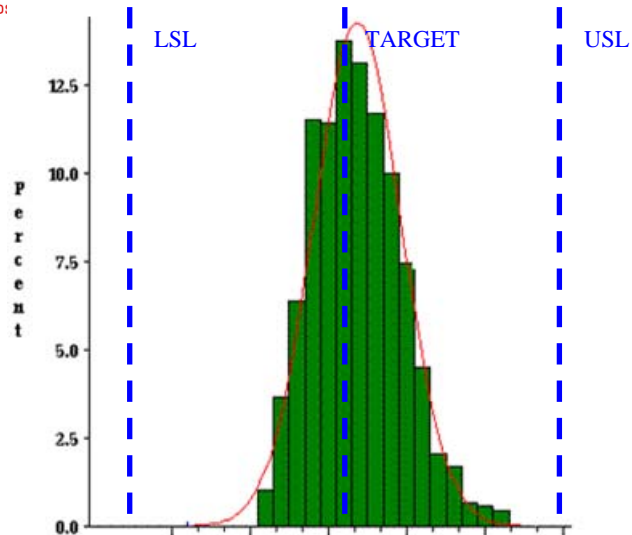


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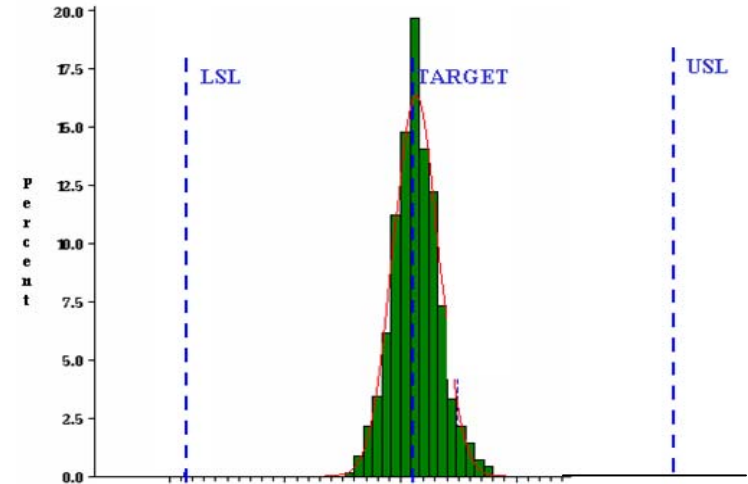
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Interconnect Variations

Metal Resistance



Metal Capacitance



- Variations are caused by random or predictable process effects
- Total variation is composed of on-die and die-to-die variation
- Variation is an issue when there is a “race”
 - For example: Data from one flop has to make it to the next before the next clock

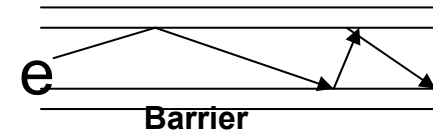


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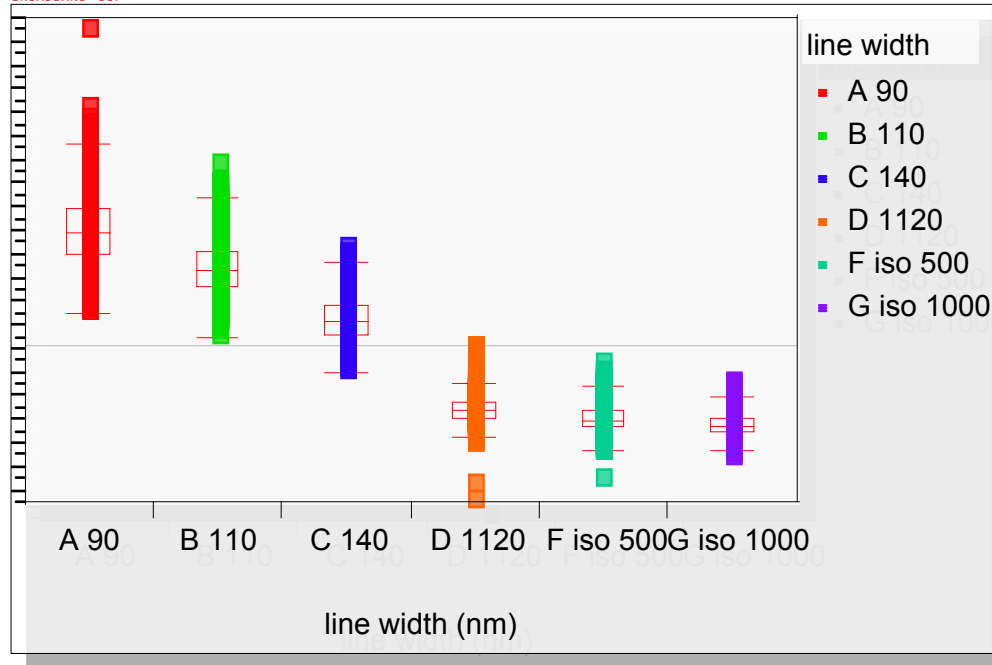
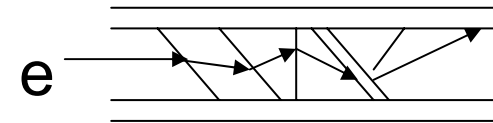
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Wire Resistance Variations

Surface



Grain Boundary



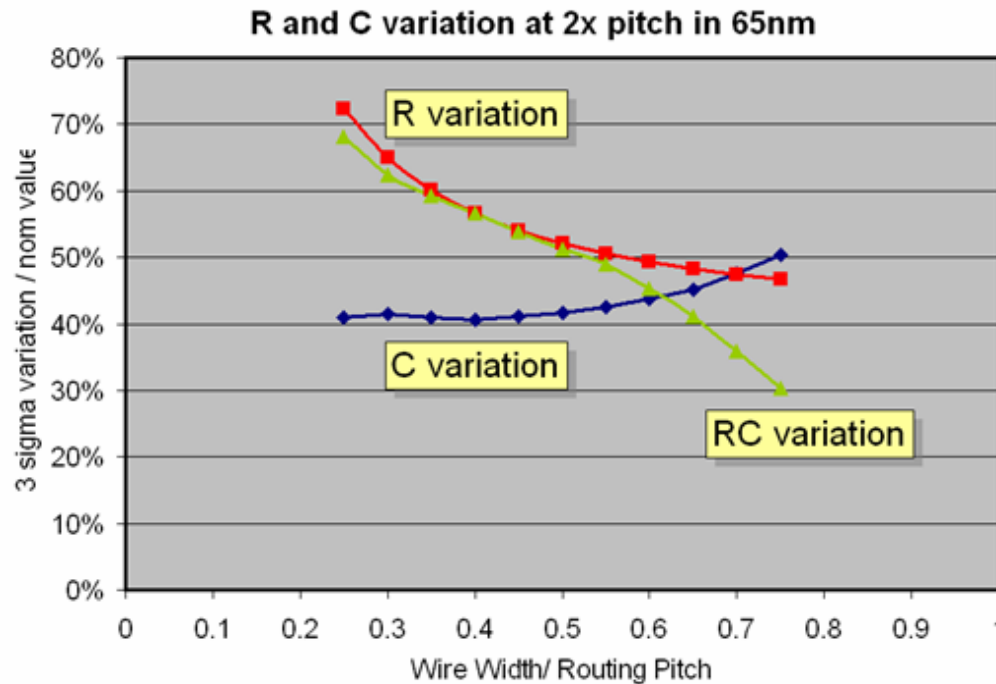
- Wire R variation increases for small widths
- CD variations cause a larger change in resistivity at small W
- R variation will get worse with scaling!



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Wire R and C variations



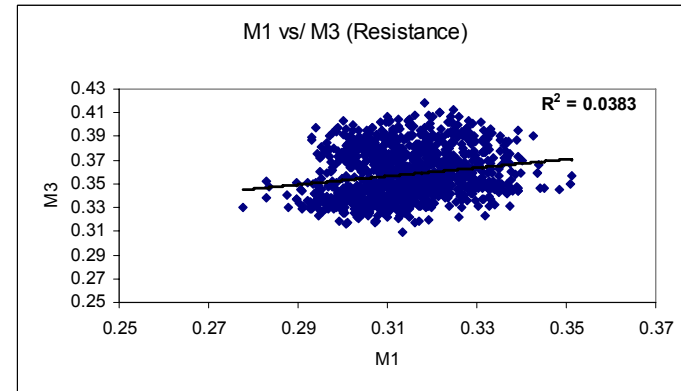
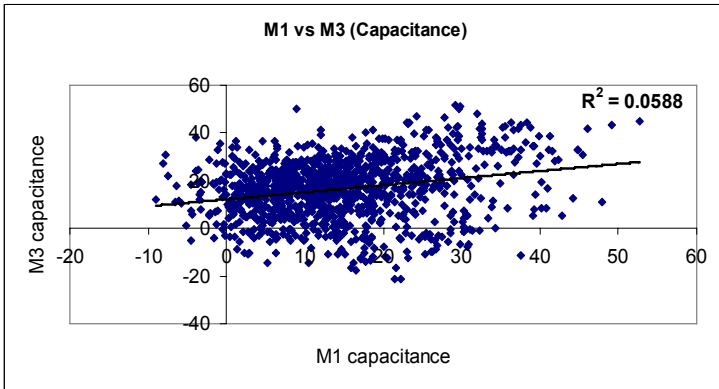
- C variation increases for smaller spaces
- R variation is larger than C variation for most widths
- RC variation decreases for large W
- Select a $W \gg W_{\min}$ to reduce variation with some increase in power
- Larger W also needs a larger driver, reducing device variations too!



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Inter-Level R and C Correlations



		130nm Capacitance				
		M1	M2	M3	M4	M5
M1		1.00	0.18	0.06	0.05	0.29
M2			1.00	0.00	0.16	0.21
M3				1.00	0.09	0.10
M4					1.00	0.16
M5						1.00

		130nm Resistance				
		M1	M2	M3	M4	M5
M1		1.00	0.08	0.04	0.07	0.06
M2			1.00	0.03	0.03	0.23
M3				1.00	0.09	0.07
M4					1.00	0.10
M5						1.00

- Data from multiple lots show that any two metal levels are weakly correlated to each other
 - Co-efficient of correlation is small (varies from zero to 0.29)
 - This can be attributed to random process effects
- Don't have to design for full 3 sigma intra-chip variation for each parameter
- Do have to design for full inter-chip variation



- Model more variations instead of lumping them into random**
- Use multiple clocks with lower frequencies for communications over larger distances**
 - Asynchronous if application permits
 - Split clocks as late as possible
- Use of skew tolerant flops or latches**
 - Variation between successive paths gets averaged
 - Hold time issues
 - More complexity
- Supply Voltage or Back Bias Scaling**



Conclusions

- ❑ **Interconnects have increasing effect on performance**
- ❑ **Wire resistance is causing a disconnect between device and wire delay scaling**
- ❑ **Wire variations are increasing with scaling too**
- ❑ **Judicious choice of physical implementation, circuits and architecture needed to keep up with device scaling**