

Inductive-Coupling Inter-Chip Link for System in a Package

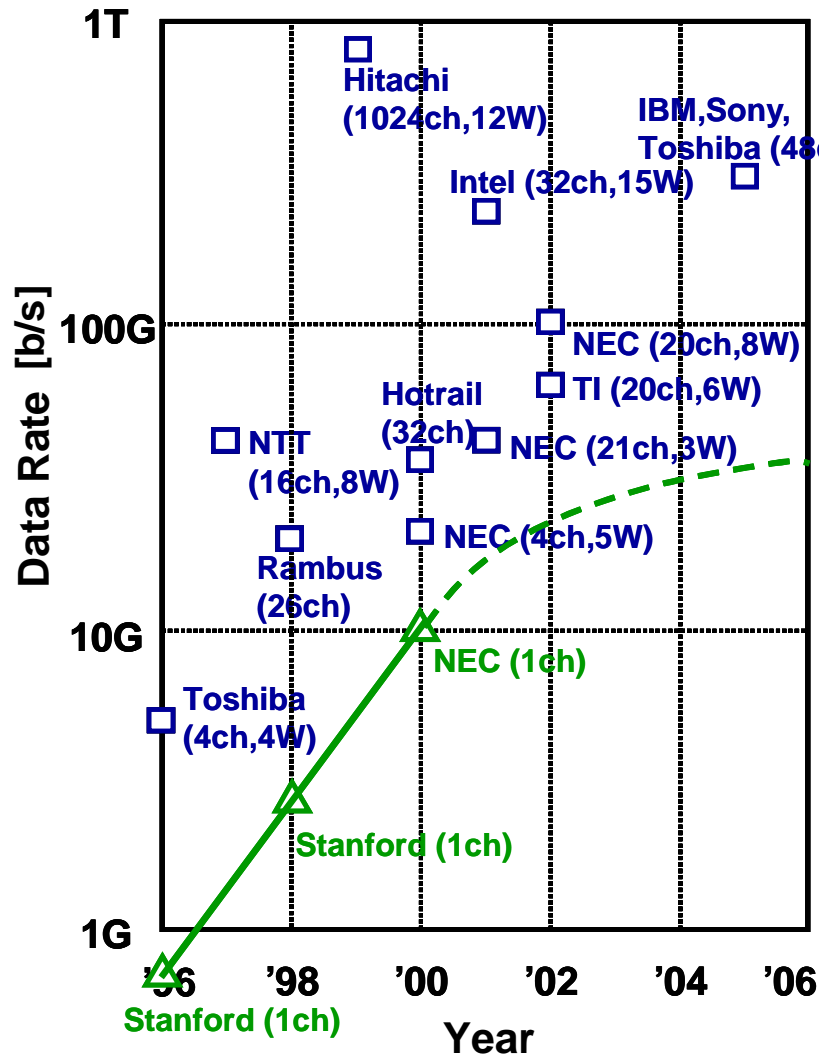
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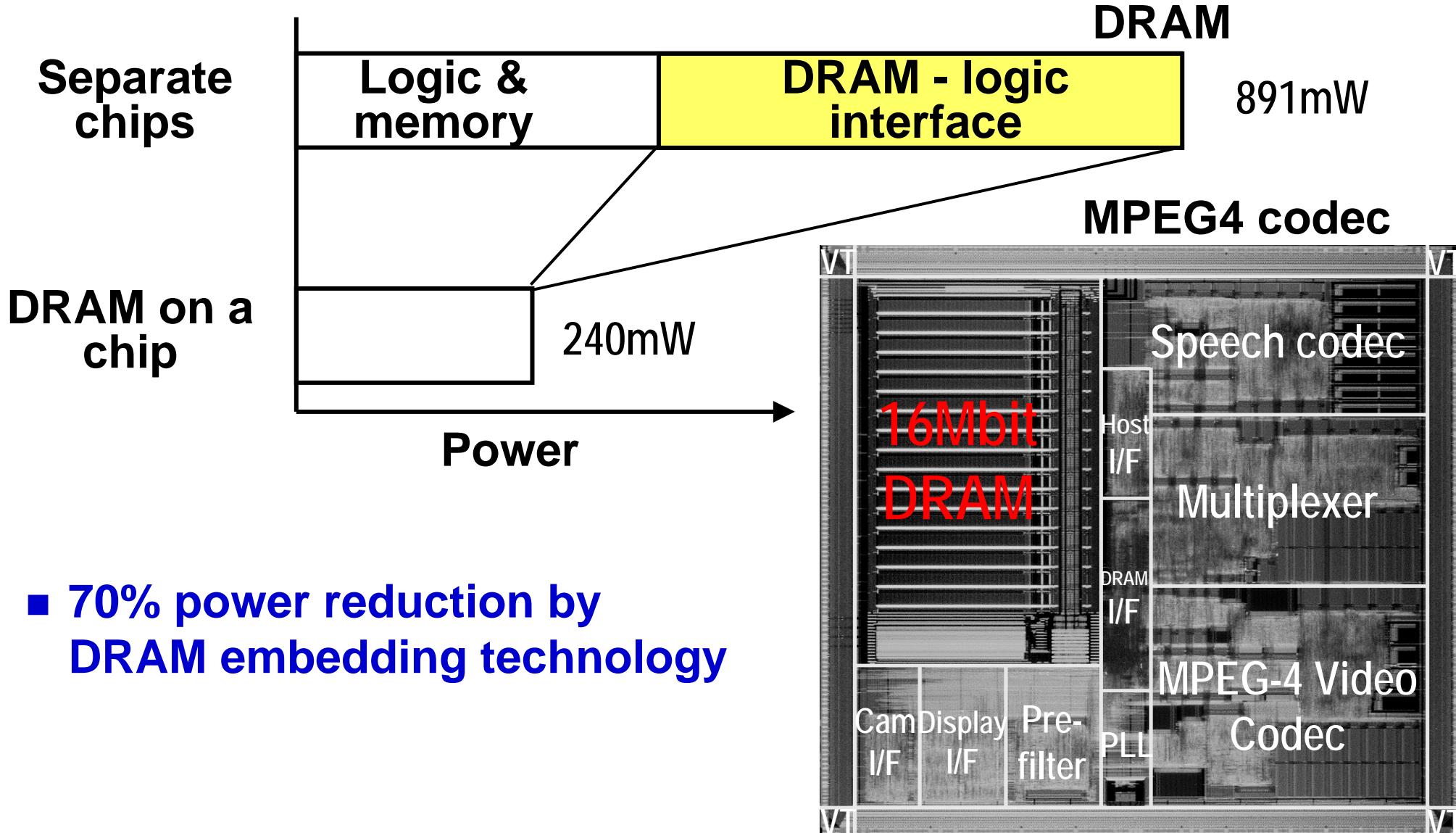
Challenges in Wireline Link

Parallel Link: Power/Area-wall



Serial Link:
Speed-wall

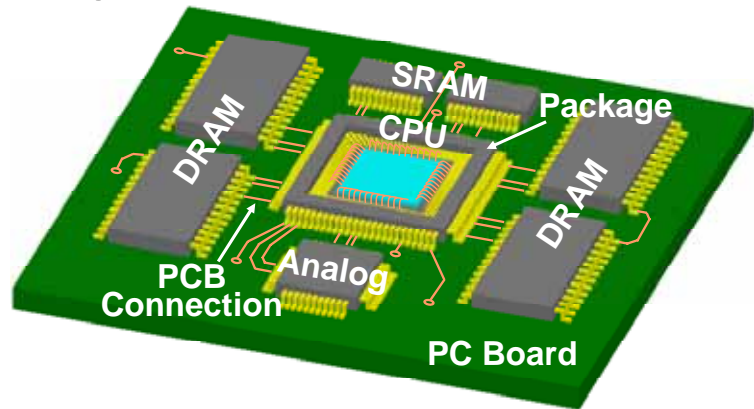
SoC Improves I/O Performance



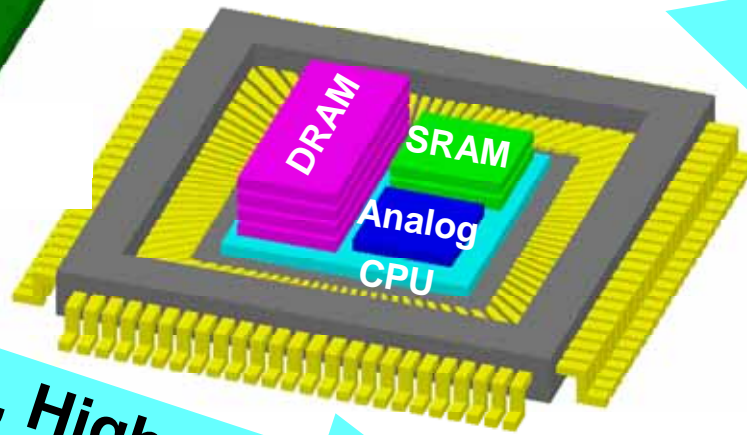
- 70% power reduction by DRAM embedding technology

From SoC to SiP

System-on-a-Board

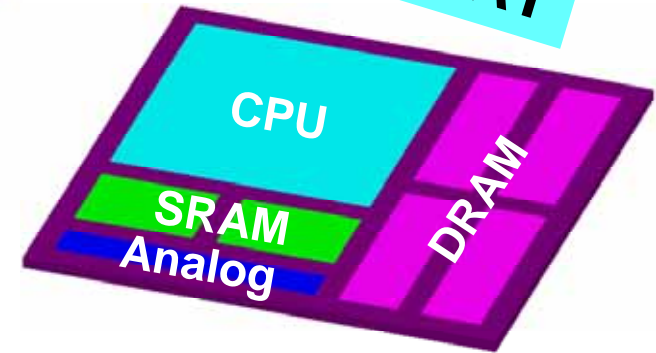


System-in-a-Package (SiP)

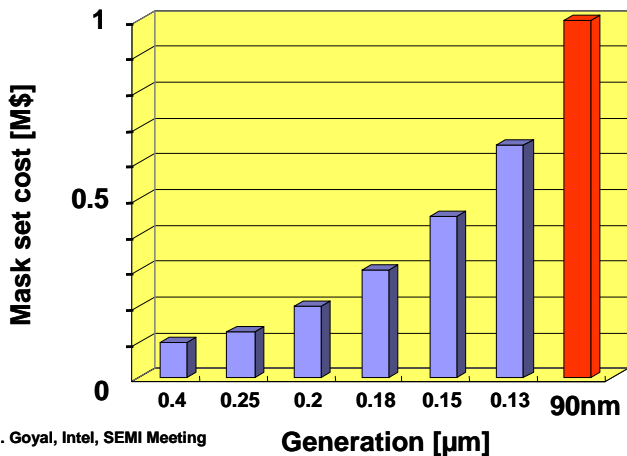


Lower Cost, QTAT

Low power, High speed



System-on-a-Chip (SoC)

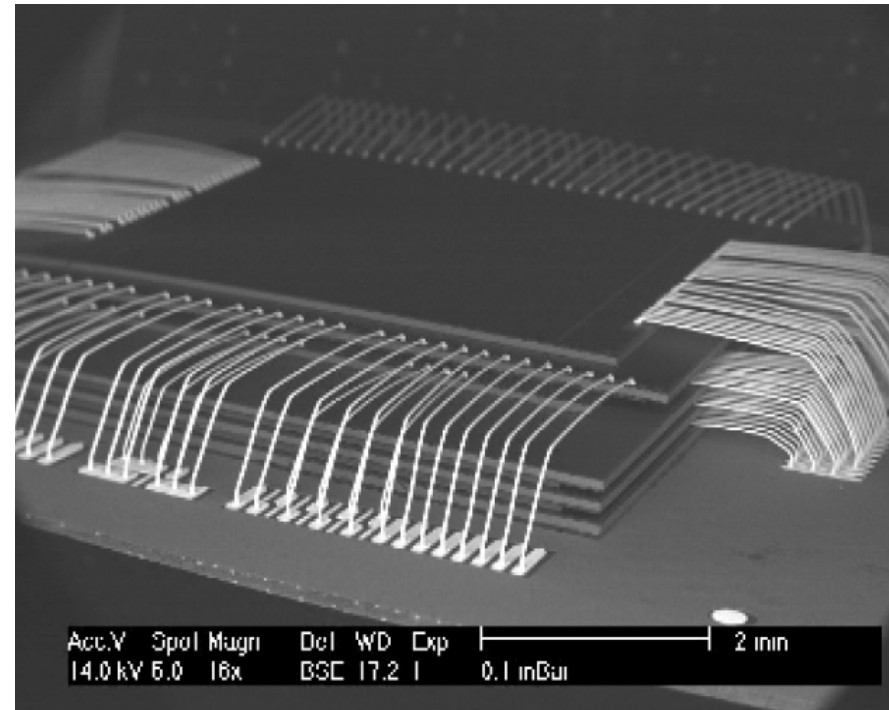


R. Goyal, Intel, SEMI Meeting

Generation [μm]

Wire Bonding

- Most common; >90% of all electronic packaging
- Minimum pitch capability $40\mu\text{m}$ with $18\mu\text{m}$ wires
- Advantage:
 - Cheap
 - Mature Process
 - Application Independent
 - Board-to chip-to-chip
- Disadvantage:
 - Chip edge connections only
 - Mechanical damage from bond
 - Mechanical integrity of bond
 - Density challenged



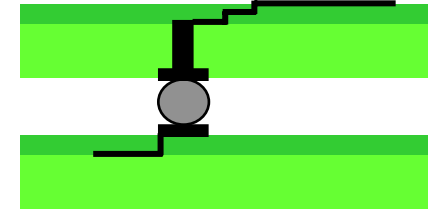
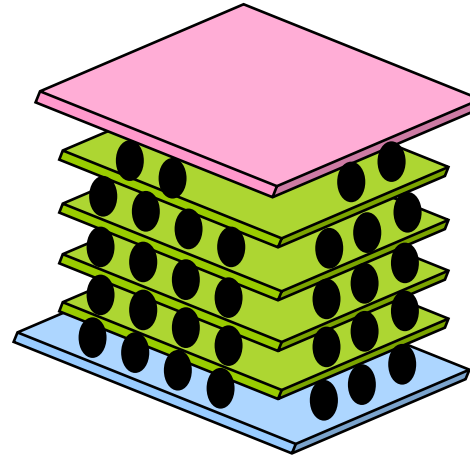
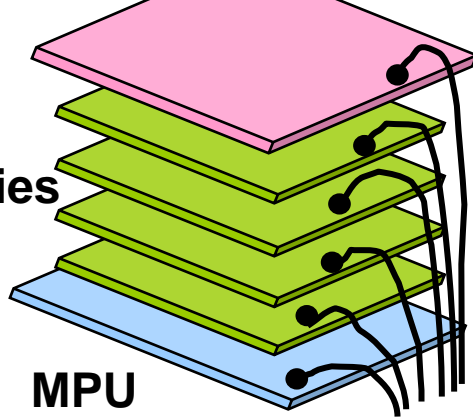
courtesy Toshiba

From Periphery to Area

Sensor / RF / Analog

Memories

MPU



■ Bonding (Conv.)

(+) low cost, practical

(-) peripheral contact:
long distance (~10mm)
small # of connections
(~100)

■ Through Si Via (Future)

(+) area contact:

short distance (~0.1mm)

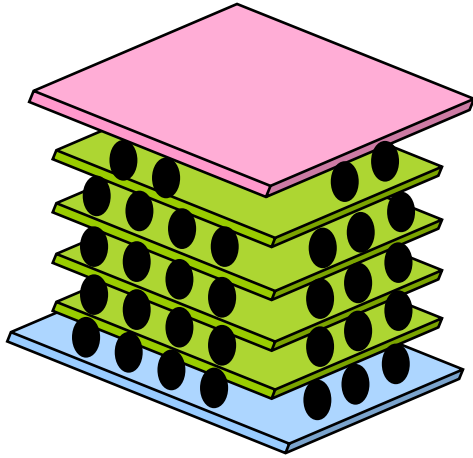
large # of connections (~10000)

(-) expensive process / reliability issue

(-) low yield due to Known Good Die
issue : difficult to test in fine pitch

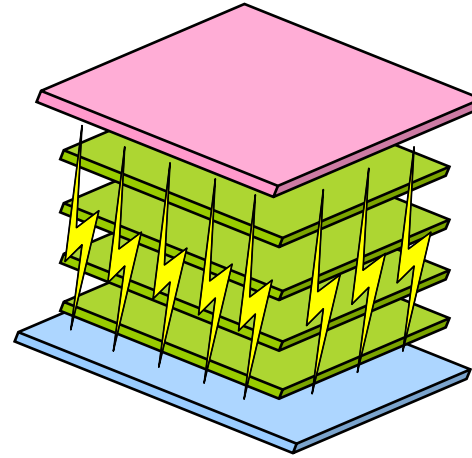
(-) scaling limit due to mechanical
contacts (~10 μ m pitch)

From Mechanical to Electrical



■ TSV

- (-) process
- (-) KGD
- (-) scaling limit

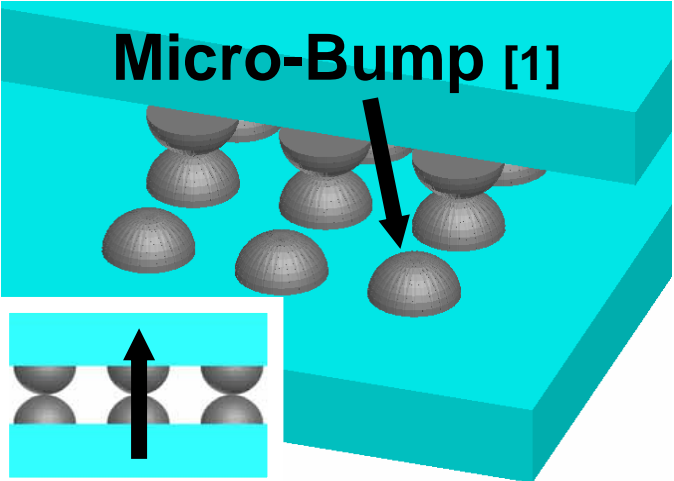
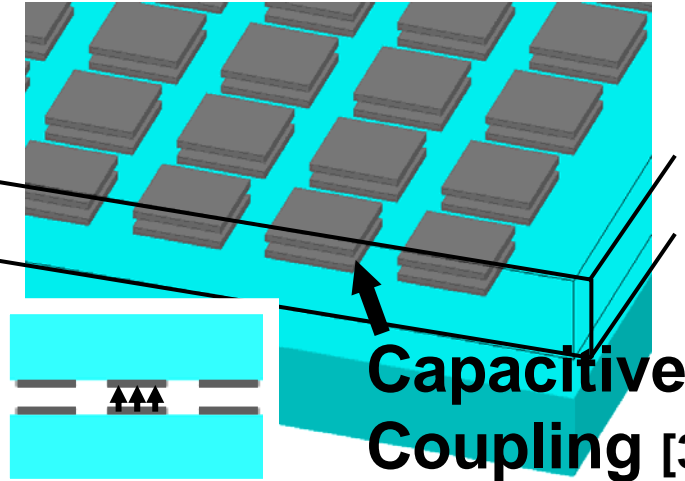
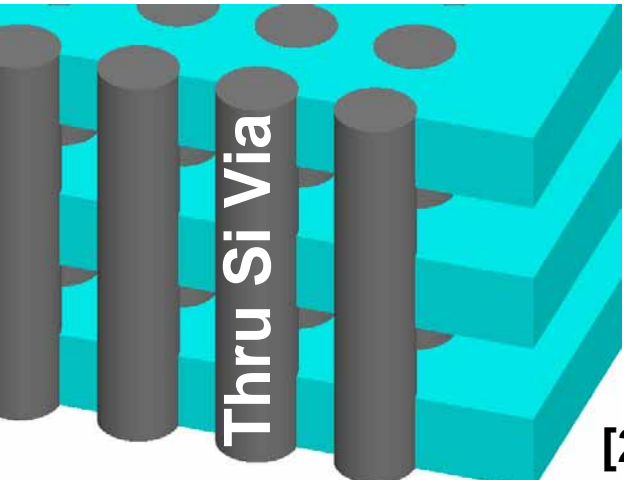
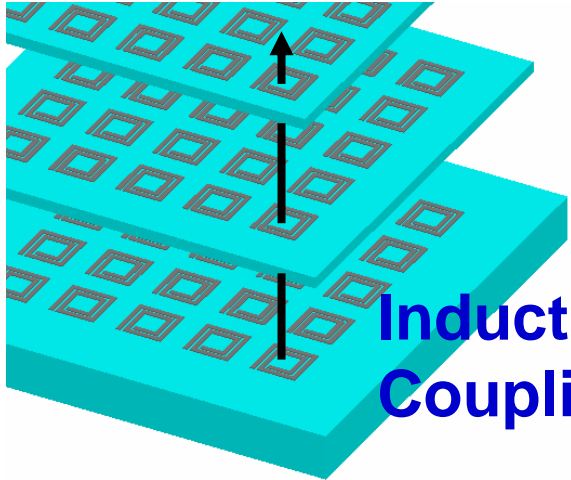


■ Wireless Interface

- (+) no addition in process, no reliability issue
- (+) KGD solvable : easy to attach and remove
- (+) high density channels (below $10\mu\text{m}$ pitch)
- (+) 3D scaling scenario (thinning a chip)
- (+) channels through active devices
- (+) low power : no ESD protection required

- Proposal
wireless transceiver arrays

3D Interface

| | Wired | Wireless |
|-----------------------------------|--|---|
| 2 Chips (Face-to-Face) |  <p>Micro-Bump [1]</p> |  <p>Capacitive Coupling [3]</p> |
| Over 3-Stacked Chips |  <p>Thru Si Via</p> <p>[2]</p> |  <p>Inductive Coupling [4]</p> |

[1] Ezaki (ISSCC'04) [2] Burns (ISSCC'01) [3] Kanda (ISSCC'03) [4] Mizoguchi (ISSCC'04)

Inductive vs. Capacitive

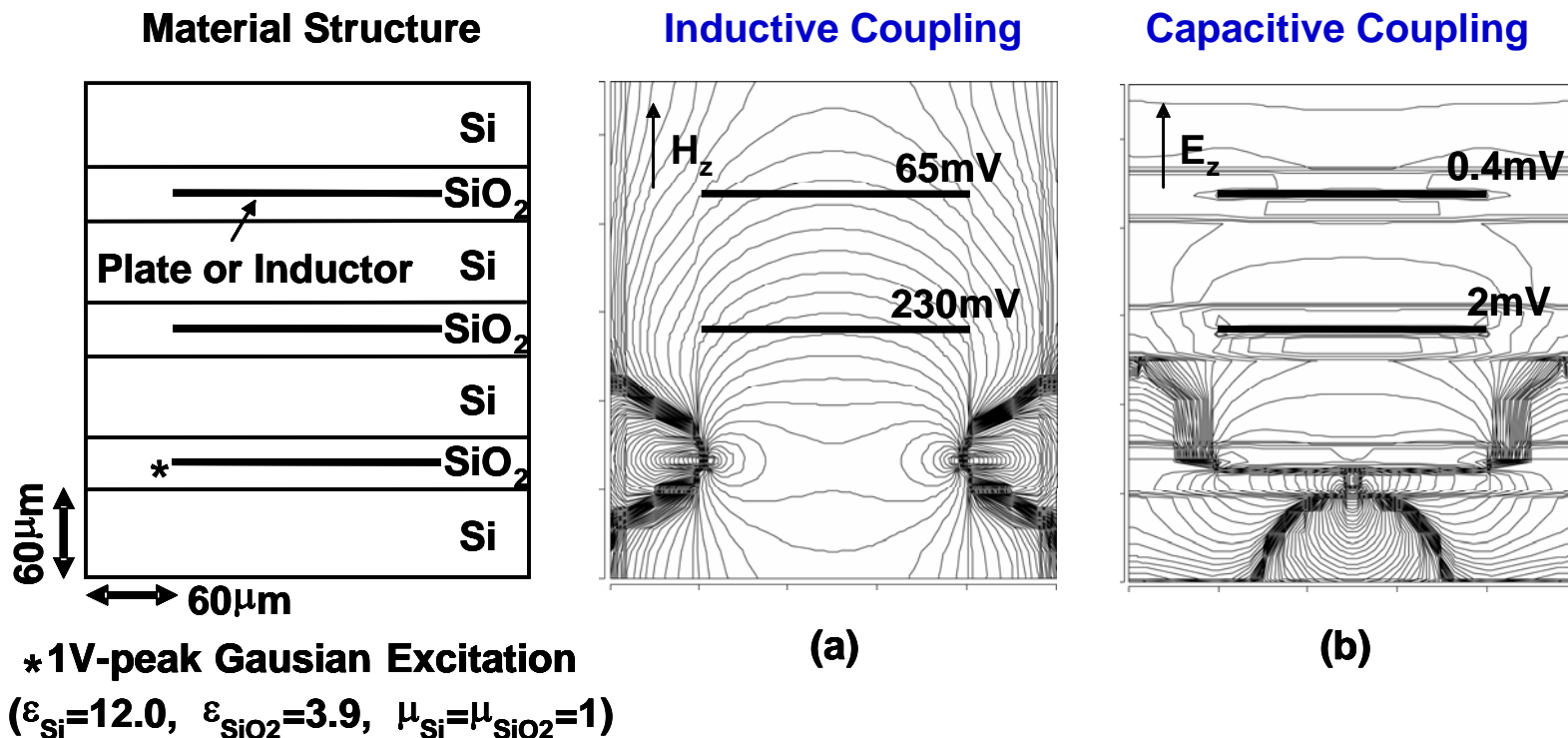
■ Advantages of Inductive Coupling

(+) reflection and absorption is much smaller

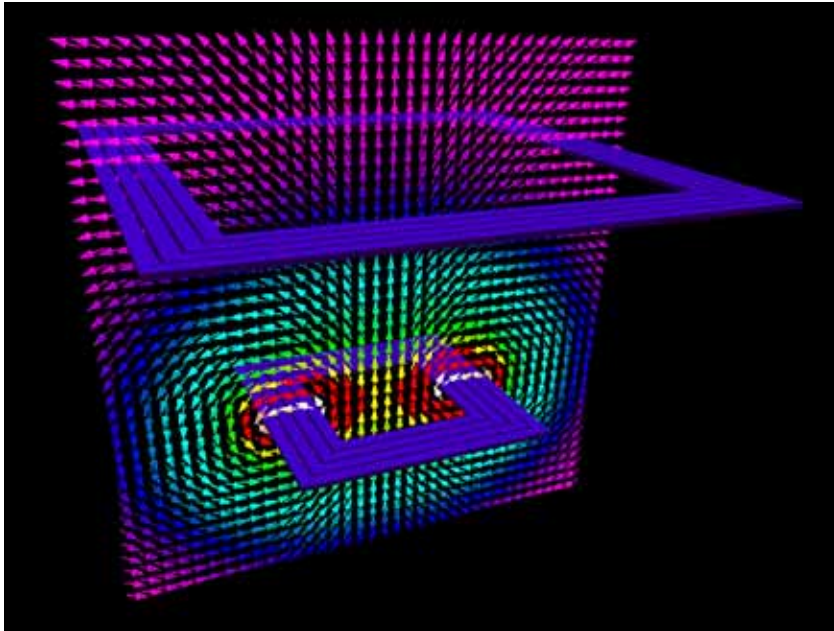
(+) more than 3 chips stacked, faced up or down, can be connected

(+) coupling coefficient is enlarged by increasing # of metal layers

(+) transmission power can be increased even at low V_{DD} 's



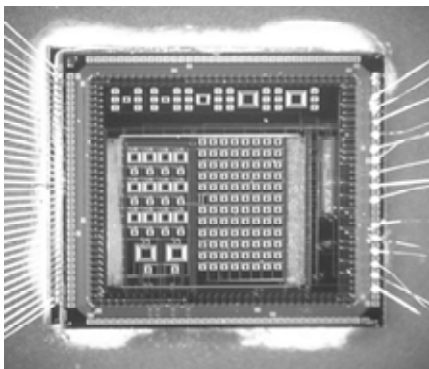
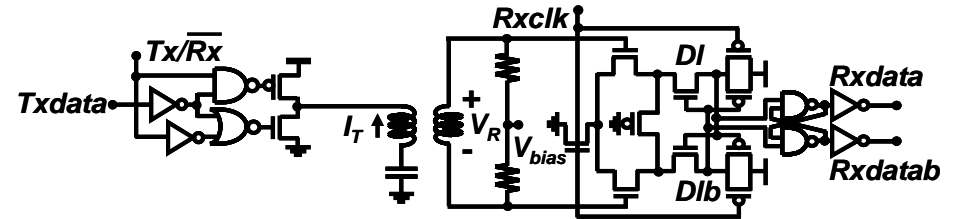
Inductive-Coupling Inter-Chip Data/Clock Link



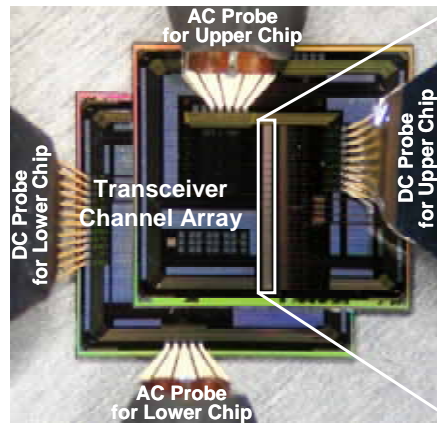
Multi-layer Wires



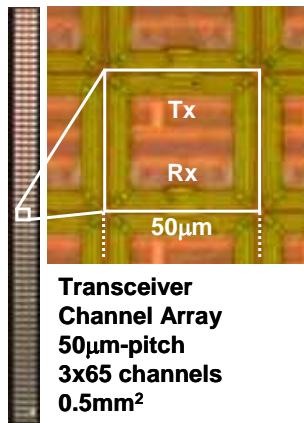
Digital CMOS Circuits



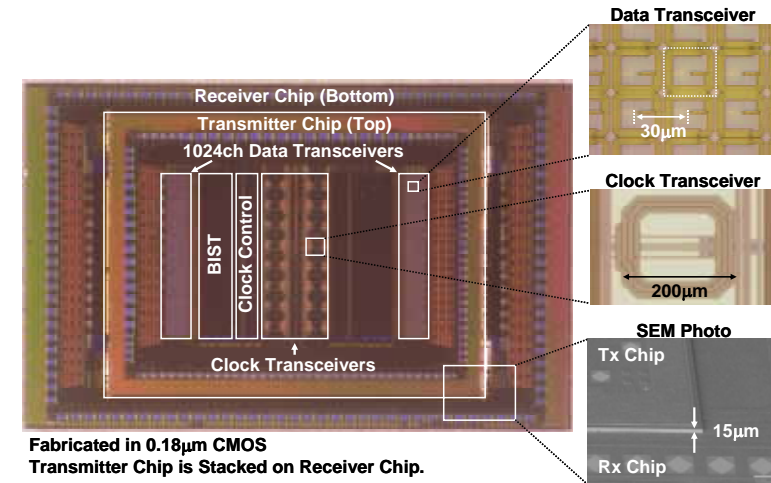
ISSCC 2004
1Gb/s



ISSCC 2005
200Gb/s



Transceiver Channel Array
50µm-pitch
3x65 channels
0.5mm²



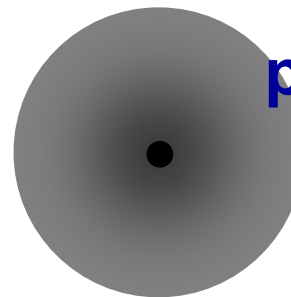
Fabricated in 0.18µm CMOS
Transmitter Chip is Stacked on Receiver Chip.

ISSCC 2006
1Tb/s

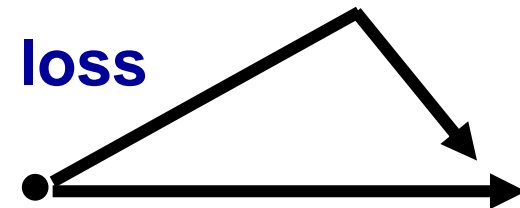
LAN Wire vs. Wireless

| | Wired LAN (Ethernet) | Wireless LAN (WiFi) |
|-------------|---|--|
| | 802.3u (100BASE-T) twisted pair <100m | 802.11b 2.4GHz <100m |
| Data rate | High speed (100Mbps) | Low speed (11Mbps) |
| Reliability | High (BER10^{-14}) | Low (BER~ <math>10^{-4}< math>)<="" td=""> </math>10^{-4}<> |
| Cost | Inexpensive (~\$15) | Expensive (~\$100) |
| Power | Low (~100mA) | High (~400mA) |
| Size | Small | Large (w/ antenna) |
| Connection | Easy (plug and play) | Complex (authentication) |
| Usability | Messy/Difficult (ie.wall) | Neat, Simple, Easy |
| Mobility | Low/Immobile | Movable |

Multiple access in free space:
cell, TDMA, FDMA, CDMA



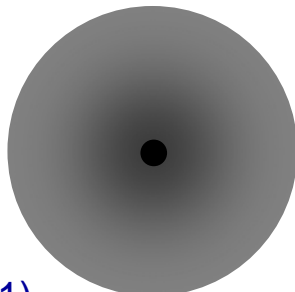
path loss



multi-path fading

Inter-Chip 3D Link Wire vs. Wireless

| | Wired Inter-Chip Link Micro-bump (2 chips) TSV (>3 chips) <math><100\mu\text{m}</math> | Wireless Inter-Chip Link Capacitive coupling (2 chips) Inductive coupling (>3 chips) <math><100\mu\text{m}</math> |
|--------------------|--|---|
| Data rate | High speed | Low speed ? |
| Reliability | High-reliable | Low-reliable ? |
| Cost | Inexpensive | Expensive ? |
| Power | Low | High ? |
| Size | Small | Large (w/ Antenna) ? |
| Connection | Easy (plug on play) | Complex (authentication) ? |
| Usability | Messy/Difficult (ie.wall) | Neat, Simple, Easy ? |
| Mobility | Low/Immobile | Movable ? |

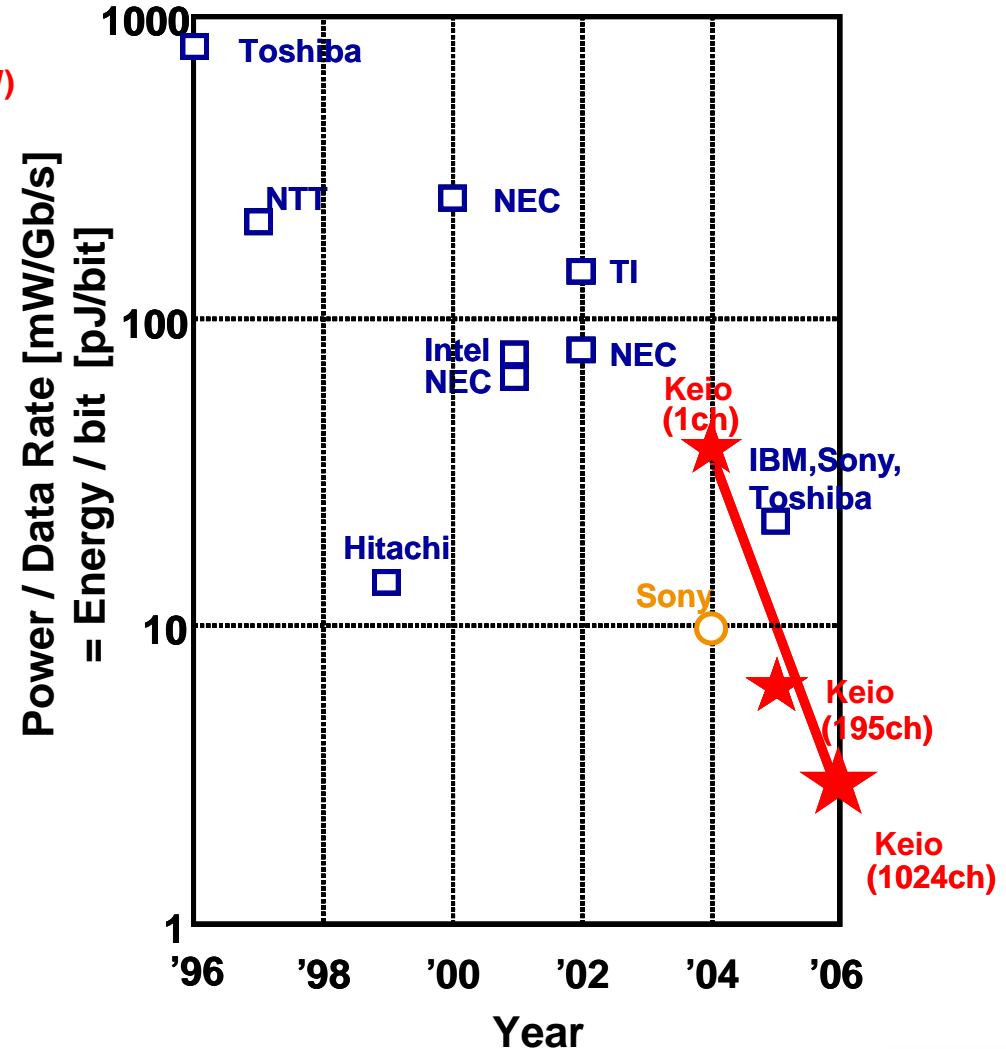
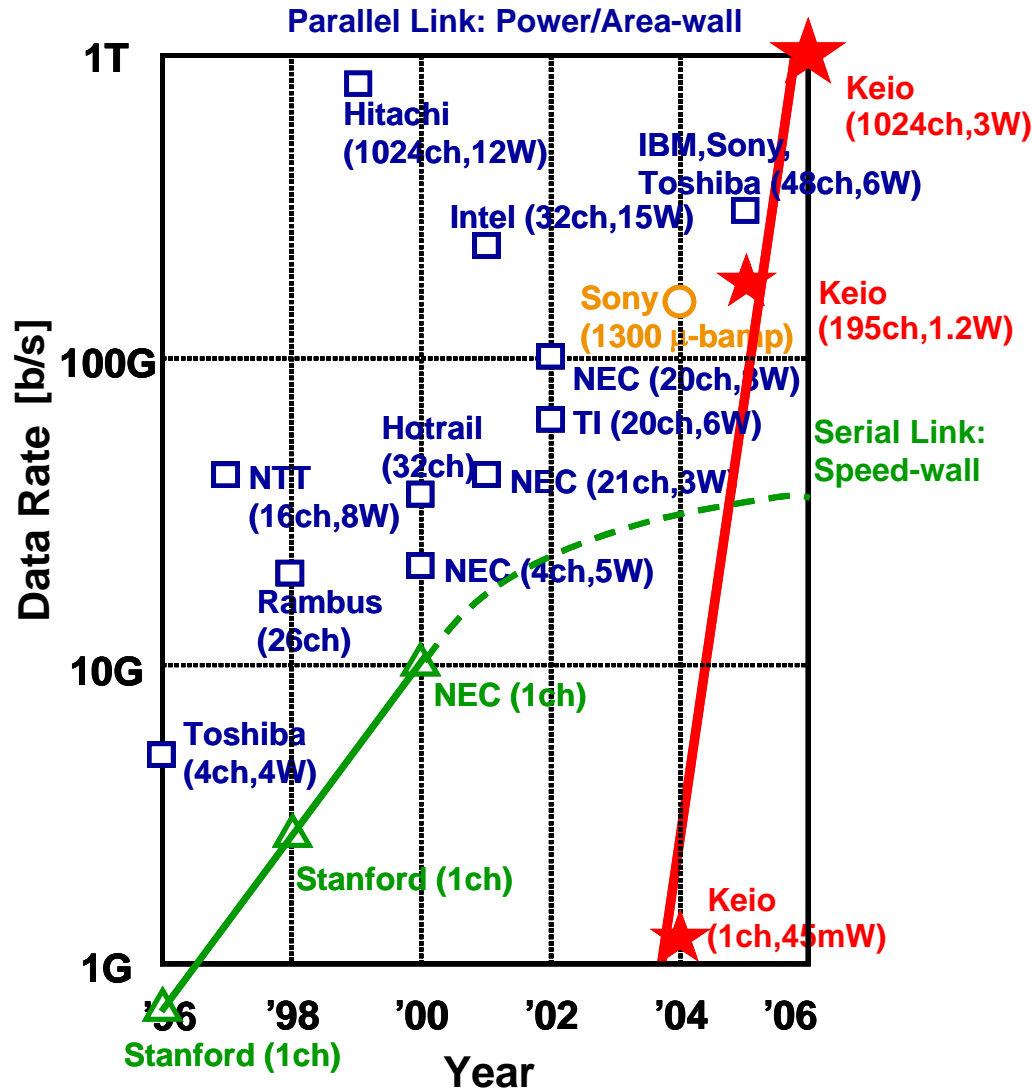


100m : 1000 wave length

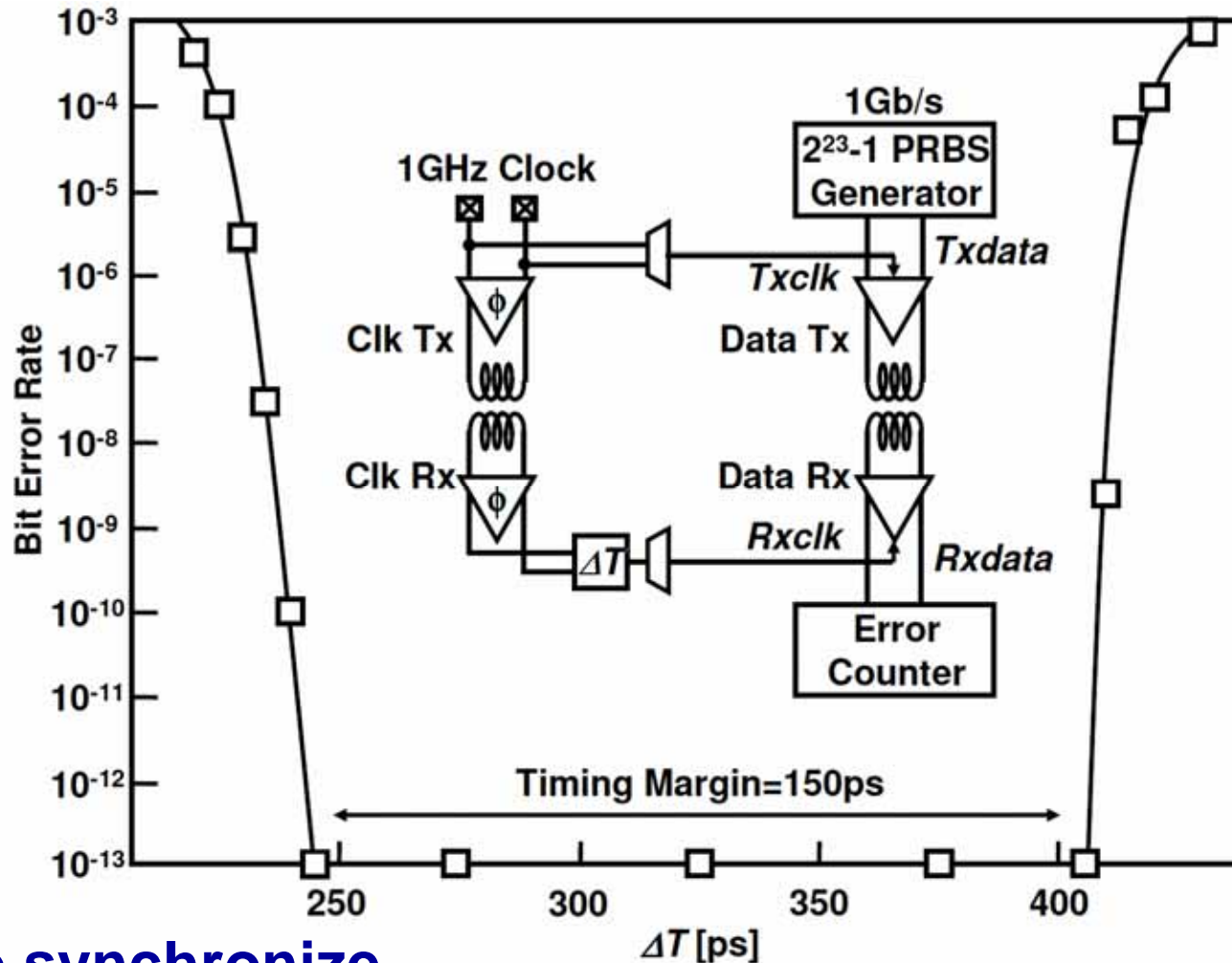


100μm: 0.001 wave length (proximity)

World Fastest (1Tb/s) and Lowest Energy (3pJ/b)



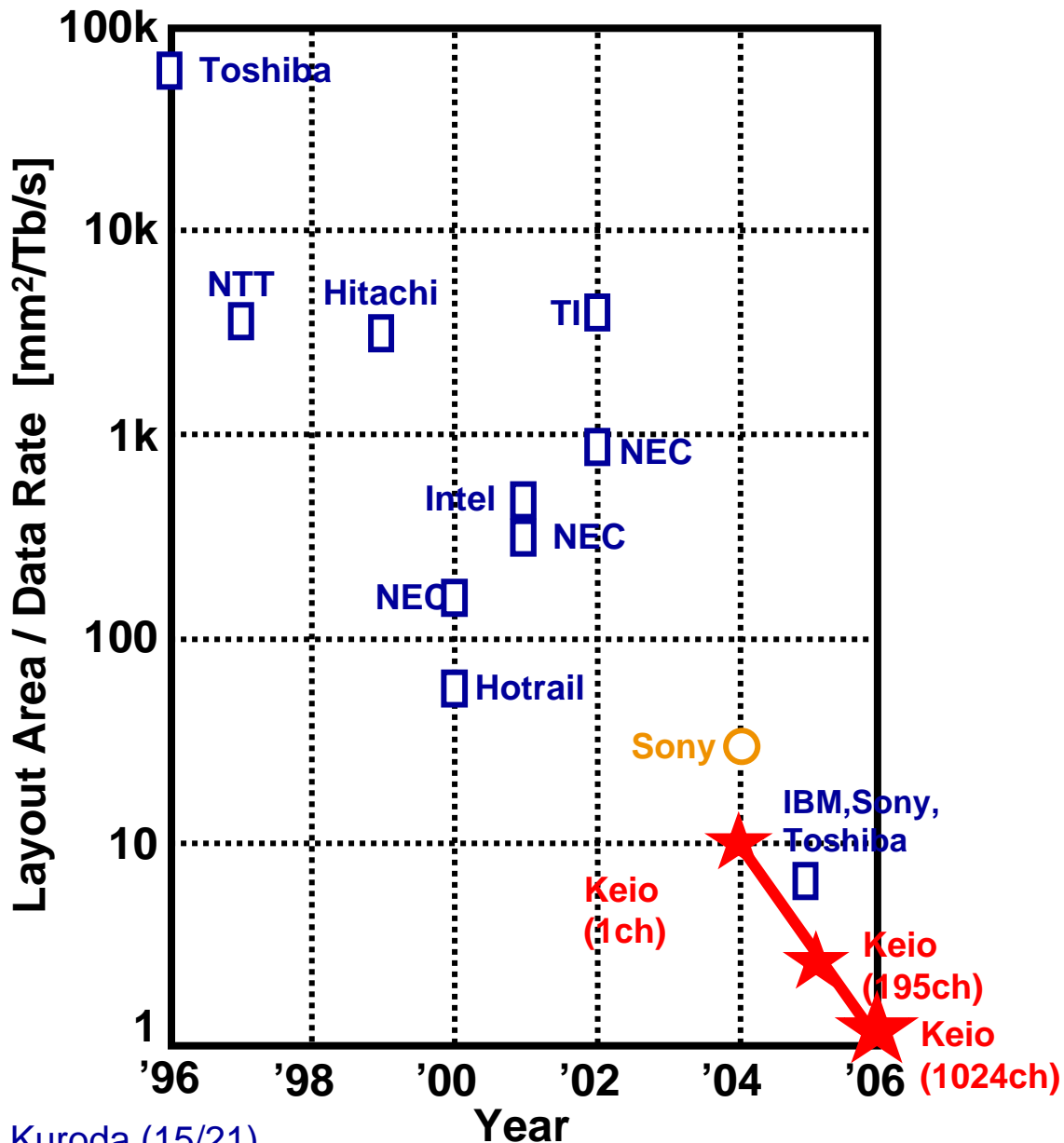
As Reliable As Wireline (BER 10^{-13})



(+) Easy to synchronize

(+) Easy to reduce pulse width to half for higher speed (2Gb/s/ch),
lower energy (1pJ/b) and narrower pitch ($30\mu\text{m}$)

World Smallest ($1\text{mm}^2/\text{Tb/s}$)



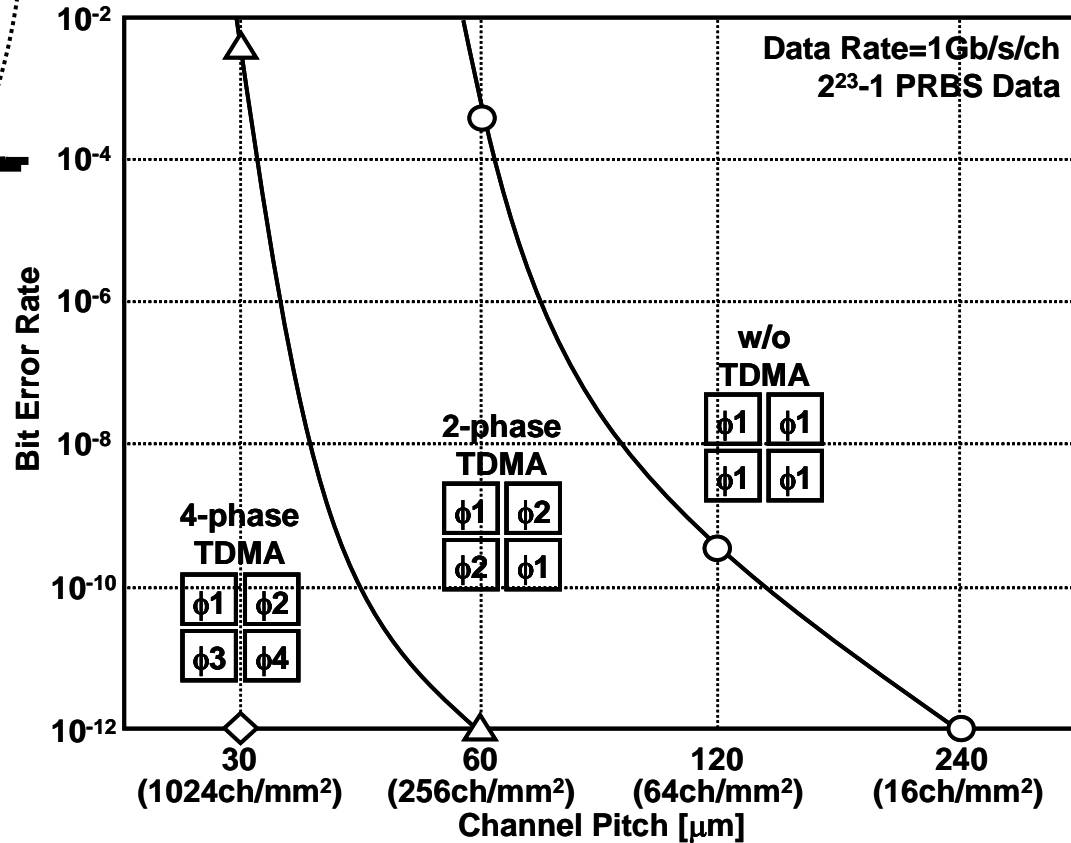
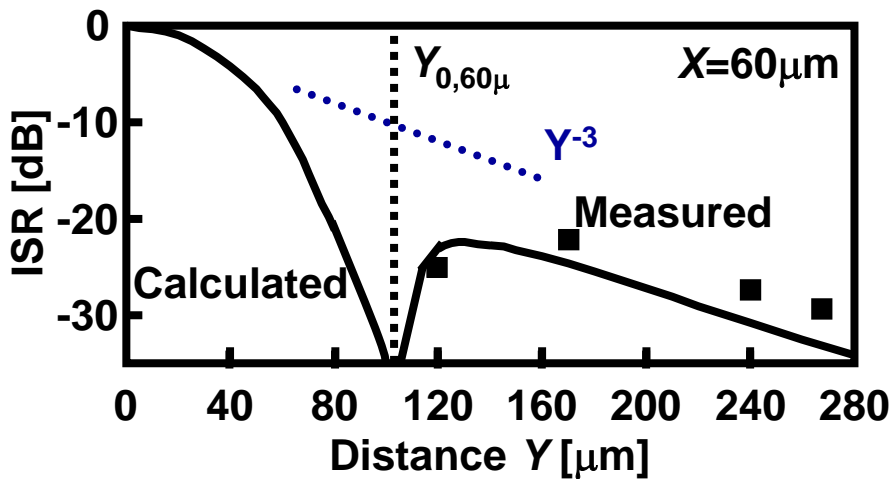
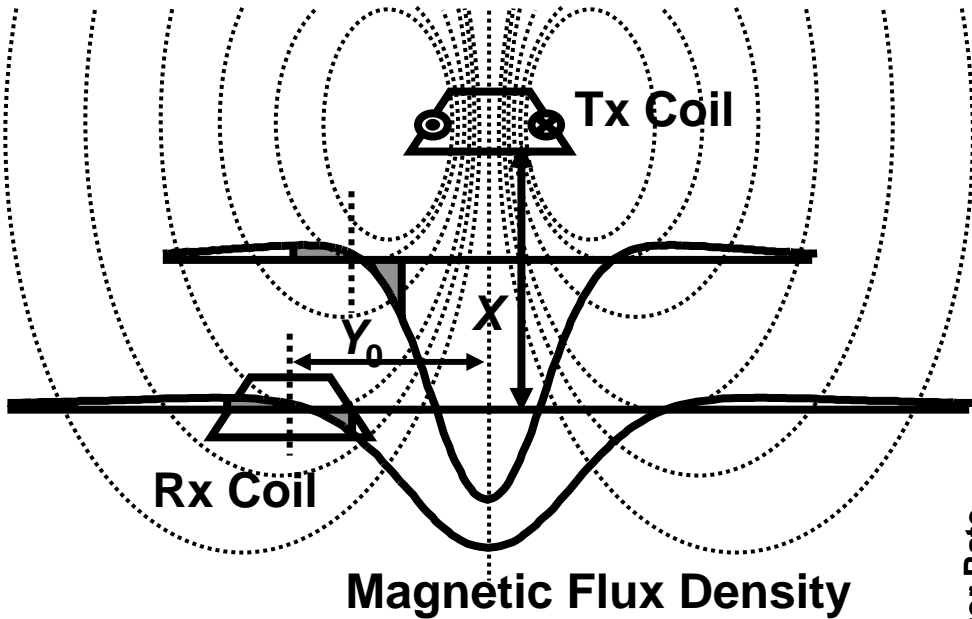
L-coupling
 30 μm pitch, $1\text{mm}^2/\text{Tb/s}$
 (20 μm pitch)
 including transceiver circuits

Micro-bump
 Sony: 60 μm pitch, $40\text{mm}^2/\text{Tb/s}$
 SFT: 50 μm pitch, $400\text{mm}^2/\text{Tb/s}$

TSV
 Elpida: 50 μm pitch
 need additional area for
 transceiver circuits

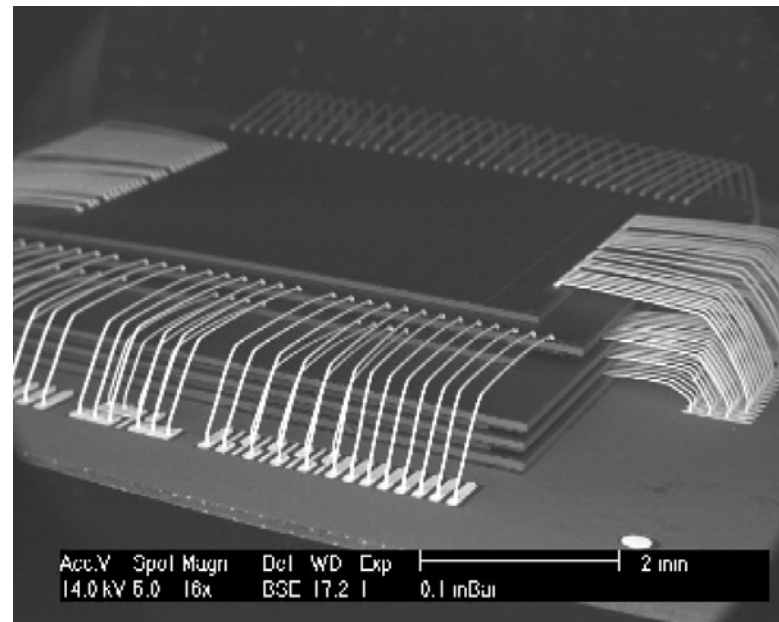
Thinner packaging possible
 than by micro-bum and TSV at
 interface

Narrower Pitch by Time Interleaving



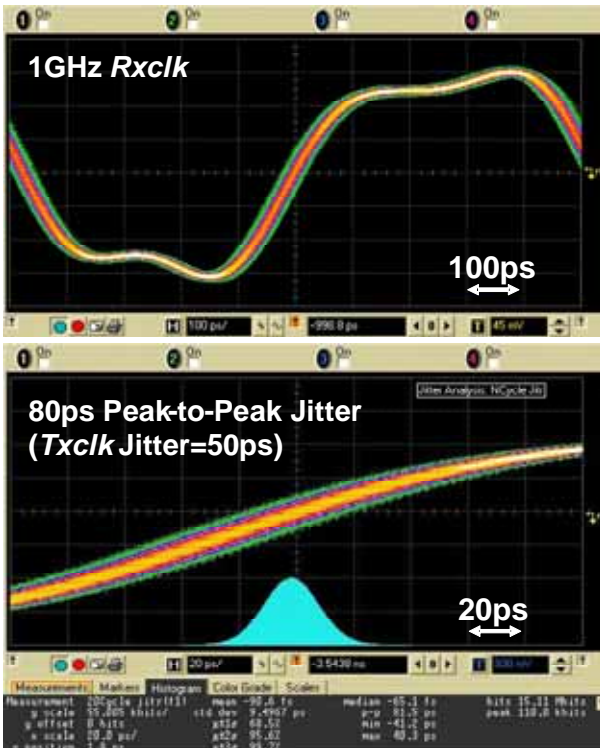
Cost Down

- **Circuit solution: no need for new process development, no additional cost in manufacturing**
- **Reduce chip size: no peripheral circuits needed, no ESD protection needed**
- **Anyplace in a chip: wireless link through transistors**
- **Less bonding wires: cost reduction in bonding and package.**

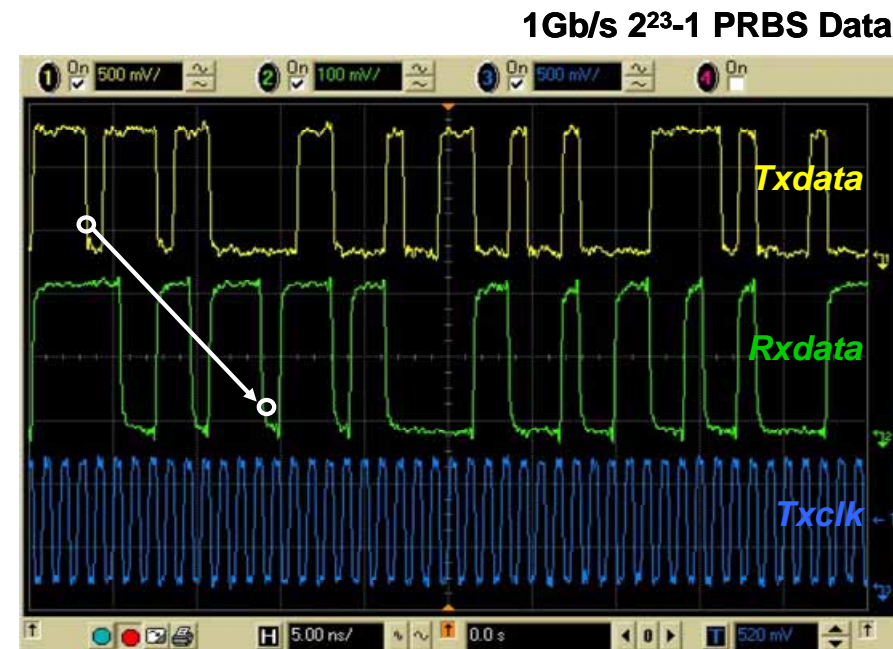
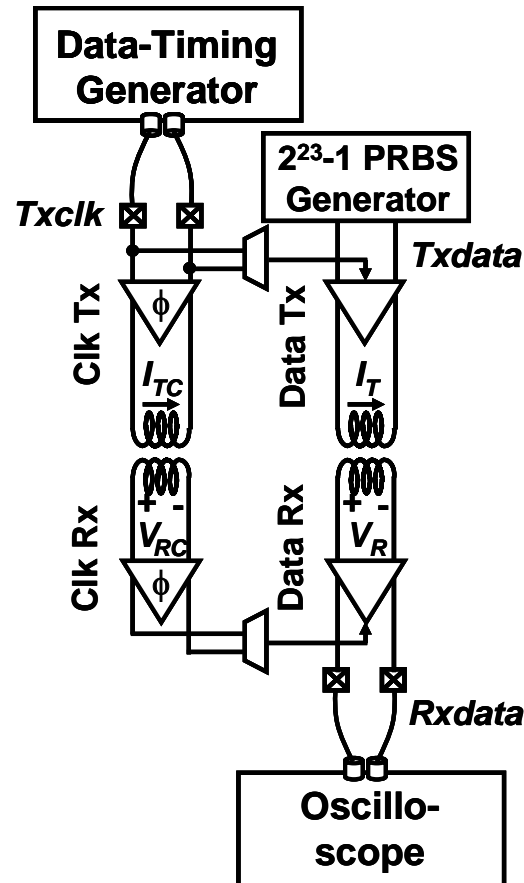


Clock and Data Link

Clock Link



Data Link



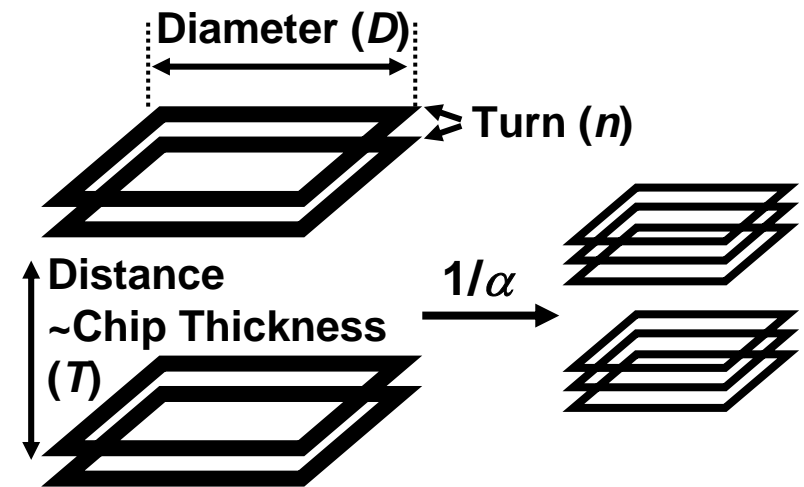
- Both clock and data are linked (one clock data latency)
- Only power needs to be provided by bonding wires
- No need for level shifter under different V_{DD} 's

Inter-Chip 3D Link Wire vs. Wireless

| | Wired Inter-Chip Link Micro-bump (2 chips) TSV (>3 chips) <100 μ m | Wireless Inter-Chip Link Capacitive coupling (2 chips) Inductive coupling (>3 chips) <100 μ m |
|--------------------|--|--|
| Data rate | High speed | High speed |
| Reliability | High-reliable | High-reliable |
| Cost | Up | Down |
| Power | Low | Low |
| Size | Small | Small |
| Connection | Easy (plug on play) | Easier (no level shifter needed) |
| Usability | Need new technology | Conventional |
| Mobility | One time attachment | Detachable |
| Scalability | Mechanical | Electrical ... Scalable |

Constant Magnetic Field Scaling

| | | |
|--------------------------------------|------------------------------------|----------------|
| Transistor Size | [x] | $1/\alpha$ |
| Power Supply Voltage | [V] | $1/\alpha$ |
| Chip Thickness | [T] | $1/\alpha$ |
| Coil Turn Number (Layer #) | [n] | $\alpha^{0.8}$ |
| Current | [I] | $1/\alpha$ |
| Circuit Delay Time | [t]~[CV/I] | $1/\alpha$ |
| Coil Diameter | [D]~[1/x] | $1/\alpha$ |
| Self Inductance | [L]~[$n^2 D^{1.6}$] | 1 |
| Magnetic Coupling Coefficient | [k] | 1 |
| Receive Signal | [v_R]~[$kn^2 D^{1.6} (I/t)$] | 1 |
| Crosstalk | [v_{RS}/v_{RN}] | 1 |
| Data Rate / Channel | [1/t] | α |
| Channel Number / Area | [1/D ²] | α^2 |
| Aggregated Data Rate / Area | [1/tD ²] | α^3 |
| Energy / Bit | [ItV] | $1/\alpha^3$ |



Self Inductance

$$L \propto n^2 D^{1.6}$$

Received Signal Voltage

$$V_R \propto M \left. \frac{\partial I_T}{\partial t} \right|_{\max} = k \sqrt{L_T L_R} \left. \frac{\partial I_T}{\partial t} \right|_{\max}$$

$$= kL \frac{I_D}{t_{pd}} = kn^2 D^{1.6} \frac{I_D}{t_{pd}}$$

Summary

- Challenges in wireline inter-chip links: speed-wall in serial link and power/area-wall in parallel link.
- Inductive-coupling inter-chip link has achieved the best performance in the world: fastest data rate (1Tb/s), lowest energy (3pJ/bit), and smallest area (1mm²/Tb/s).
- Since it is a circuit solution in a conventional technology, it is less expensive than micro-bump and TSV.
- Performance will be further improved by the constant magnetic field scaling.

