

# ULTRA-LOW POWER RF TRANSCEIVERS

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**Mixed-Signal  
Microelectronics  
Group**



# Outline

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- ❑ INTRODUCTION
- ❑ SYSTEM LEVEL ASPECTS
- ❑ FHSS FREQUENCY SYNTHESIZERS
- ❑ FHSS PRE-DISTORTION BASED TRANSMITTER DESIGN
- ❑ RECEIVER PLANNING
- ❑ CONCLUSIONS

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□ FHSS PRE-DISTORTION BASED TRANSMITTER DESIGN

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□ CONCLUSIONS

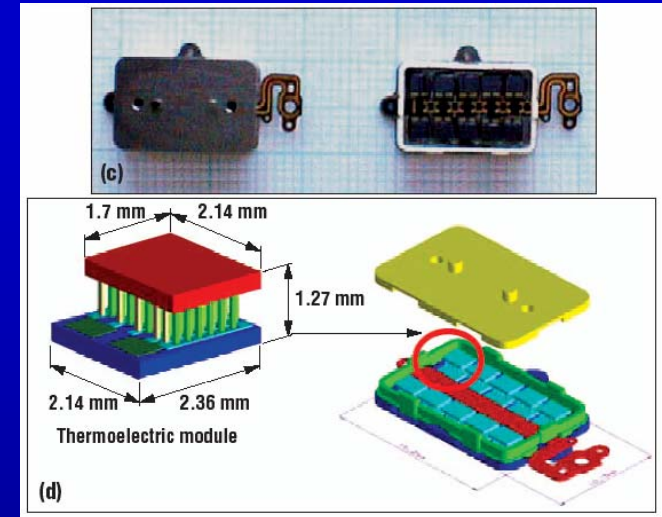
# Introducing Ultra-low Power Transceivers

- ❑ Definition of ultra-low power transceivers
  - Operation time  $\geq 10$  years harvesting energy from the ambient (solar, vibrational...)
  - Operating range: 2 to 10 meters
  - Current consumption below 2 mA
  
- ❑ Meeting the ultra-low power target
  - Data rates in the range of few kbits/sec
  - Reduced external components
  - High level of integration
  - Deep-sleep mode with on demand “turn-off” and “wake-up”
  - Current consumption during deep-sleep mode well below 100 nA

# Energy scavenging possibilities

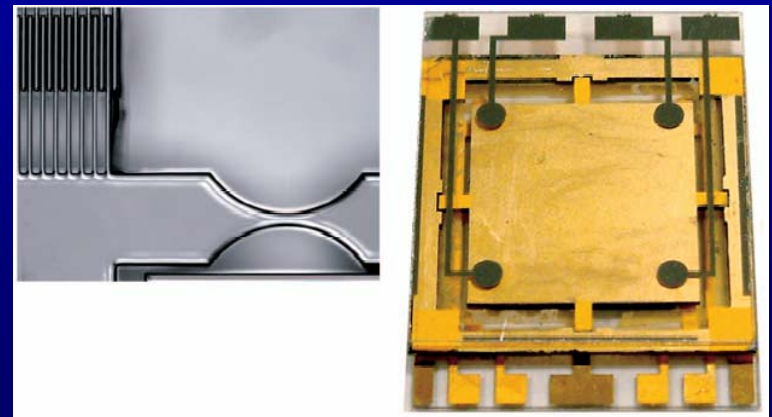
## ❑ Thermoelectric conversion

- Carnot Efficiency: 10  $\mu$ A at 3 V with 5 degrees Celsius of temperature difference (Applied Digital Solutions Thermo Life)



## ❑ Vibrational excitation

- 8 and 6  $\mu$ W @ 2.5 kHz resonance frequency
- Expected power from vibrational microgenerators up to 4  $\mu$ W/cm<sup>3</sup> (human motion) and up to 800  $\mu$ W/cm<sup>3</sup> from machine-induced stimuli



## ❑ Solar energy : 0.01 mW (indoor, 170 Lux)

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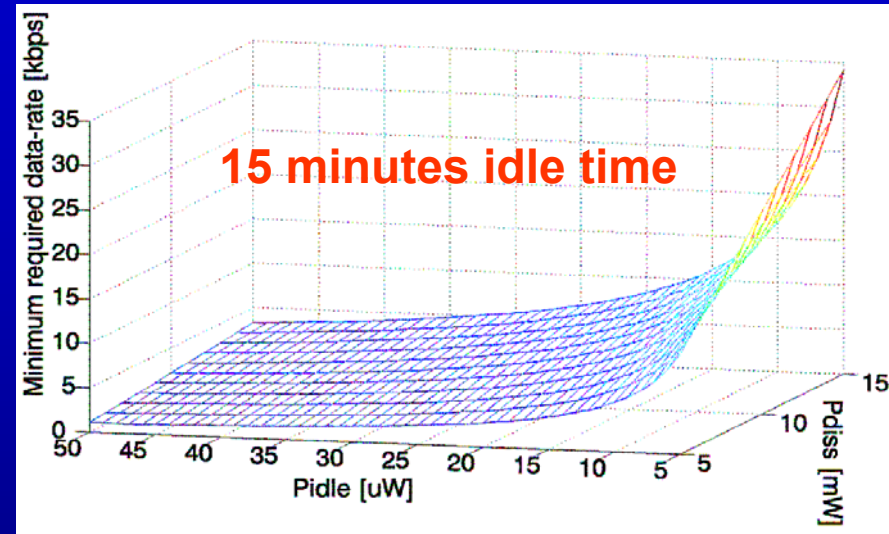
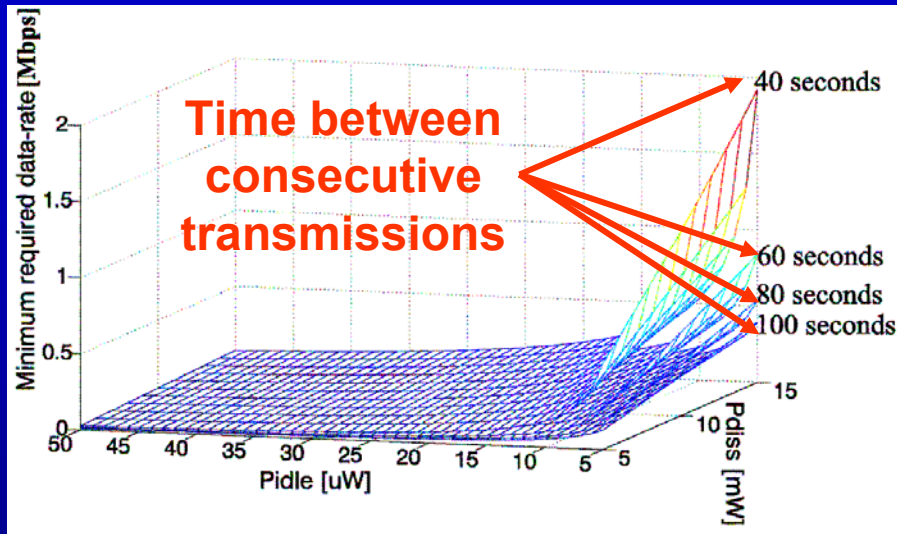
□ RECEIVER PLANNING

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## System level aspects

Minimum required data-rate for an average power consumption smaller than  $P_{idle} + 10\%$

Packet length = 1000 bits, 100  $\mu$ s wake-up time, NF=20 dB, SNR=15 dB



❑ Increasing the data-rate can effectively reduce the average power consumption


➤ The advantage decreases by reducing the duty-cycle

❑ At very-low duty-cycle (one transmission every 15 minutes) a data-rate lower than 35 kbps is allowed

❑ Increasing data-rate, increases hardware complexity and leakage currents → average power consumption will increase

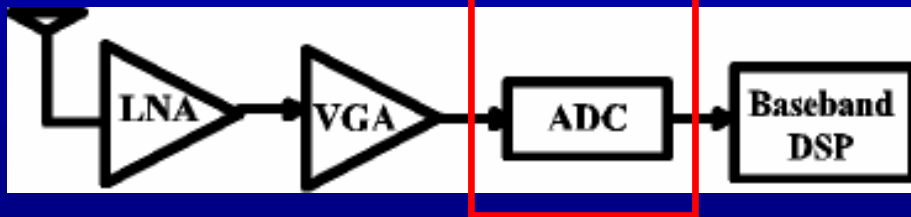
# Ultra-wideband transceivers

- Occupied bandwidth larger than 500 MHz (FCC rules)

$$C = BW \times \log_2 \left( 1 + \frac{P_S}{P_N} \right)$$


For small C (low data-rate applications), the SNR can be very small → low transmitted power!

## UWB Receiver block diagram



- ❖ ADC will require a very high sampling rate
- ❖ High-speed (Low-resolution) flash converter mandatory

- 2.2 pJ/conversion<sup>1</sup>
- ENOB = 4 and  $f_{\text{sample}} = 1\text{GHz}$

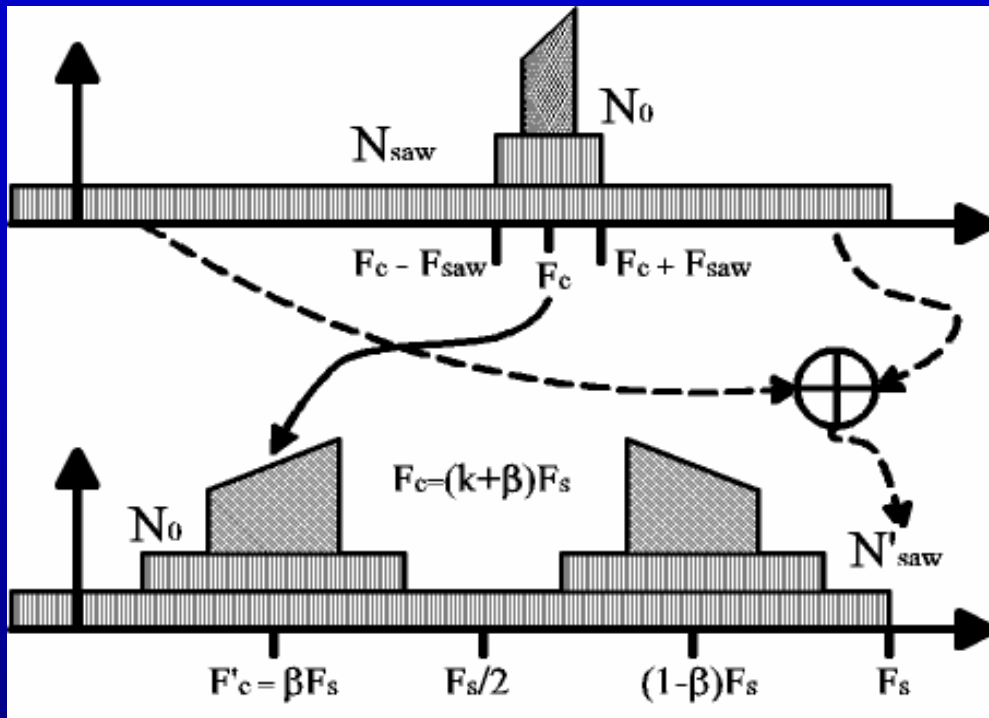
$$FOM = \frac{P}{2^{ENOB} \times f_{\text{sample}}}$$



**35 mW**

(1) C. Sandner et al., **A 6bit, 1.2GSps Low-Power Flash-ADC in 0.13μm Digital CMOS**, Proceedings of the conference on Design, Automation and Test in Europe, 2005, Vol.3, pag. 223-226,

# Sub-sampling architectures



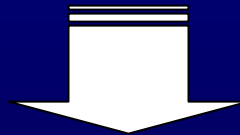
- Noise aliased back → degrade SNR
- SNR degradation equal to:

$$D = 10 \times \log_{10} \left( 1 + \frac{2MN_{saw}}{N_0} \right)$$

$M$  = ratio between the carrier frequency and the sampling frequency

❑ BPF requirements will increase

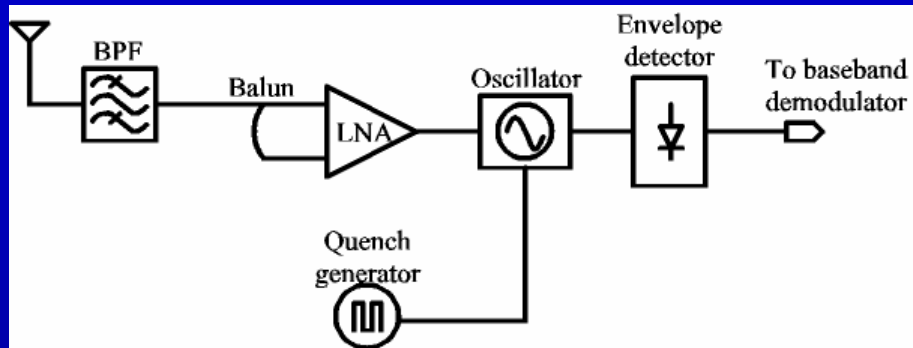
❑ Phase noise is amplified<sup>1</sup> by  $M^2$  → interferers can degrade the SNR via reciprocal mixing



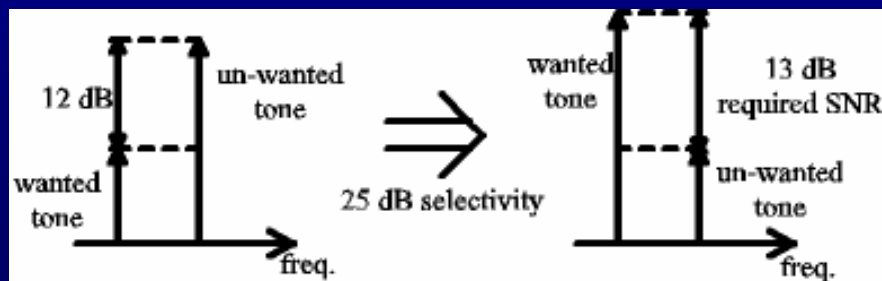
**SUITABLE FOR AN INTERFERER-FREE SCENARIO**

# Super-regenerative architectures

## Super-regenerative receiver

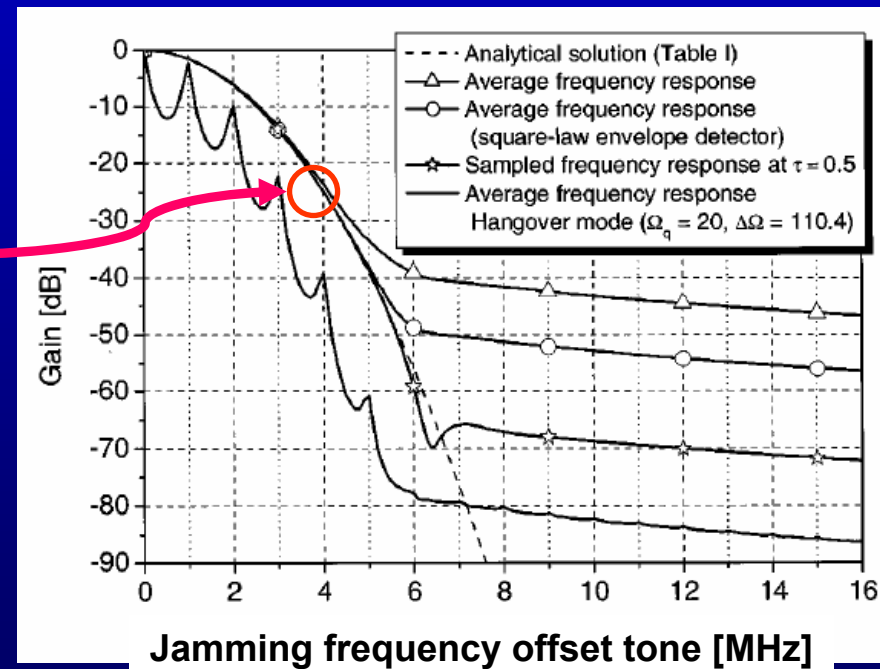


- 13 dB SNR for a 0.1% BER
- 25 dB selectivity achievable for unwanted jamming tone at  $\pm 4$  MHz away
- Jamming tone max 12 dB higher than the desired tone



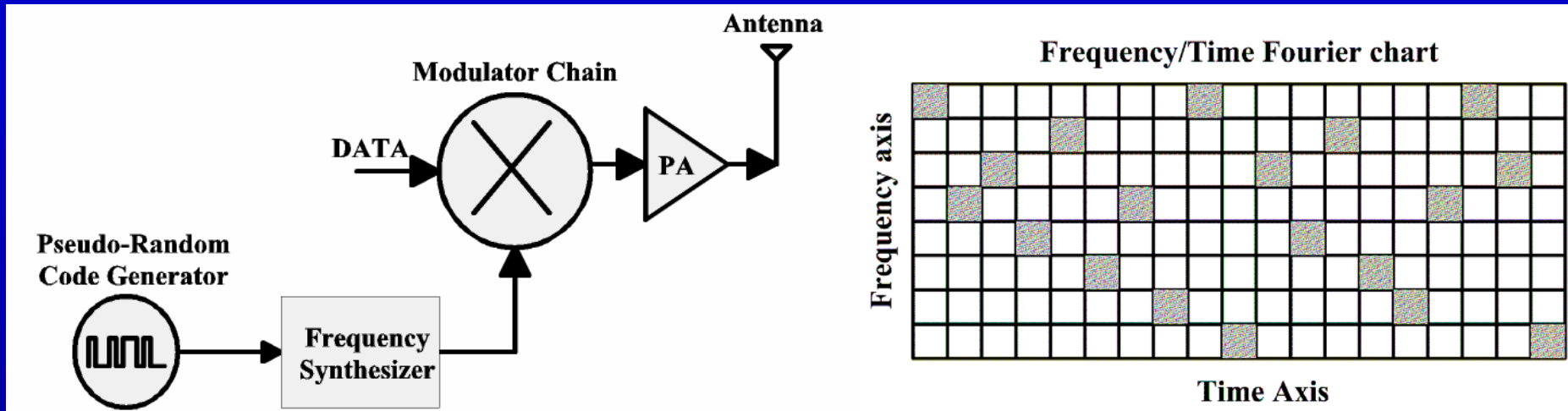
Real applications require more than -40 dB C/I at  $\pm 3$  MHz

- Poor selectivity
- Lack of stability
- OOK modulation required



A. Vouilloz et al., "A low-power CMOS super-regenerative receiver at 1 GHz", JSSC 2001

# FHSS systems strongholds (I)



## Spread-Spectrum systems

### Synchronization time

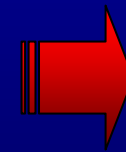
$$\overline{T_S} = (C - 1) T_{da} \left( \frac{2 - P_d}{2P_d} \right) + \frac{T_i}{P_d}$$

- $T_i$  = Integration time
- $P_d$  = Probability of detection (correct cell)
- $T_{da}$  = Dwell time
- $C$  = total number of cells

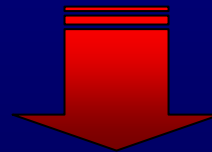
### Synchronization accuracy

$$\pm T_c / 2 \quad \text{DSSS}$$

$$\pm T_{\text{symp}} / 2 \quad \text{FHSS}$$



$$C \approx 1/\text{Accuracy}$$



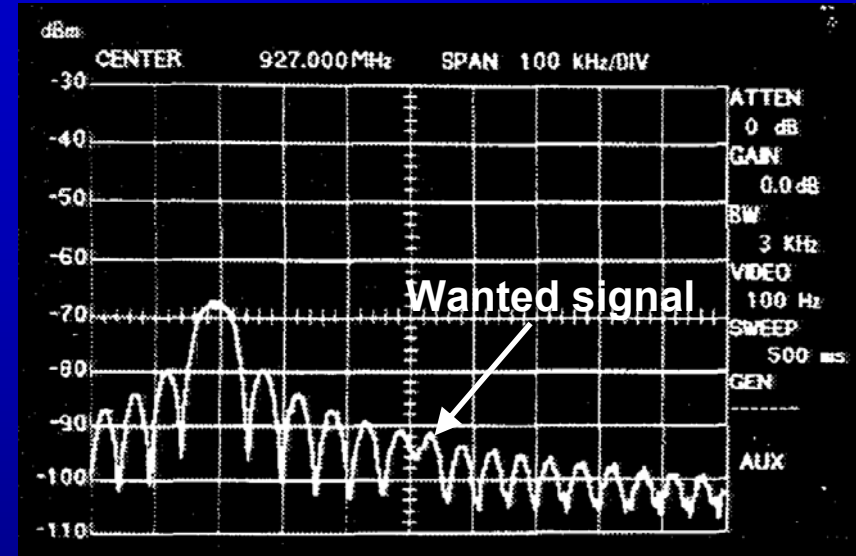
$$T_c \approx G \times T_{\text{symp}}$$

# FHSS systems strongholds (II)

BFSK signal<sup>1</sup>



BPSK signal<sup>1</sup>



- ❖ Unwanted signal at 5 meters distance, wanted signal 60 meters far away
- ❖ BFSK modulation techniques more robust than BPSK against the near-far problem

**DSSS generally employs BPSK modulation format while FHSS uses BFSK**

(1) E. McCune and K. Feher, "Near-far interference experiments using minimum cost hardware", 47<sup>th</sup> Vehicular Technology conference, May 1997

## FHSS systems strongholds (IV)

❑ Non-linear amplification can be used (class-E PA)

- BFSK does not have abrupt phase changes
- Phase modulation exhibits abrupt phase changes

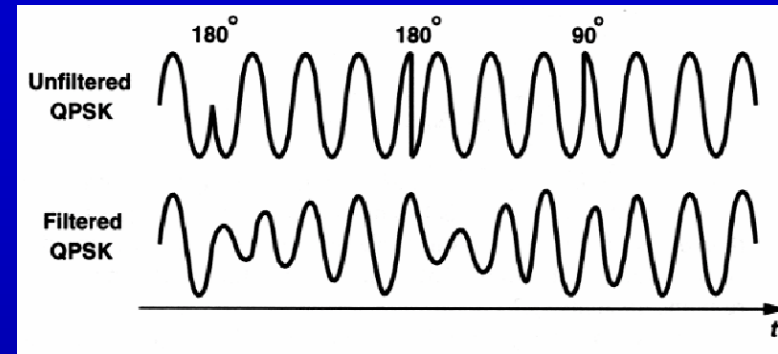
❑ BFSK less bandwidth efficient but more power efficient

❑ Spectral re-growth due to non-linear PAs and non-constant envelope modulation formats can increase noise level in adjacent channels

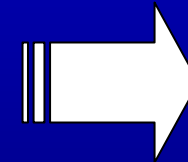
❑ FSK modulation formats more robust against fading, attenuation and interferences

❑ It can be non-coherently detected

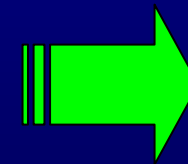
❑ It can be added to the hopping world in the digital domain



Razavi, RF Microelectronics



**Linear amplifiers  
less power  
efficient**



**Lower  
hardware  
complexity and  
lower power  
consumption**

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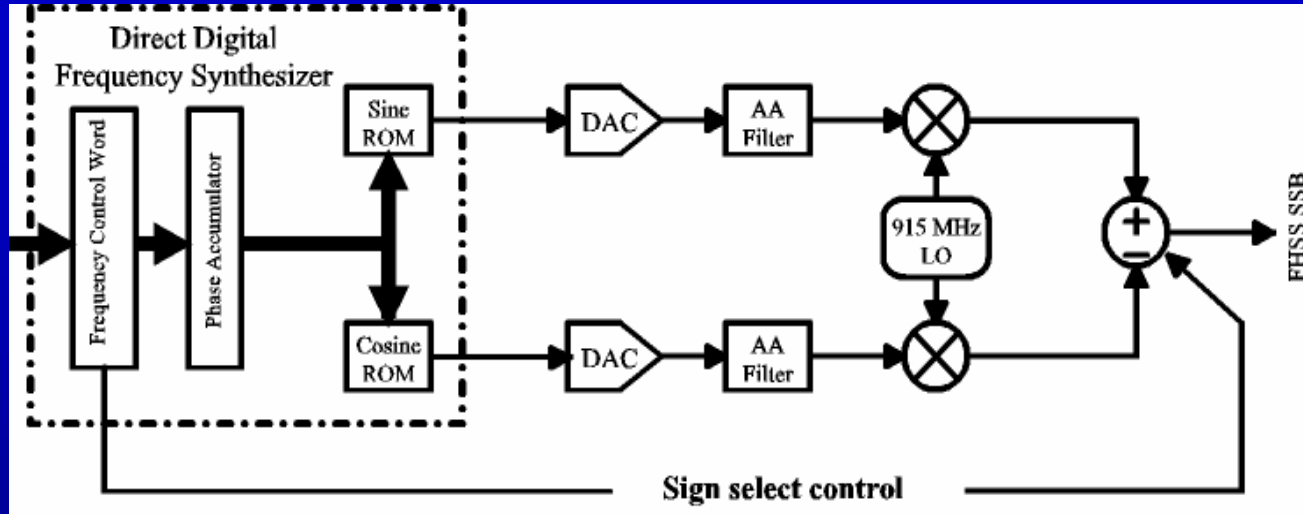
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# FHSS frequency synthesizers (I)

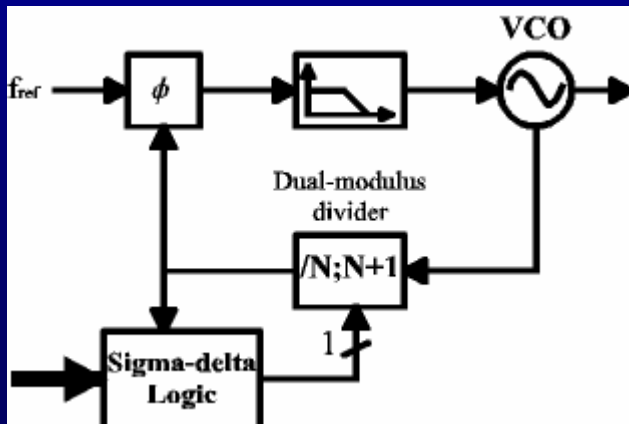
## DDFS architecture



G. Chang et al. 1994

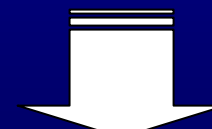
- 40 mW from 3 V
- 80 mW including DACs
- 1 $\mu$ m CMOS design

## Fractional-N PLL architecture



D. Theil et al. 2001

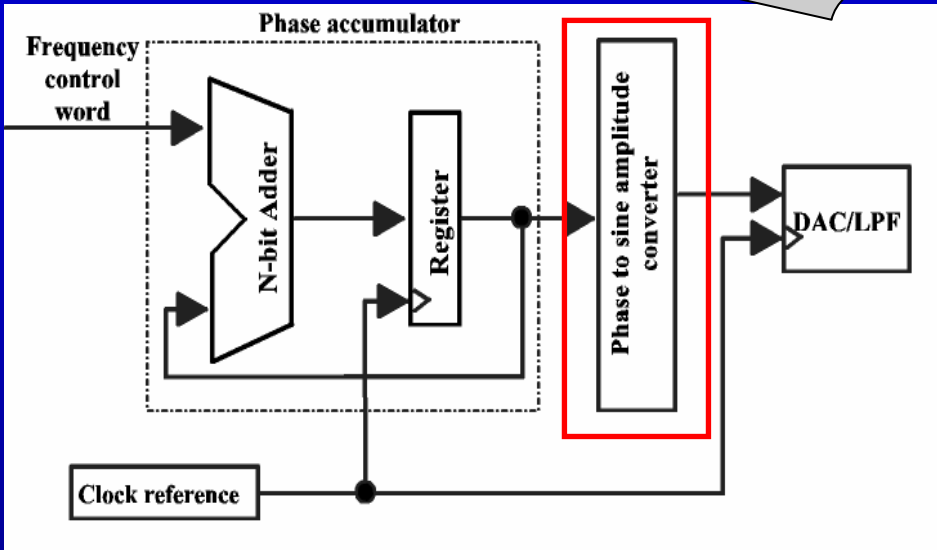
- 55 mW from 2.5 V
- Increased phase noise from  $\Sigma$ - $\Delta$  modulator



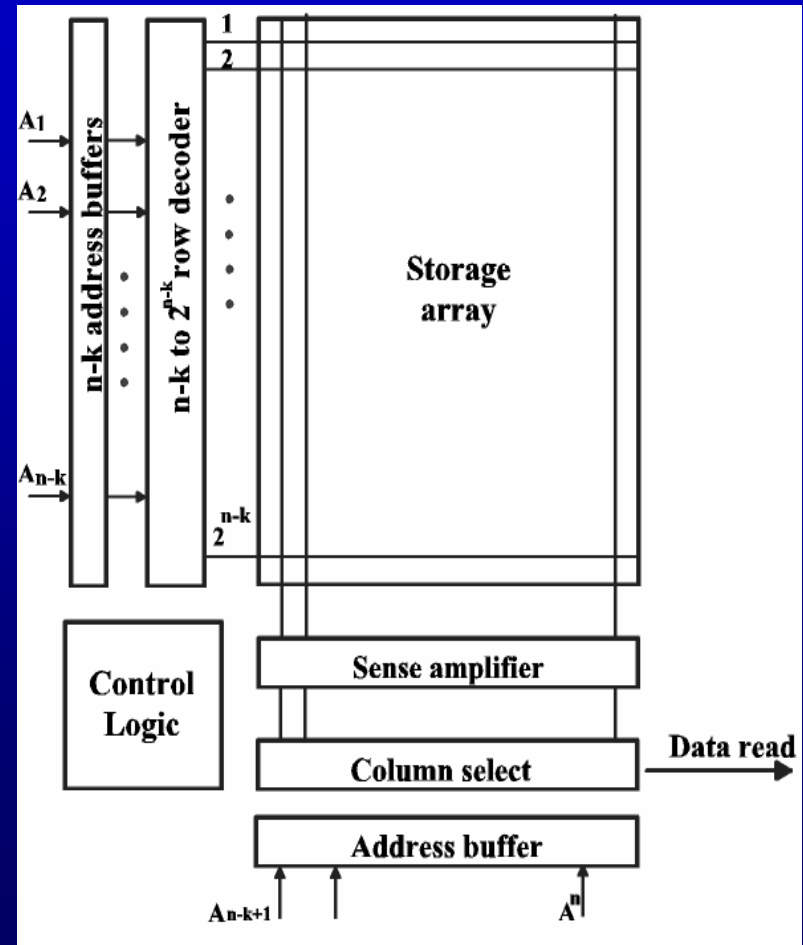
❖ Increase reference frequency or loop filter order

**MORE POWER**

# FHSS frequency synthesizers (II)



## ROM



➤ 192 kbit ROM size (14-bit phase word and 12-bit word-length in amplitude)

➤ Most of the power in the ROM comes from evaluation or pre-charge of the memory cells

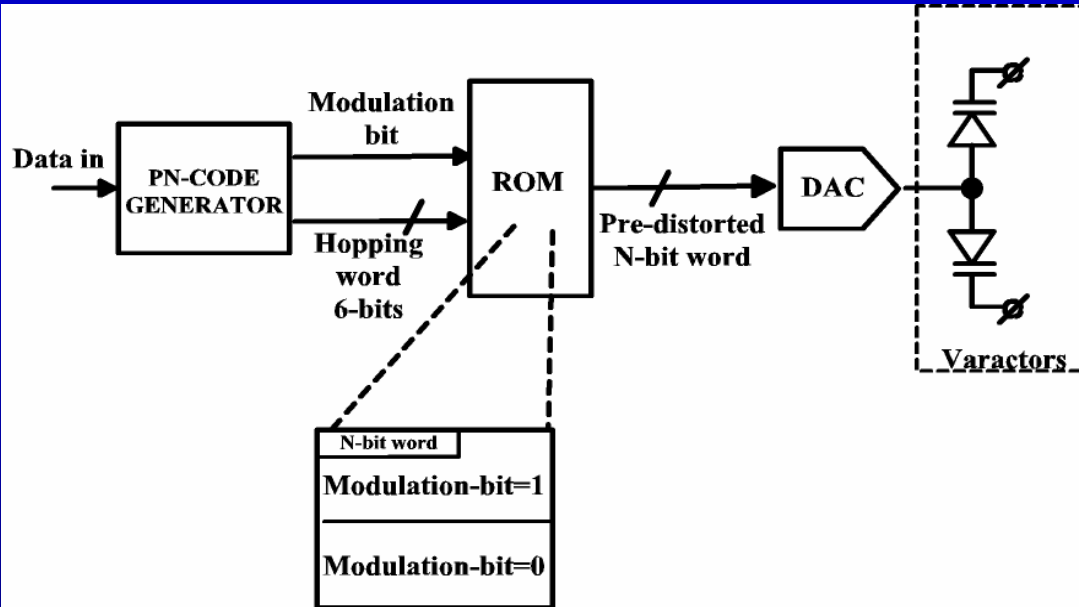


6.25 mW (phase accumulator in CMOS 0.18  $\mu\text{m}$ )

5.4 mW (ROM in CMOS 0.18  $\mu\text{m}$ )

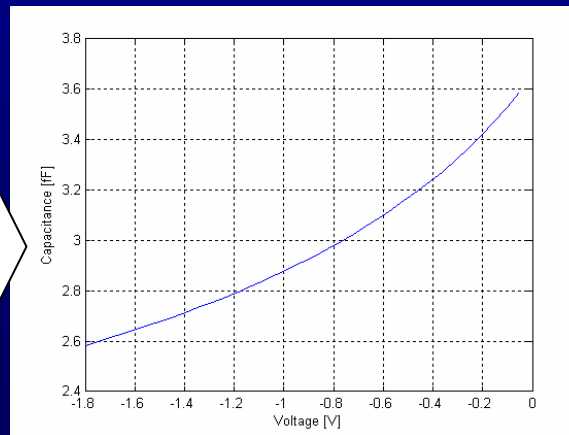
# Pre-distortion based synthesizers (I)

## Architecture

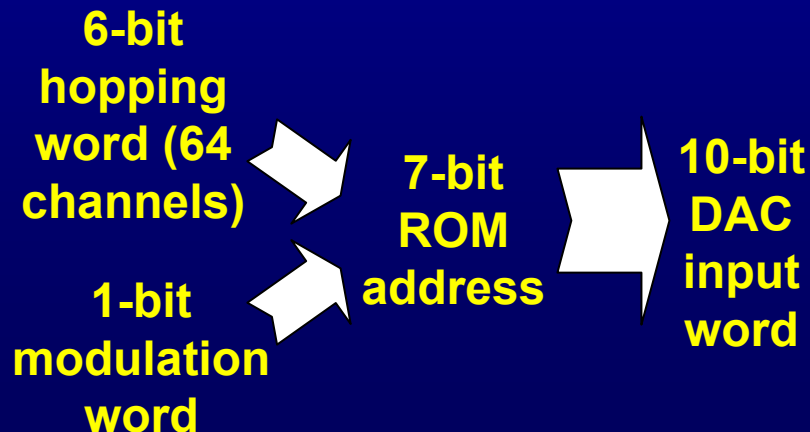


- ❑ ROM size:  $2^7 \times 10 = 1280$  bits
- ❑ No constraints on DAC dynamic linearity
- ❑  $< 100 \mu\text{A}$  DAC feasible
- ❑ No PLL required  $\rightarrow$  very small start-up time

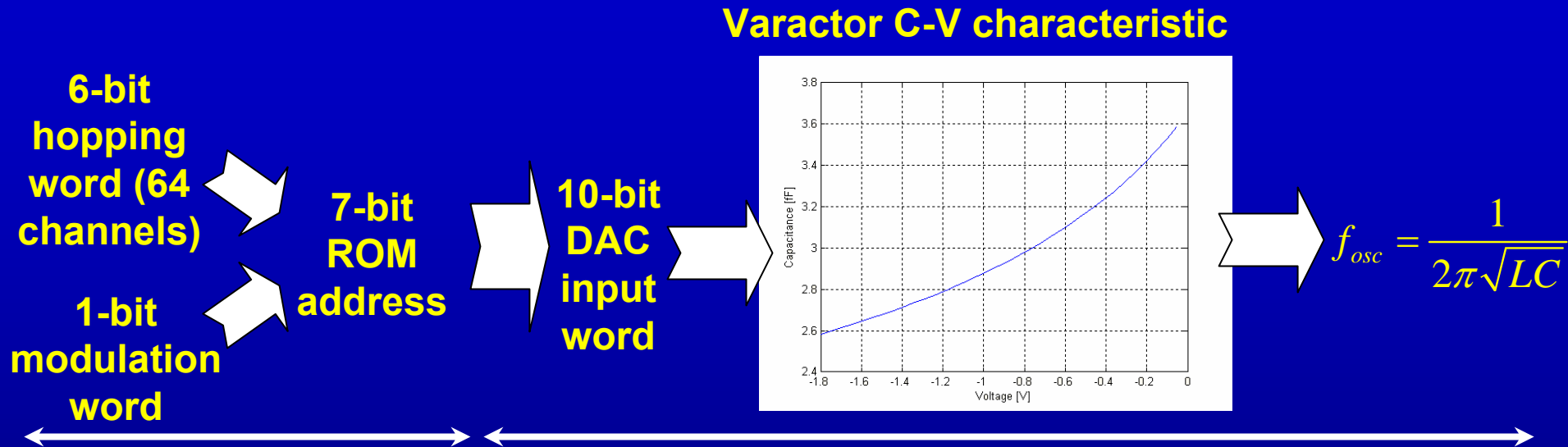
## Varactor C-V characteristic



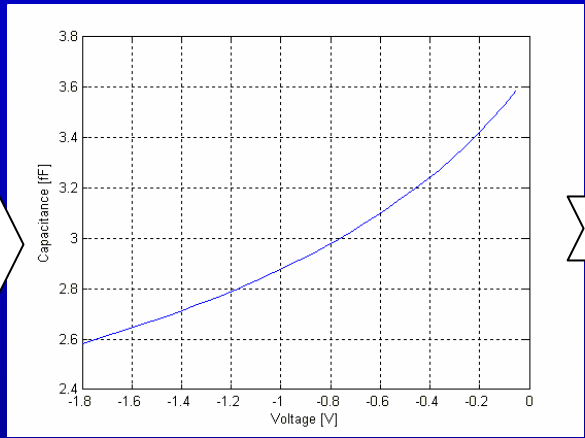
$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$



# Pre-distortion based synthesizers (II)



Varactor C-V characteristic



LINEAR

NON-LINEAR:

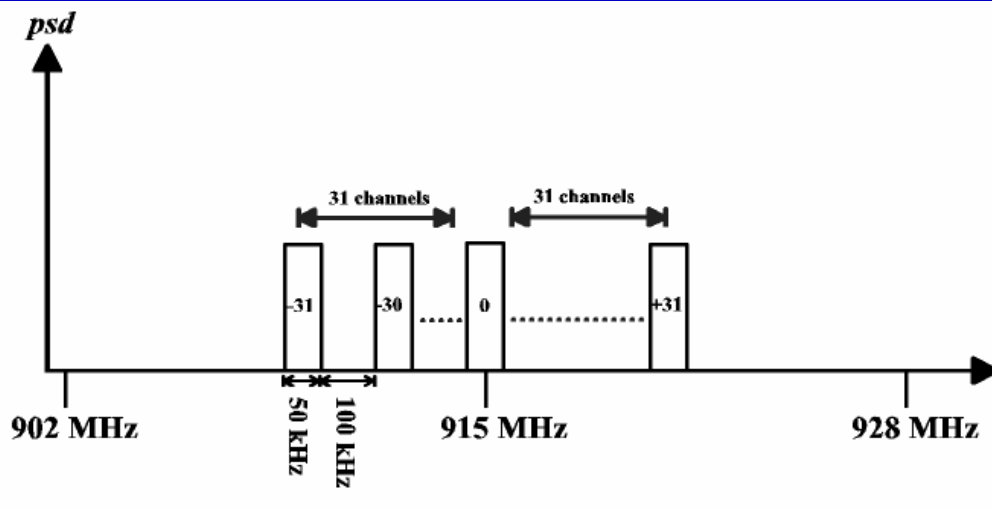
- ❖ DAC Integral-non-linearity
- ❖ Varactor C-V characteristic
- ❖  $f \sim \frac{1}{\sqrt{C}}$

Orthogonal PN-codes

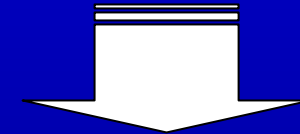


Frequency-hopping bin sequences are non-orthogonal

# Pre-distortion based synthesizers (III)

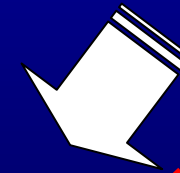


- Inter-channel distance = 150 kHz
- Maximum shift in bin center frequency smaller than 100 kHz



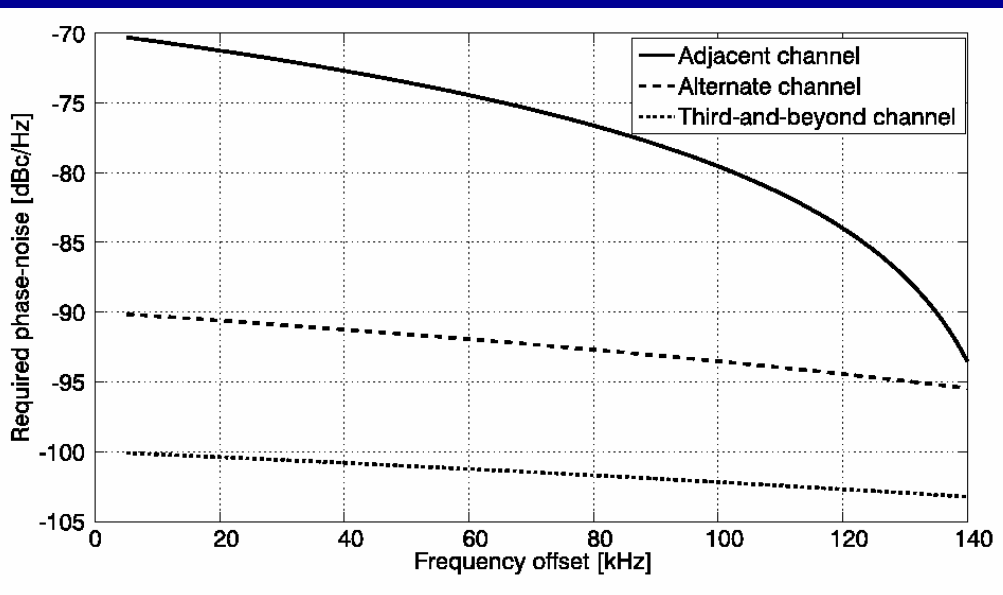
- Reciprocal mixing will reduce SNR due to smaller channel space

- Require better phase-noise performances

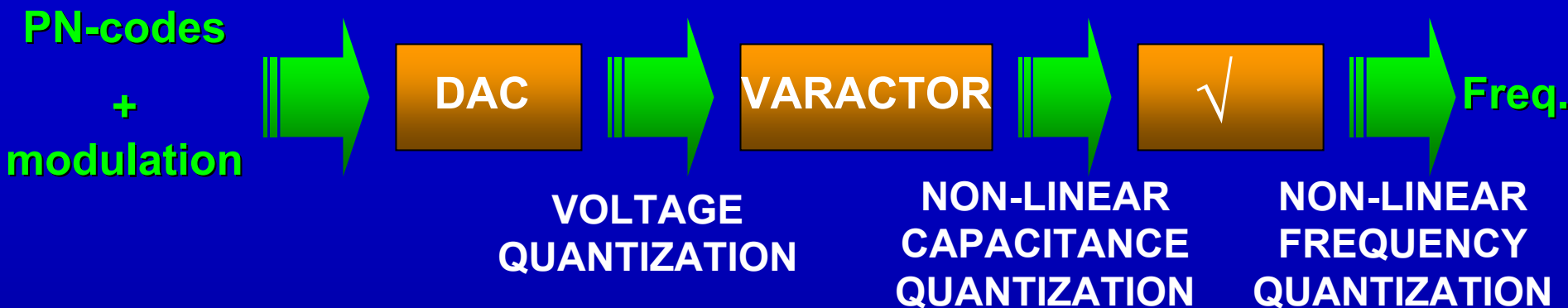


~~MORE POWER~~

Accepting 0.5 dB SNR degradation → 25 kHz maximum residual frequency offset



## Pre-distortion based synthesizers (V)



### Square-root non-linearity

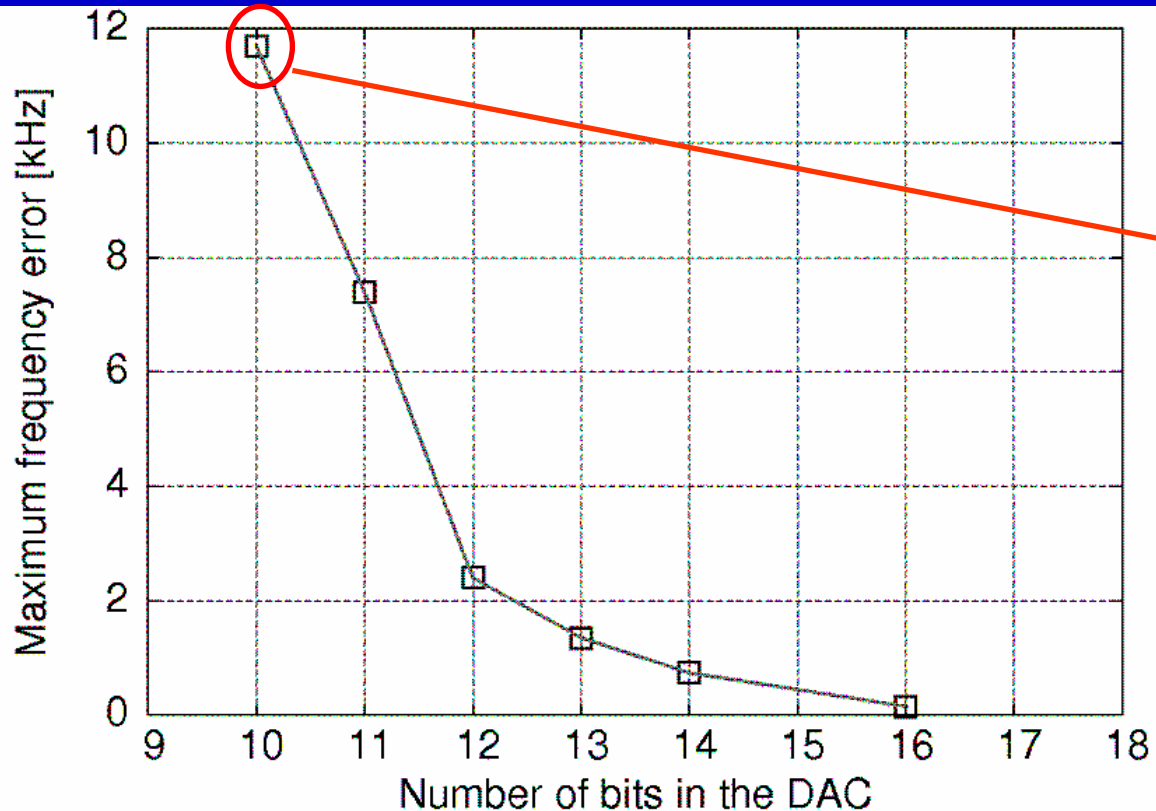
- At higher frequencies the synthesized capacitance is the smallest possible
- Quantization error → the largest frequency deviation
- The varactor is highly linear in this voltage range

### Varactor non-linearity

- At smaller frequencies the varactor is highly non-linear
- Synthesized capacitance is the largest possible
- Error due to the quantization error caused by the square-root relation is the smallest possible

**Varactor non-linearity has the biggest effect → 2.2 mV voltage step required → 10-bit DAC resolution**

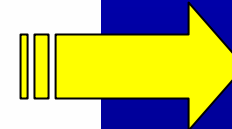
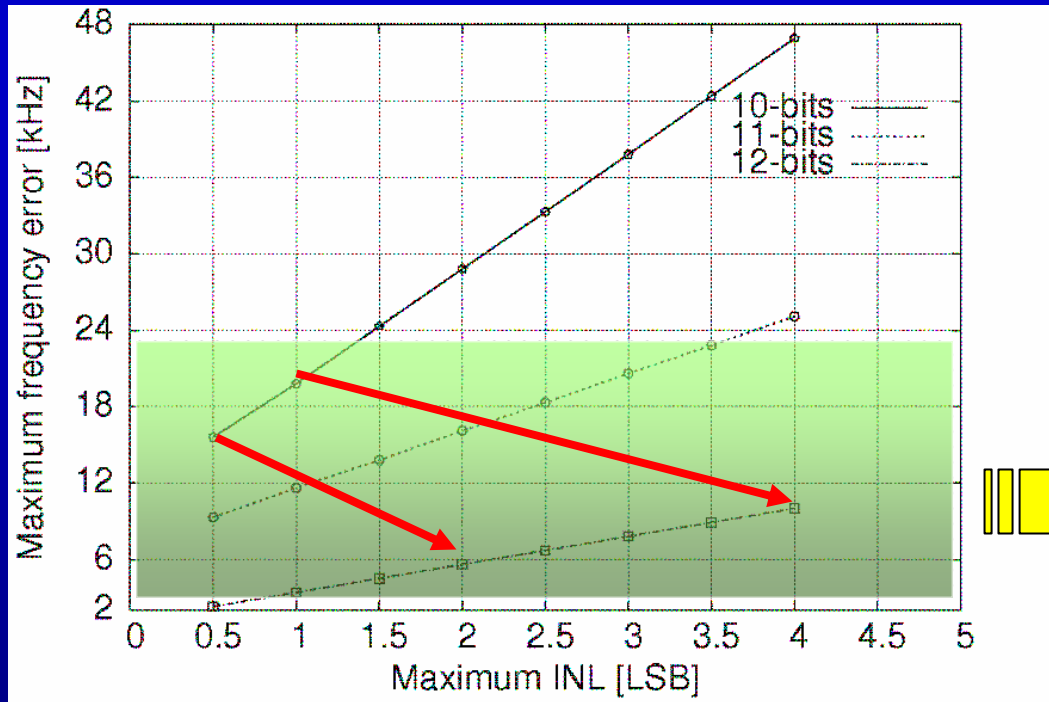
## Pre-distortion based synthesizers (VI)



Simulink simulation showed a 12 kHz maximum residual frequency error after predistortion with a 10-bit DAC and INL of the DAC equal to zero (ideal DAC)

- ❑ From theory the predicted residual frequency error after pre-distortion is 15 kHz
- ❑ Accuracy in the frequency synthesis can be improved by increasing the DAC resolution

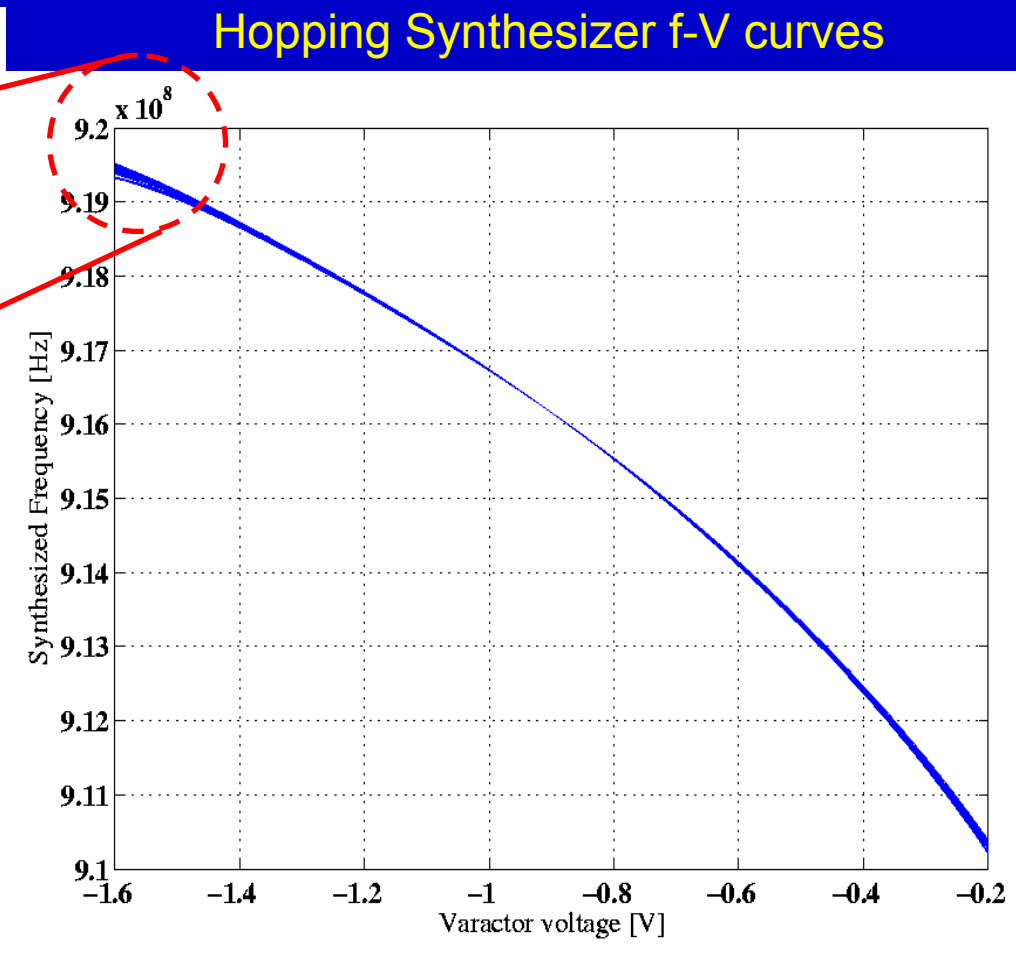
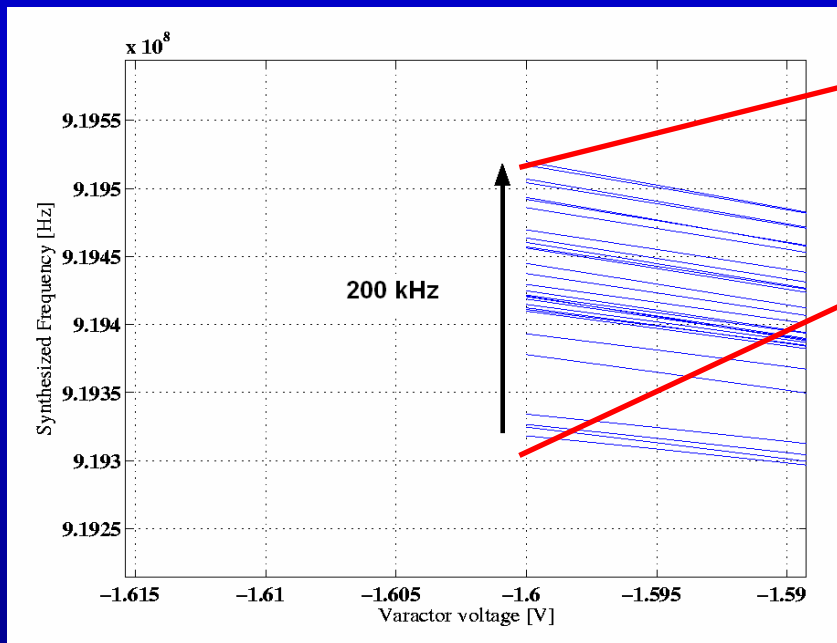
## Pre-distortion based synthesizers (VIII)



**USEFUL  
AREA**

- ❑ DAC INL will increase the residual frequency error
- ❑ INL is process (and therefore IC) dependent → cannot be 100% pre-corrected
- ❑ For a residual frequency offset smaller than 25 kHz a 10-bit DAC with  $INL_{max} < 1.5$  LSB can be chosen
- ❑ Resolution can be traded for linearity (see red lines)

# Pre-distortion based synthesizers (IX)



The standard deviation of the maximum frequency spread has been calculated to be:

$$\sigma \approx 33 \text{ kHz}$$



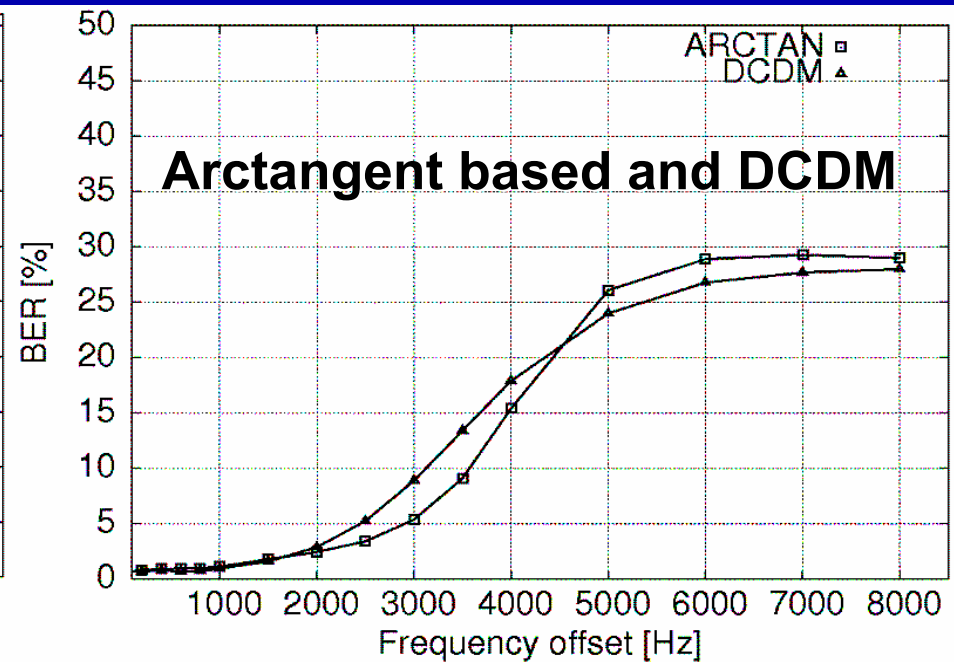
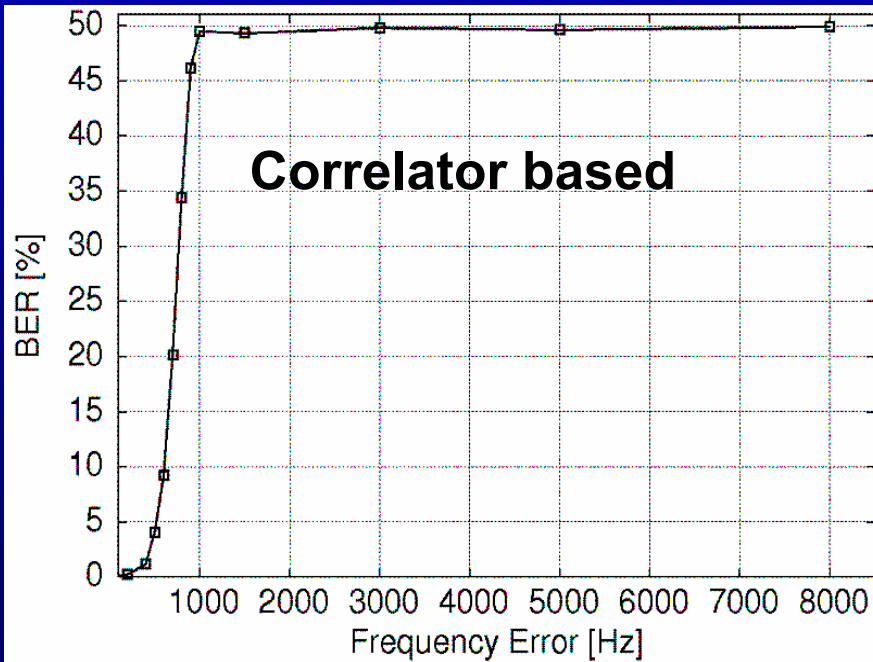
**RELATIVE POSITION  
CHANNELS PRESERVED**

**30 Samples measured (same batch)**

# Receiver design issues (I)

## □ Different potentially ultra-low power demodulator topologies

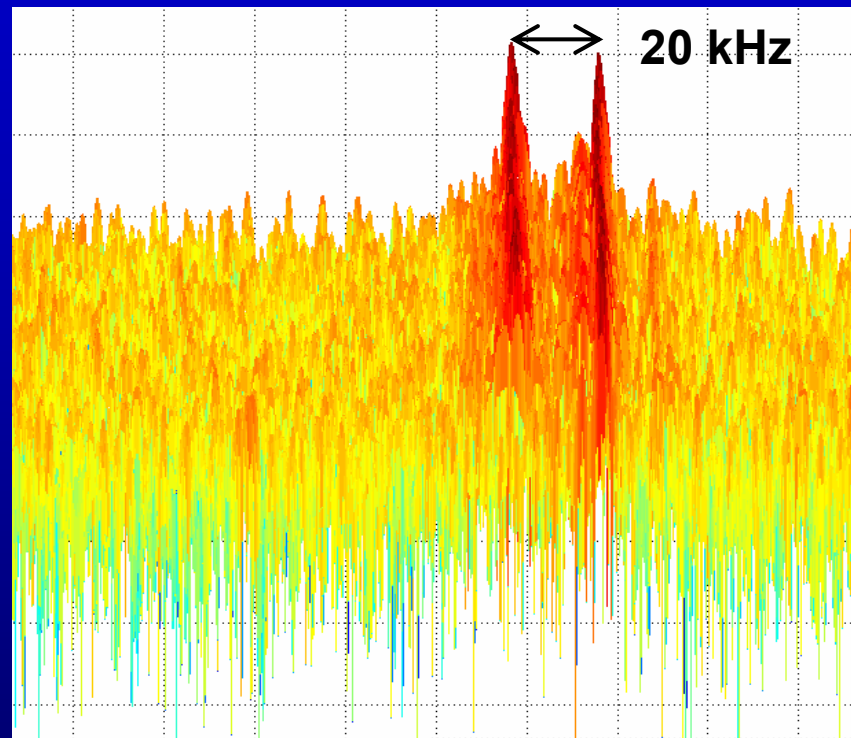
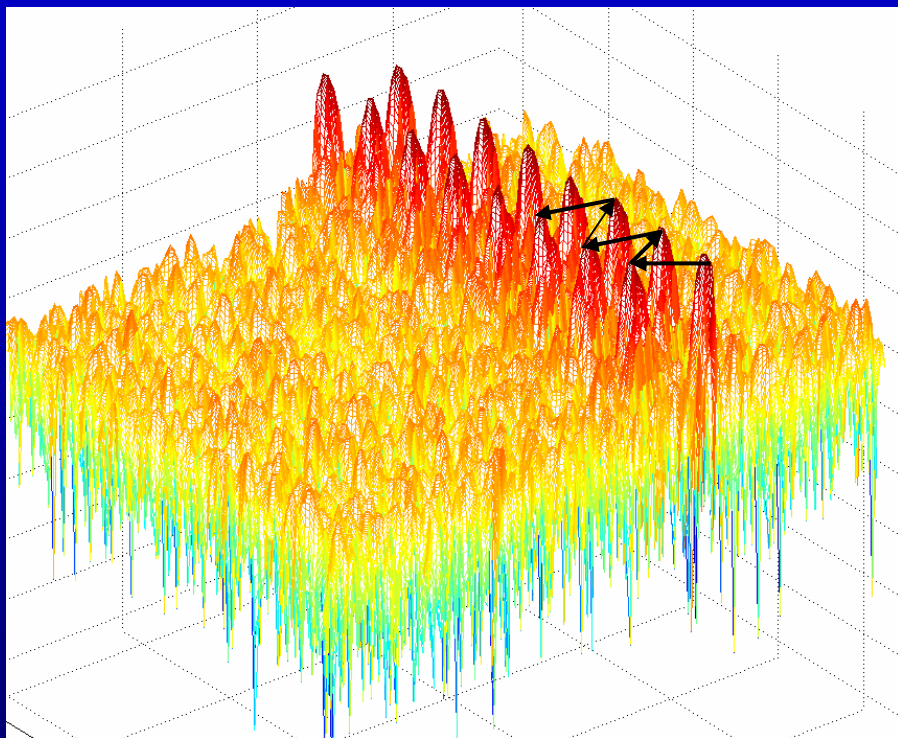
- Correlator based
- DCDM and arctangent based
- ST-DFT based



**BOTH TOPOLOGIES REQUIRE AN AFC LOOP → MORE POWER!**

## Receiver design issues (II)

## SHORT-TIME DFT ALGORITHM



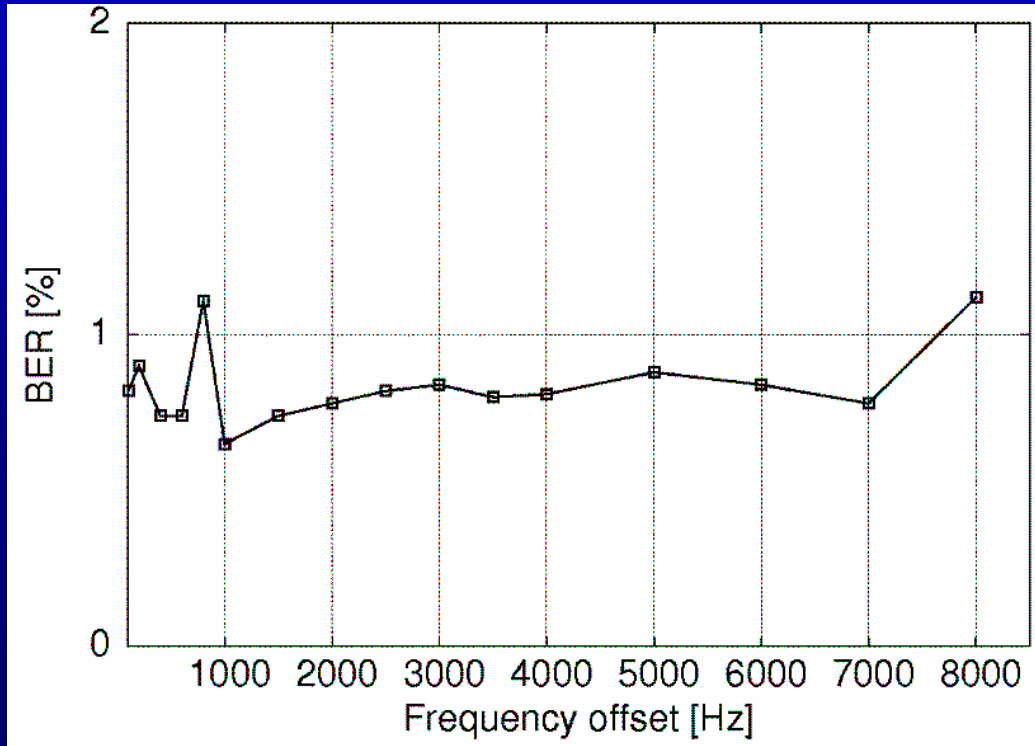
- ❑ Differential encoding is applied
- ❑ Required frequency window equal to  $BW + 2 \cdot f_{\text{off}(\text{max})} = 100 \text{ kHz}$
- ❑ With 256-point DFT a resolution smaller than 400 Hz can be achieved

## Receiver design issues (III)

❑ 103 nJ/FFT (256-point and 8-bit)

❑ Power consumption between 100  $\mu$ W and 1 mW for data-rate between 1 and 10 kbps (0.18  $\mu$ m CMOS process and 1.5 V operation)<sup>1</sup>

### ST-DFT BER performances



❖ Power supply and temperature variation effect on the synthesized frequency cancelled out by differential encoding

❖ DAC INL effect needs to be cancelled:

- DSP techniques
- Dedicated pre-distortion table
- Calibration loop

(1) B. H. Calhoun et al. "Design considerations for ultra-low energy wireless microsensor nodes" IEEE Transaction on Computers, 2005

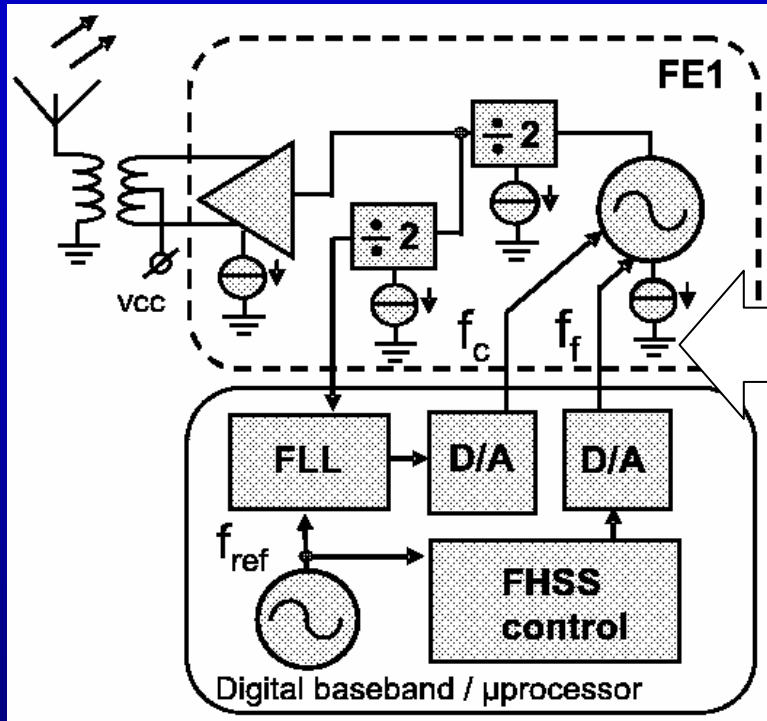
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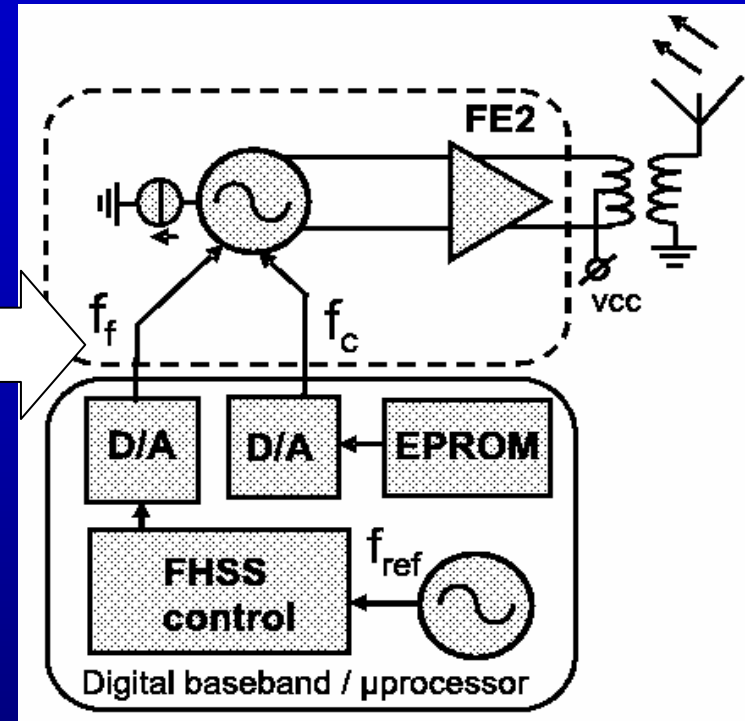
# FHSS pre-distortion based transmitter design (I)

## Conventional FE



915 MHz  
ISM band

## Single RF block FE

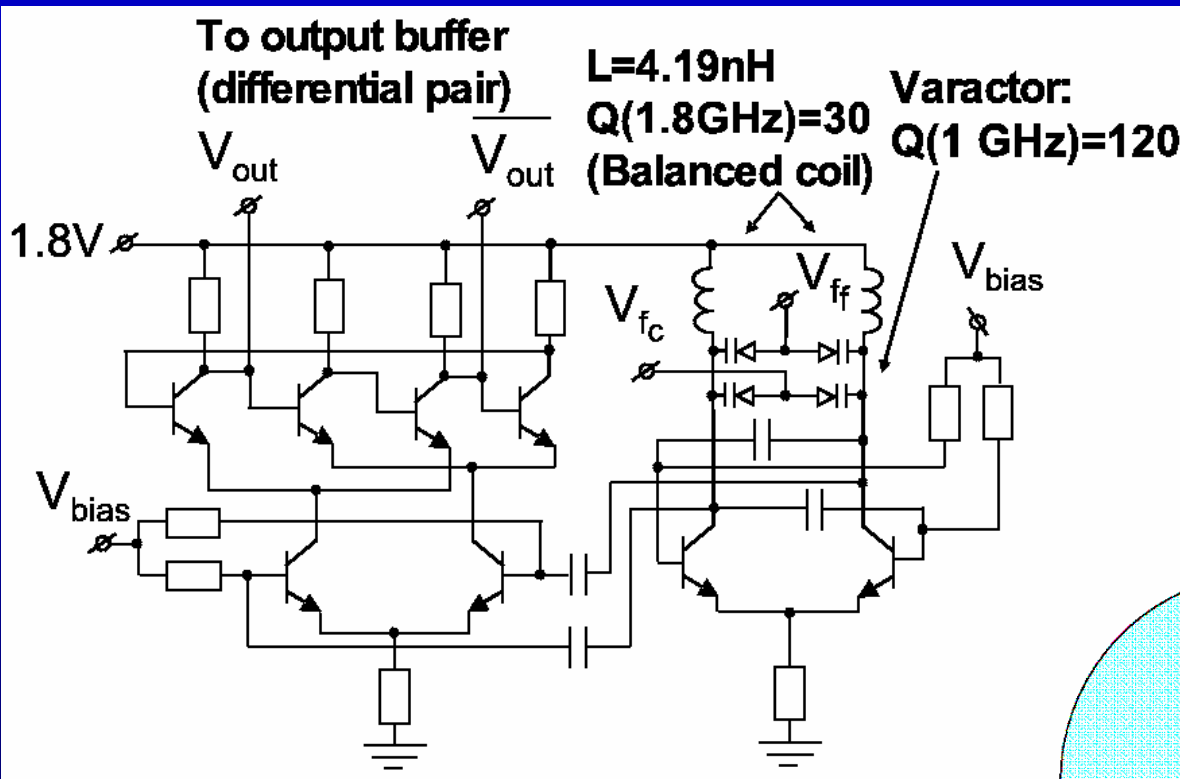


- ❑ Oscillator+divider
- ❑ -25 dBm output power
- ❑ Coarse calibration through FLL loop
- ❑ 64 channels

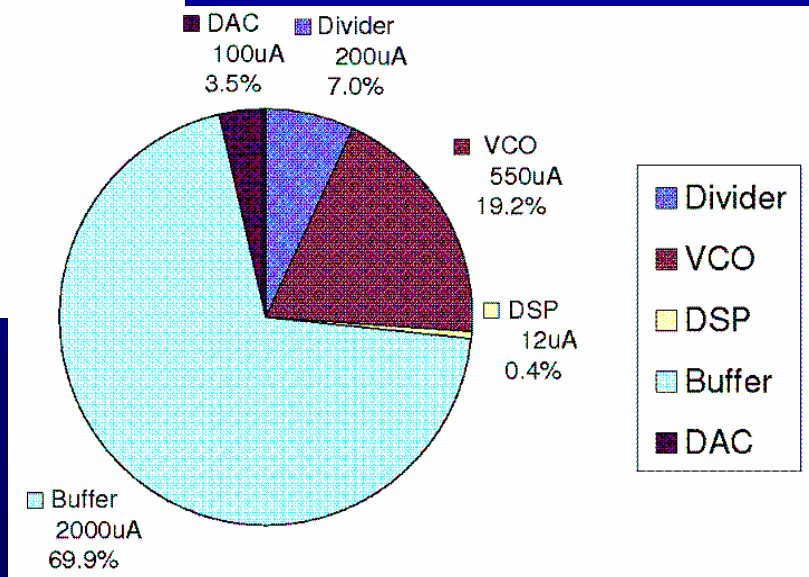
- ❑ Power VCO based
- ❑ -18 to -5 dBm output power
- ❑ Coarse stored in the EPROM
- ❑ 64 channels

# FHSS pre-distortion based transmitter design (II)

## Transistor level schematic of FE1



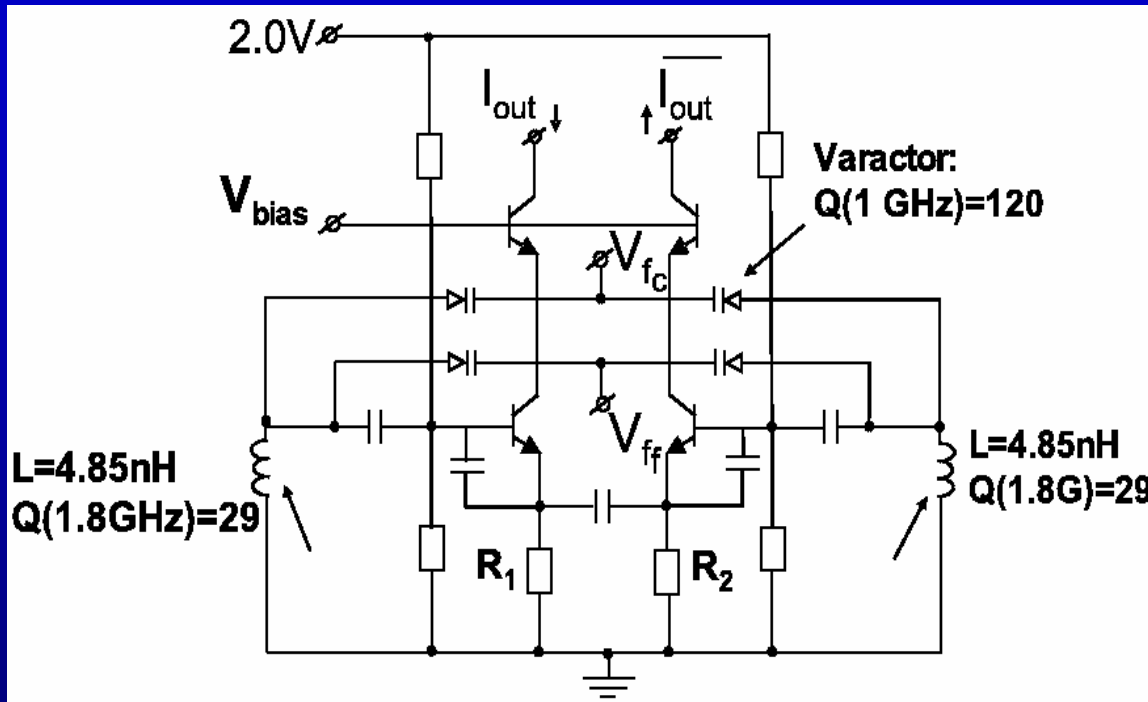
- ❑ Buffer not optimized
- ❑ Front-end power consumption =  $750\mu\text{A}$
- ❑ Buffer power accounts for 70% of the total power



**FRONT-END POWER CONSUMPTION EQUAL TO  $750\mu\text{A}$  FROM  $1.8\text{V}$**

# FHSS pre-distortion based transmitter design (III)

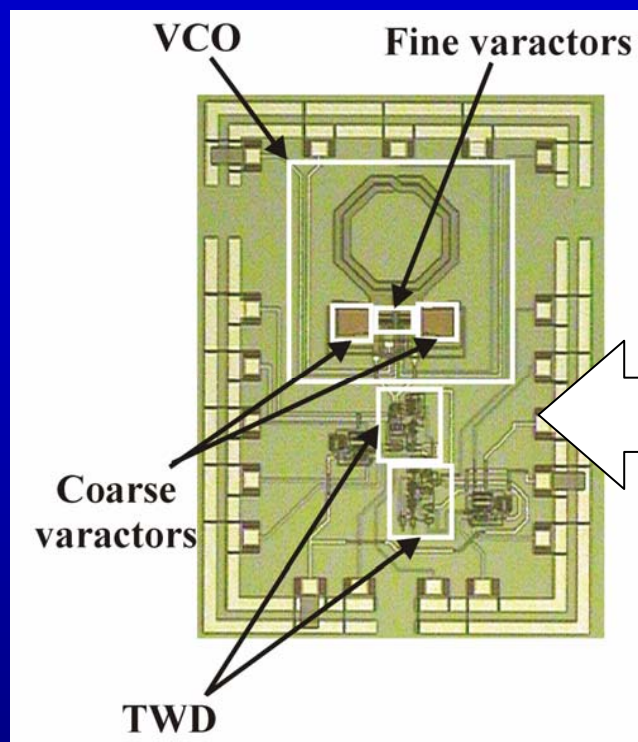
## Transistor level schematic of FE2



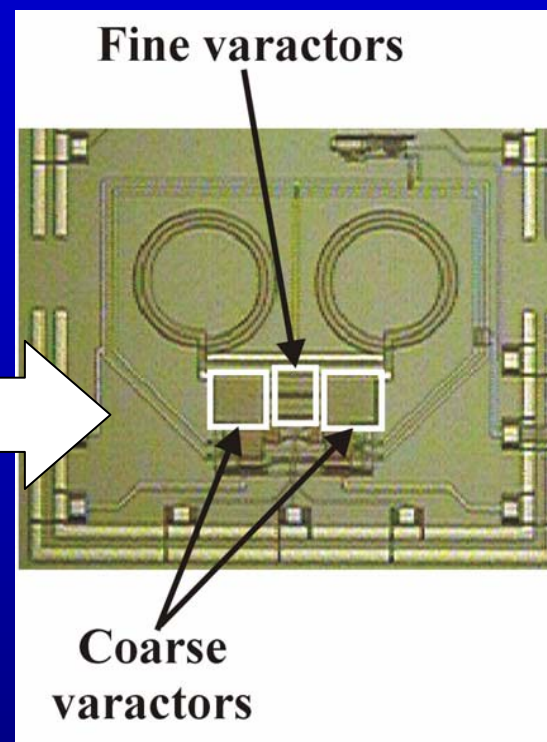
- ❑ Oscillator and PA are merged through cascode transistors
- ❑ Oscillator works at half frequency (915 MHz)
- ❑ Differential Colpitts oscillator
- ❑ 1 mA Front-end power consumption at -18 dBm output power

- ❑ Power consumption is minimized
- ❑ VCO pulling is reduced
- ❑ No PA required
- ❑ Antenna is directly coupled through a balun to the RF front-end

## FHSS pre-distortion based transmitter design (IV)



**SOA bipolar  
technology**



❑ Active area = 2.8 mm<sup>2</sup>

❑ Phase noise = -109 dBc/Hz @ 450 kHz

❑ FE consumes 2.75 mA (including buffer) from 1.8 V

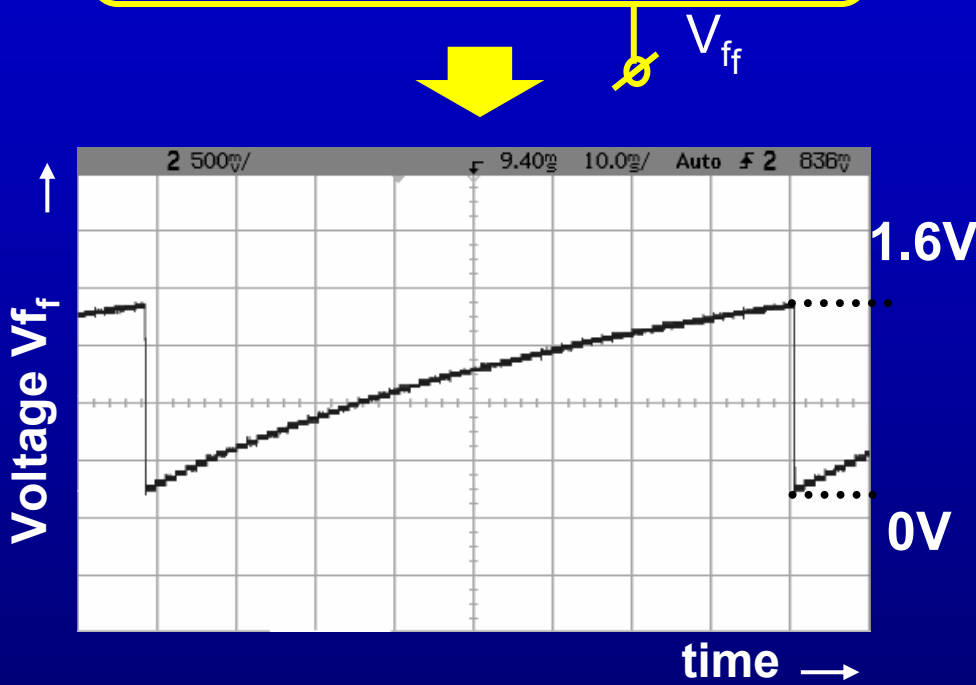
❑ Active area = 3.6 mm<sup>2</sup>

❑ FE consumes only 1 mA at -18 dBm output power

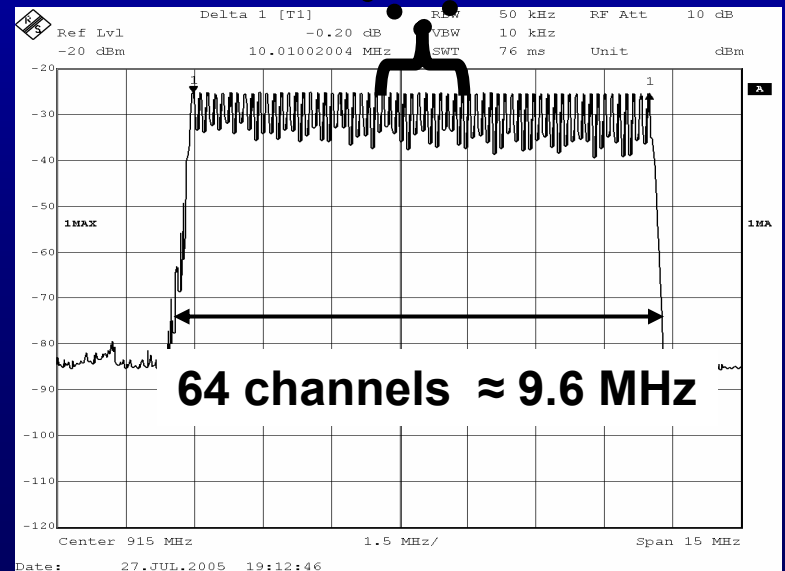
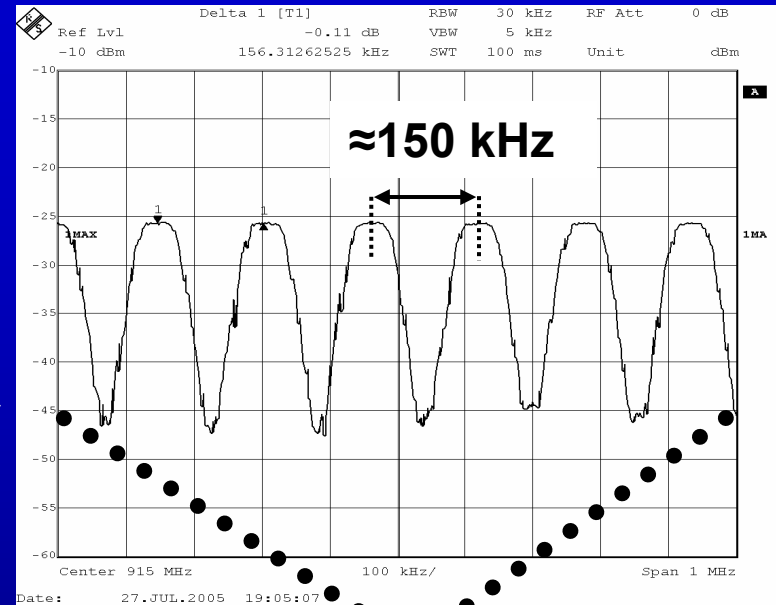
❑ Phase-noise ranges between -102 (-18 dBm) and -115 (-5 dBm) dBc/Hz @ 450 kHz

# FHSS pre-distortion based transmitter design (VI)

Digital base-band: predistortion look-up table and D/A converter



TX front-end FE2 (or TX FE 1)

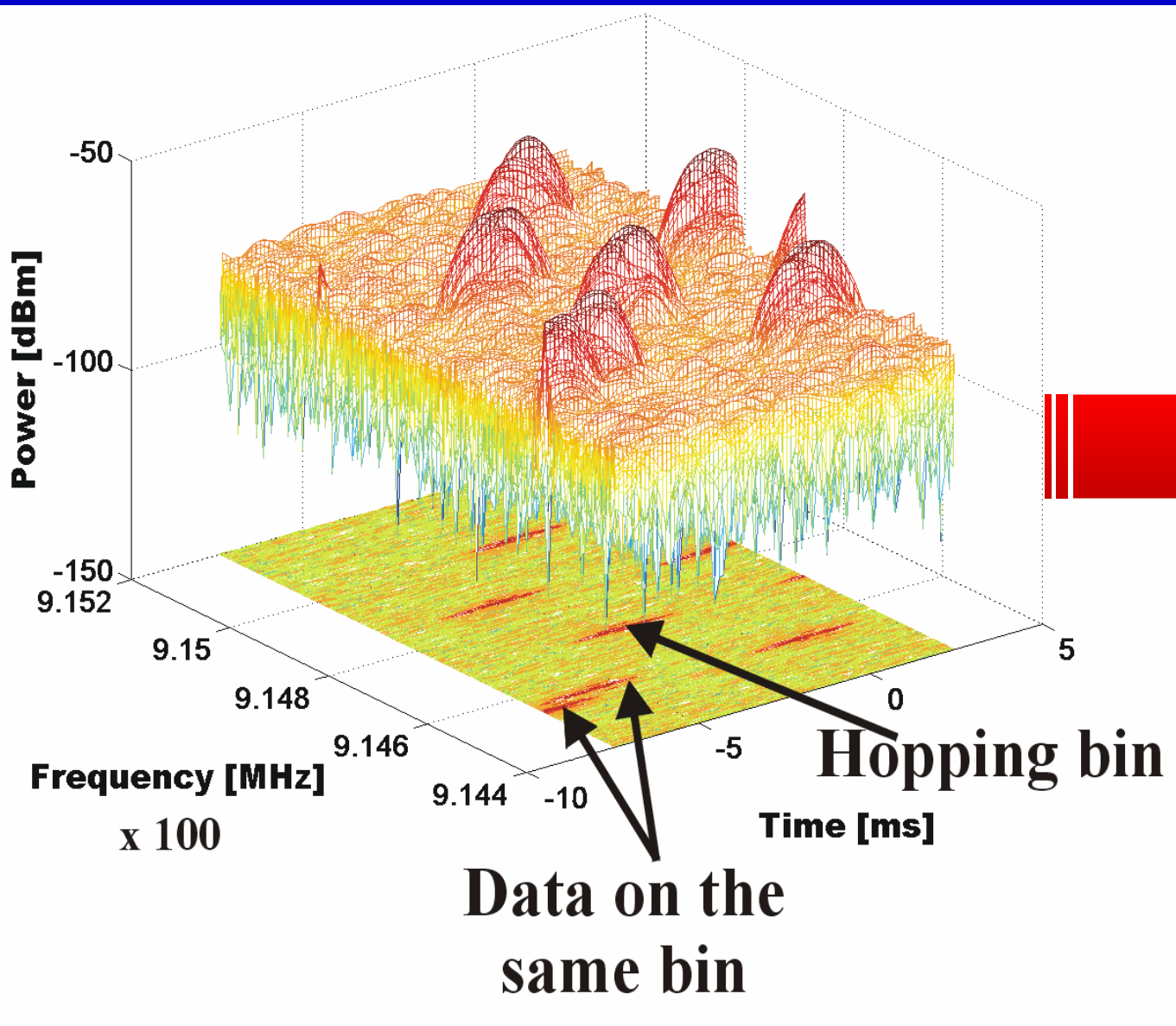


## FHSS pre-distortion based transmitter design (VII)

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- ❑ The maximum measured frequency deviation from the ideal grid is smaller than 5 kHz (12-bit DAC used)
  
- ❑ A wireless link has been set with the realized transmitter
  - Antennas are placed at 8 meters distance in a NLOS condition (indoor office environment)
  - Transmitted power is -25 dBm
  - Data-rate is 1 kbps at 1 khop/s hopping rate
  - Receiver employs a super-heterodyne architecture

# FHSS pre-distortion based transmitter design (VIII)



**MEASURED  
BER  
SMALLER  
THAN 1.1%  
(no FEC  
employed)**

# Outline

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□ INTRODUCTION

□ SYSTEM LEVEL ASPECTS

□ FHSS FREQUENCY SYNTHESIZERS

□ FHSS PRE-DISTORTION BASED TRANSMITTER DESIGN

□ RECEIVER PLANNING

□ CONCLUSIONS

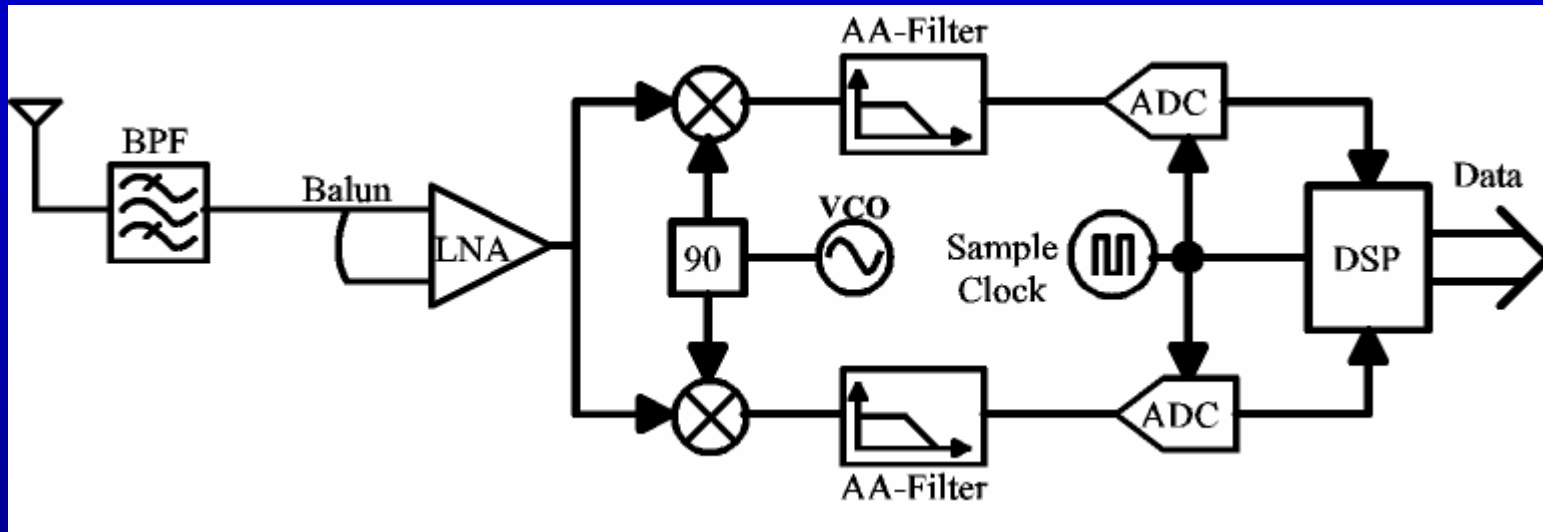
# Receiver planning (I)

## RECEIVER REQUIREMENTS

- ❑ Max communication distance  $\approx 30$  meters
- ❑ Min communication distance  $\approx 0.4$  meters
- ❑ Transmitted power  $\approx -6$  dBm
- ❑ Frequency band = 2.4 GHz ISM band
- ❑ Data rate  $\approx 2$  kbps
- ❑ SNR @ demodulator  $\geq 20$  dB (1% BER)
  - Takes into account deep fading conditions
- ❑ Noise bandwidth 24 kHz (modulation index equal to 5)
- ❑ Oversampling ratio = 4
- ❑ Two tone interferers power =  $-39$  dBm

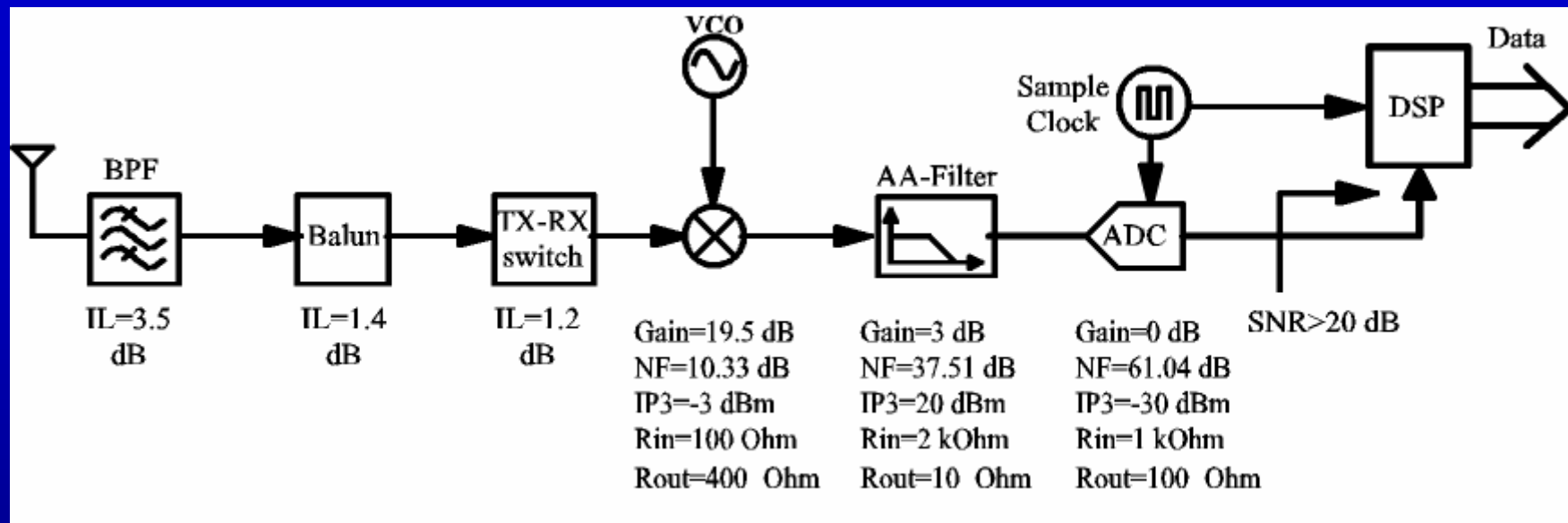
# Receiver planning (I)

## Proposed receiver architecture



- ❑ Zero-IF architecture with wideband-FSK modulation
- ❑ Low-frequency ADC
- ❑ Simplified front-end
- ❑ Target power consumption 2 mW (1.8 V supply)

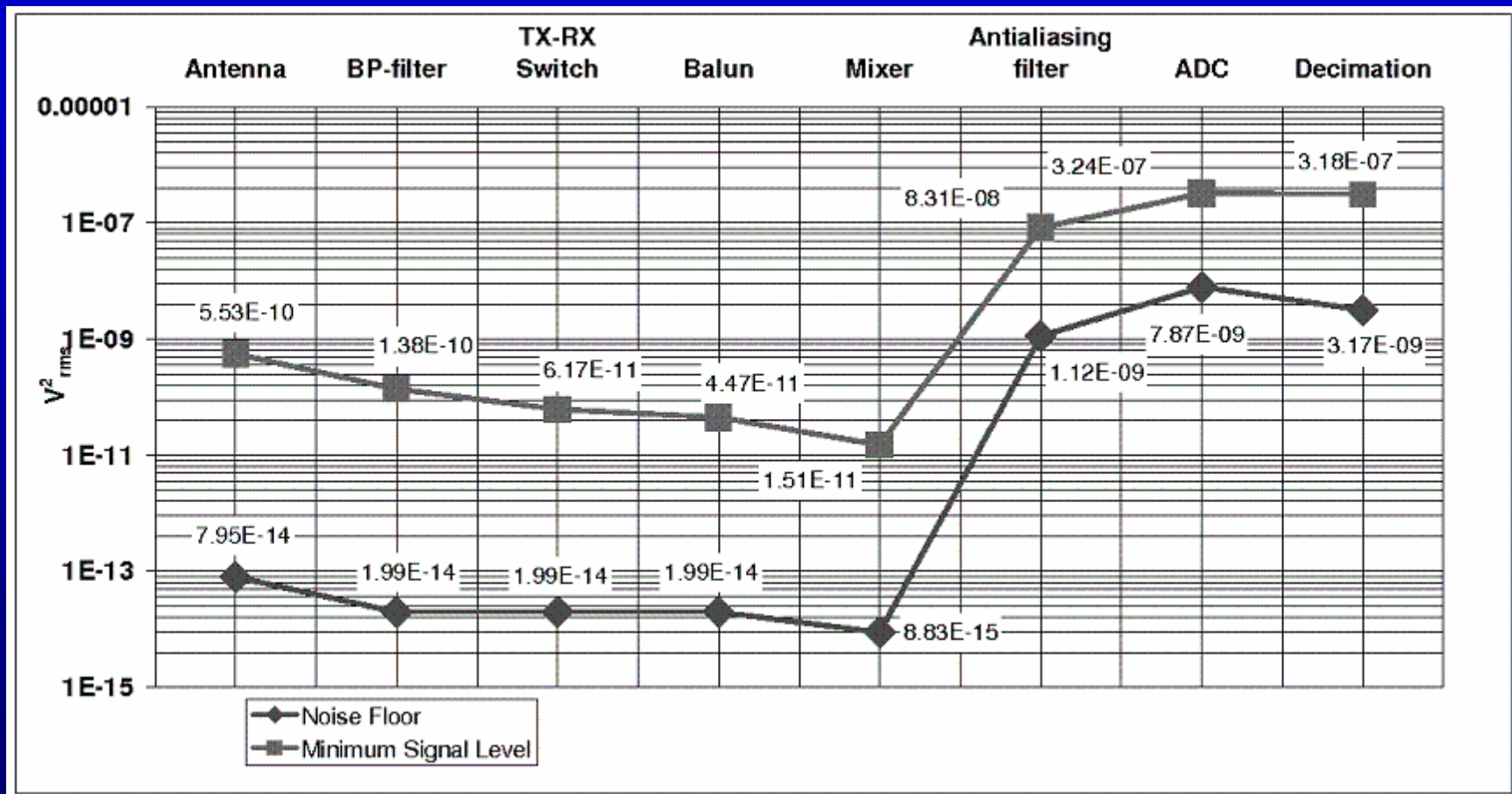
## Receiver planning (II)



- ❑ LNA and mixer merged to reduce power consumption
- ❑ Oversampling (factor 4) to relax AA-filter specs
- ❑ ADC → Delta-Sigma is the best candidate
- ❑ Channel bandwidth  $\geq 50$  kHz
- ❑ No AGC used → Maximum receiver power gain  $\leq 34$  dB

➤ ADC Full-scale Range  $\approx 0.4$  V

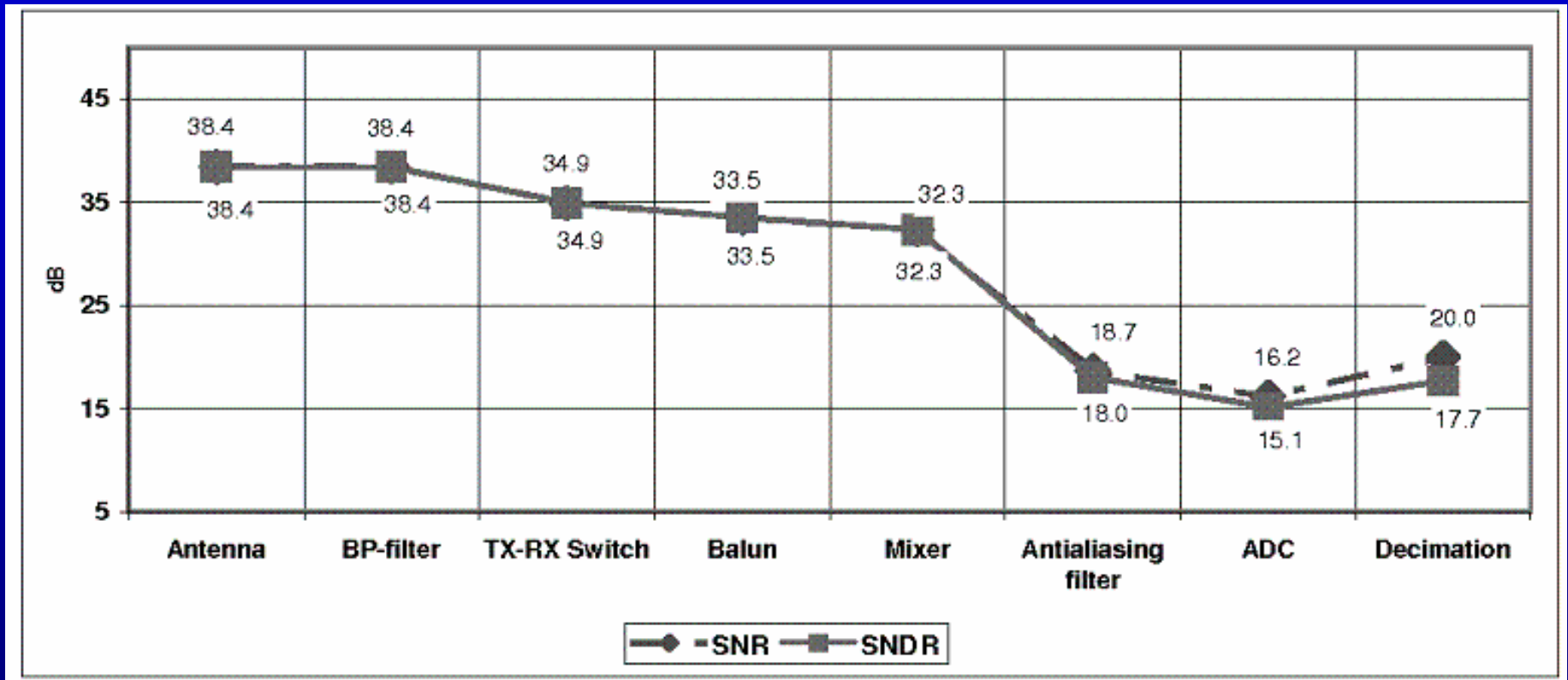
## Receiver planning (III)



❑ Most of the gain in the merged LNA-mixer

❑ 6 dB gain in the AA-filter

## Receiver planning (IV)

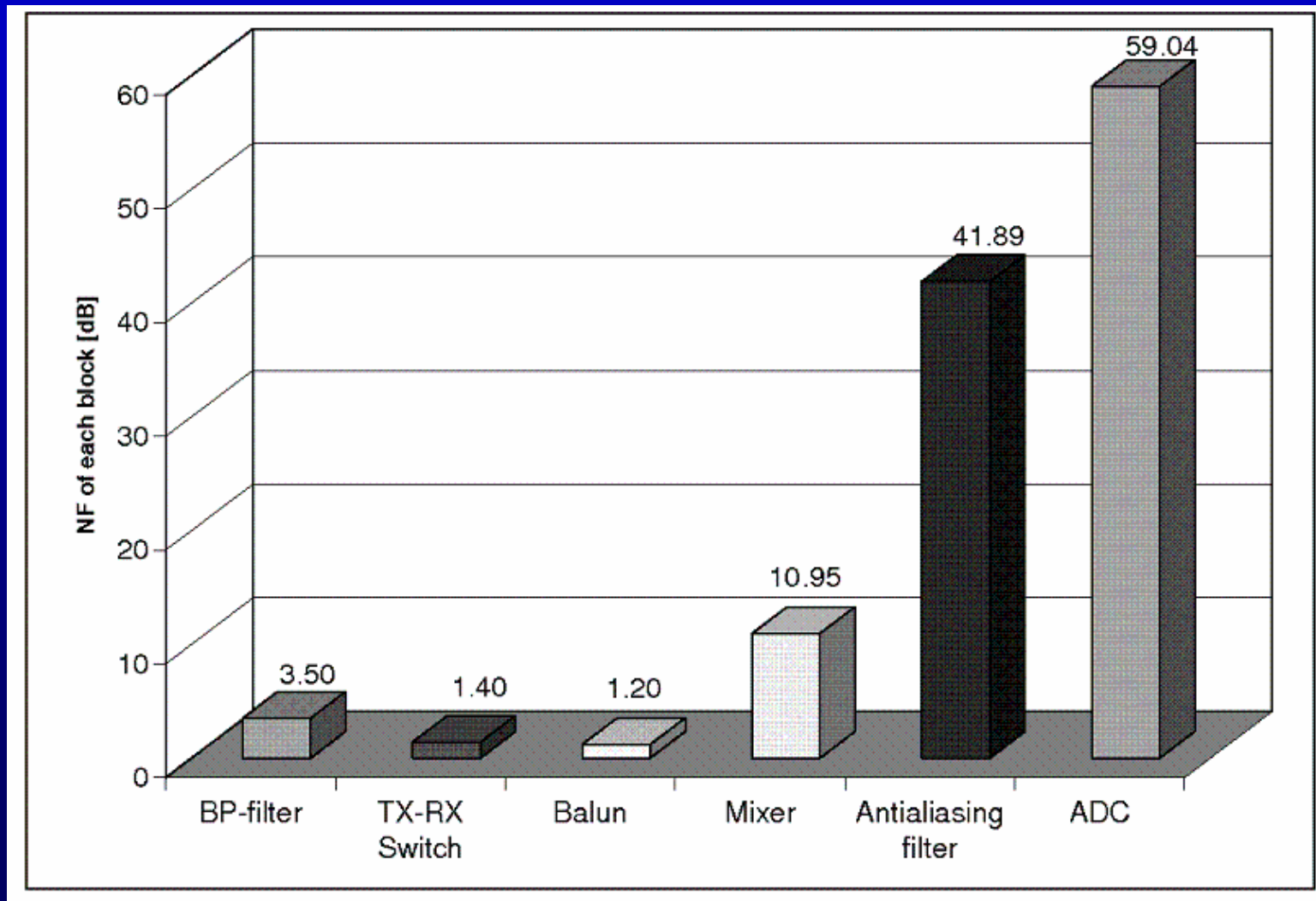


❑ Intermodulation distortion needs in zero-IF architecture a very linear filter

❑ The signal is allowed to be 3 dB above the sensitivity level (achieving the same BER)

# Receiver planning (V)

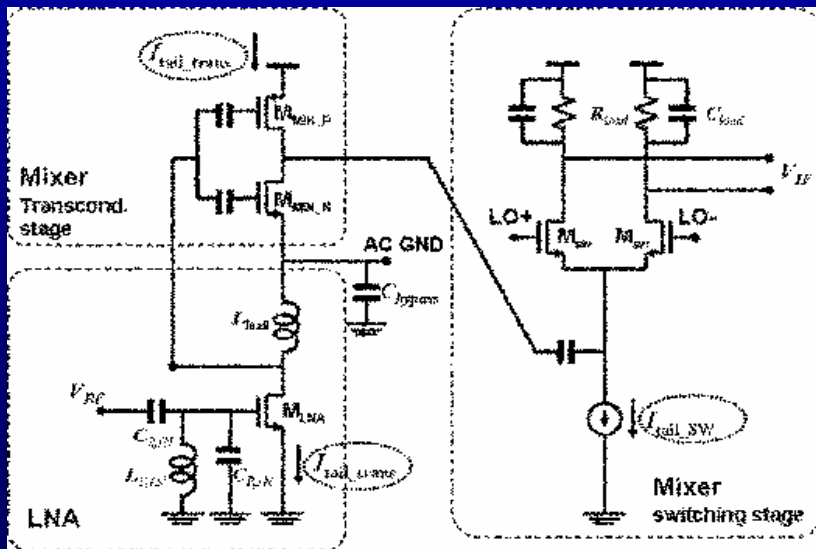
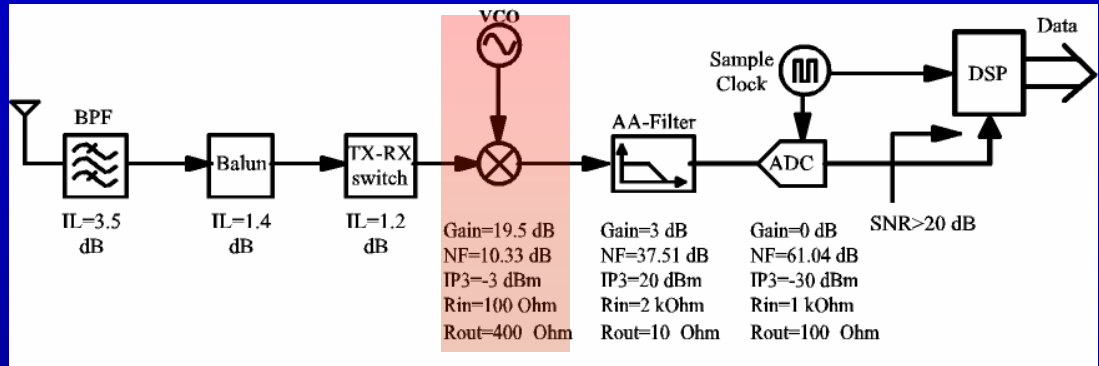
## NOISE FACTOR OF EACH STAGE



# Receiver planning (VI)

## LNA-MIXER SUMMARY

- ❑ 19.5 dB voltage gain
- ❑ 10.33 dB NF
- ❑ IP3 = -3 dBm

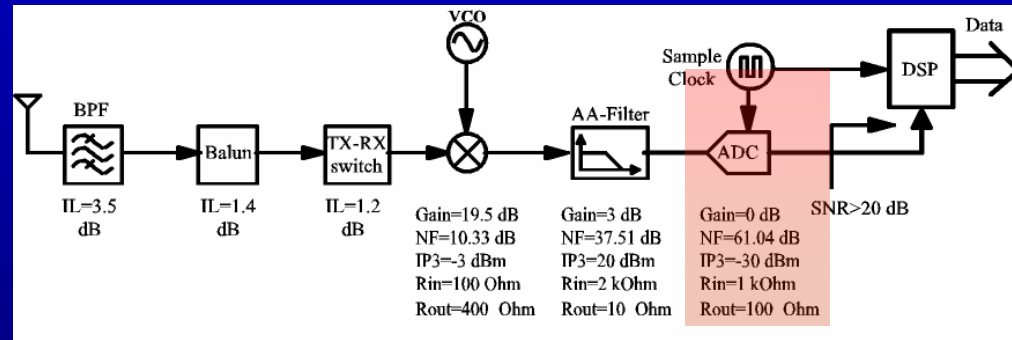


- ❑ 31.5 dB conversion gain
- ❑ 11.8 dB NF @ 10 MHz
- ❑ 500  $\mu$ A current consumption
- ❑ 1 V power supply

# Receiver planning (VIII)

## ADC SUMMARY

- ❑ Sampling rate = 192 ksample/s
- ❑ SNR= 72 dB → ENOB = 11.67 bits
- ❑ ADC FSR = 0.4 V
- ❑ ADC power supply = 1.2 V
- ❑ NF ≤ 61 dB
- ❑  $Z_{in} = 1000 \Omega$ ,  $Z_{out} = 100 \Omega$



$$FOM = \frac{P}{2^{ENOB} \times f_{sample}}$$



**0.4 pJ/conversion  
@ 250 μW power  
consumption**

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## Conclusions

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- ❑ Increasing the data rate does not improve power efficiency at very-low duty cycle
- ❑ FHSS based architectures combine robustness and low-power capabilities
- ❑ State-of-the-art FHSS synthesizers are too power hungry
- ❑ A novel FHSS synthesizer based on digital pre-distortion simplifies hardware requirements
- ❑ A TX prototype showed an overall power consumption 7 times smaller than the state-of-the-art
- ❑ Raw BER smaller than 1.1% at -25 dBm transmitted power and 1.1 mA overall current consumption
- ❑ Direct conversion requires at low power further improvements in NF and gain
- ❑ ADC is feasible at low power levels