



Technology, Inc.

A Sampling Mixer Allowing Heterodyne Conversion to Baseband With No Local Oscillator and Multi-GHz Operation on a Standard Digital CMOS Process.

Presenter: Martin Mallinson
Kelowna Design Center
July 2006

ESS Technology, Inc



Audio



Video



Imaging





Outline

- Introduction
- Functional description
- Advantages/constraints
- A circuit level spice example
- A layout implementation
- Other considerations
- Conclusion
- Acknowledgements





Introduction

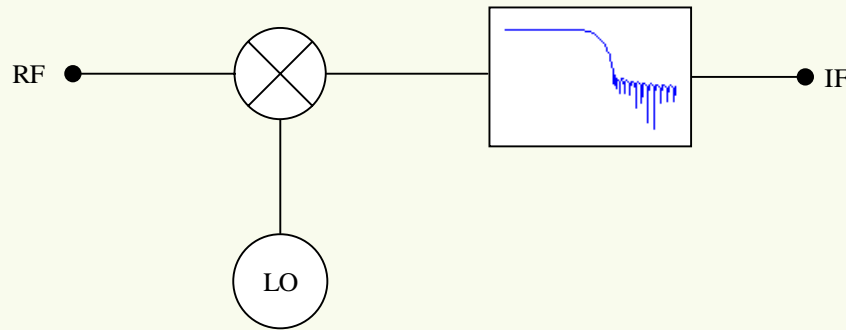
- The purpose of this presentation is to show a novel circuit to perform frequency translation to baseband.
- This task is normally performed with a conventional mixer and a local oscillator.
- The circuit can operate on a GHz RF signal yet no signal in the translation circuit is faster than 30-40 MHz.
- This topology allows standard CMOS process to be used.





Functional Description

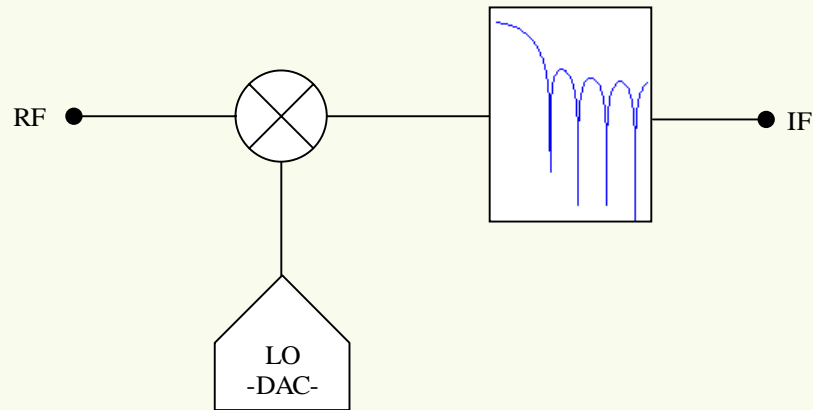
- We start from a well known circuit and progressively change it to get the new circuit:
- The traditional mixer/lo/filter:





Functional Description

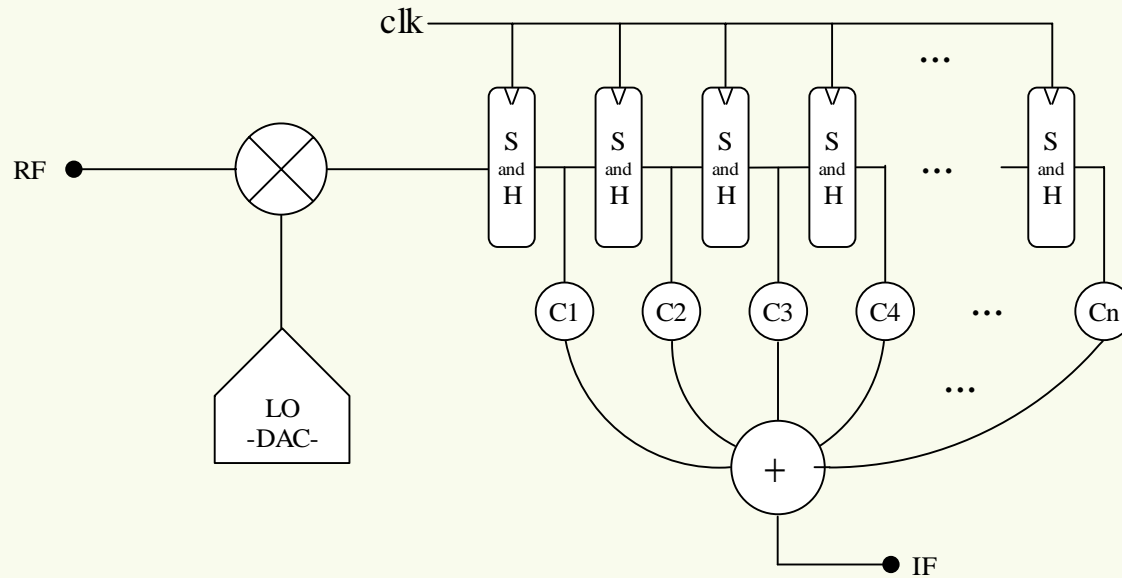
- We change the filter to a $\sin(x)/x$ filter and we replace the real LO with a very high speed DAC. We still have the same functionality.





Functional Description

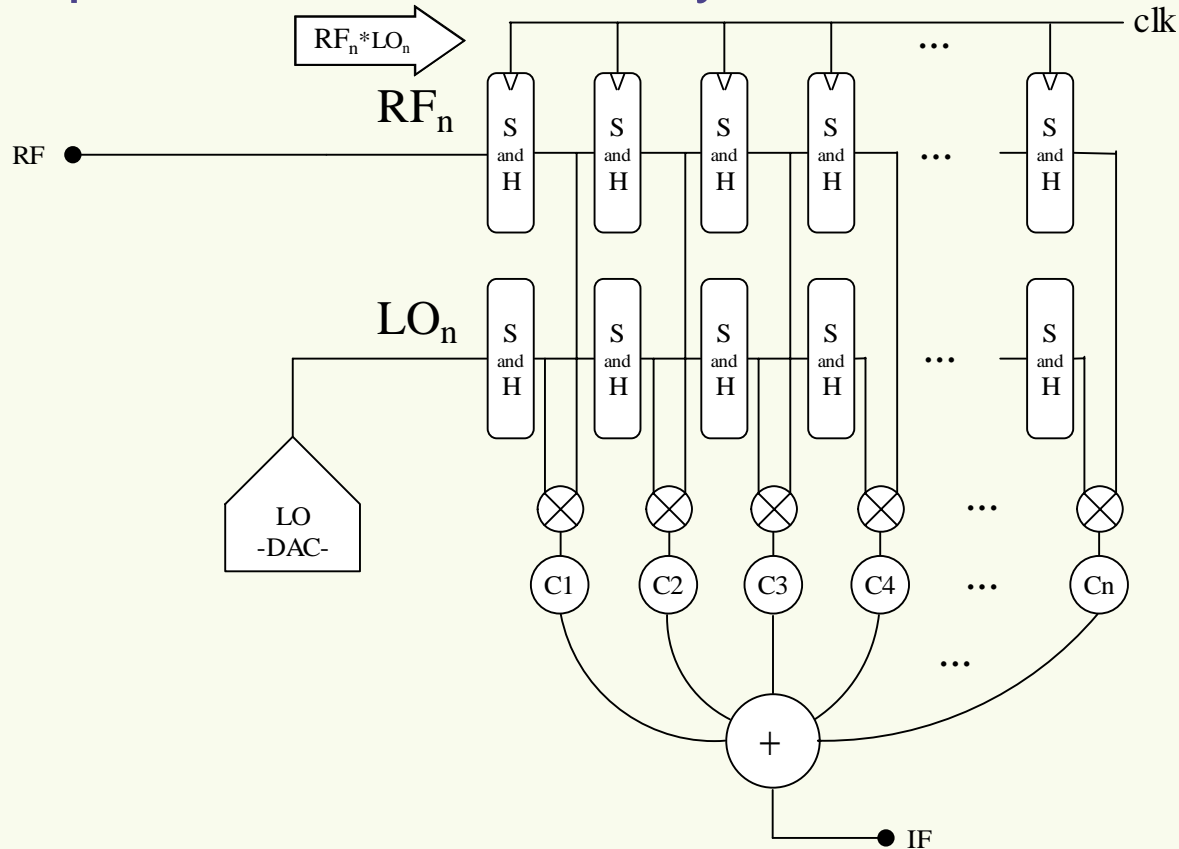
- We implement the filter with a discrete time continuous amplitude filter.





Functional Description

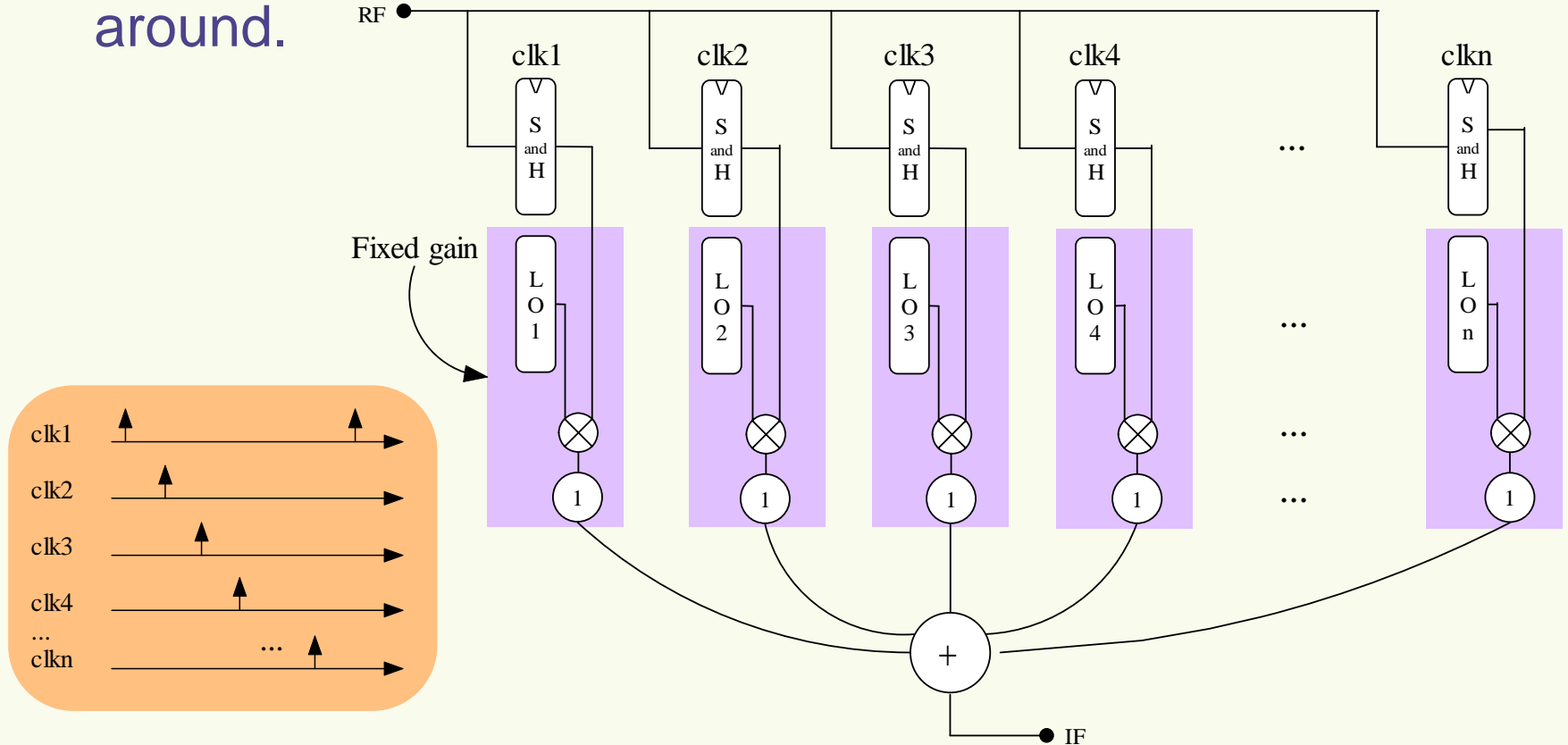
- We can now sample the RF and the LO and move the multiplication after the delay element of the filter.





Functional Description

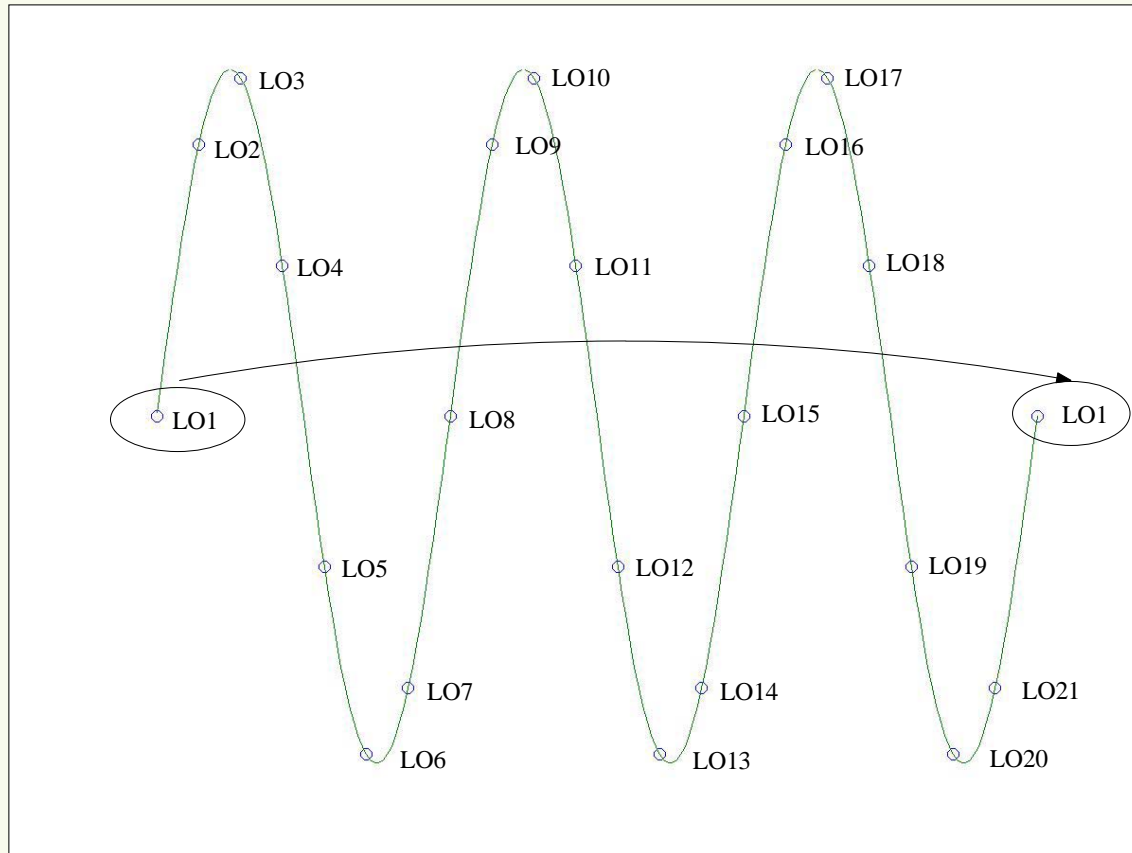
- We can now “freeze” the LO sample and rotate the RF around.





Functional Description

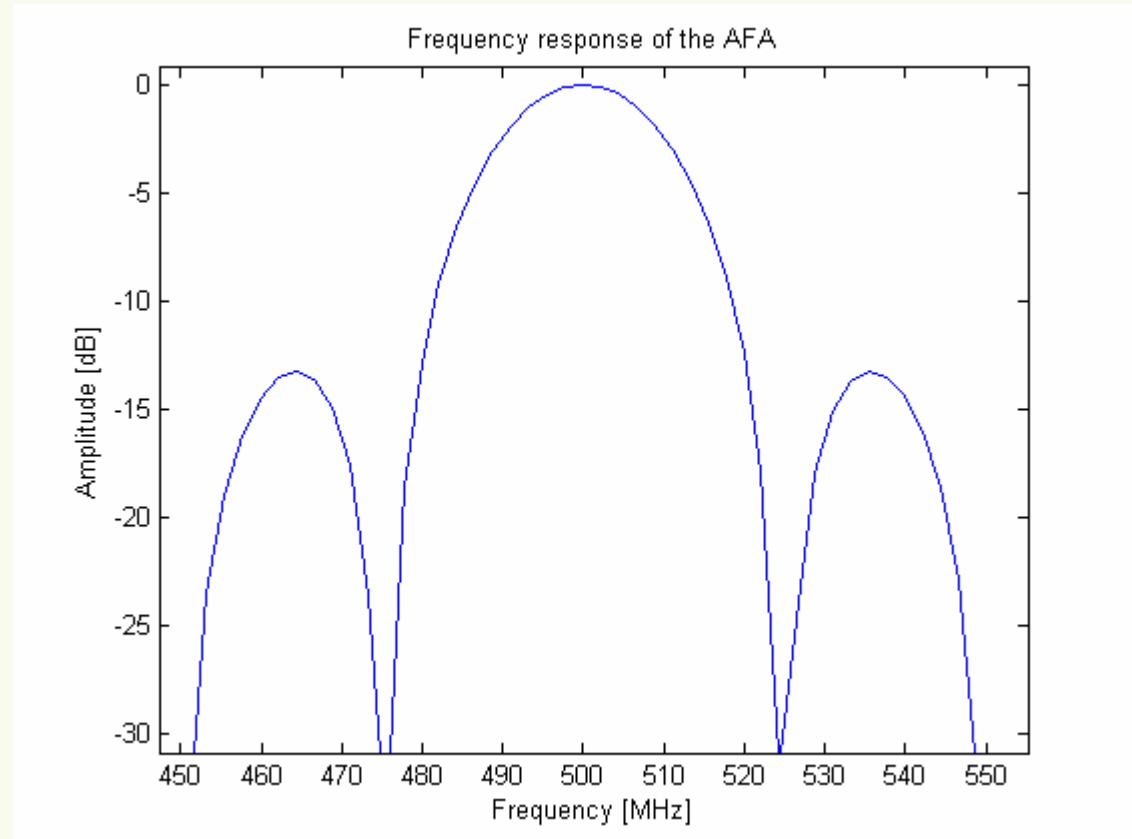
- Virtual local oscillator wrap around in a seamless manner.





Functional Description

- The frequency response is following a $\sin(x)/x$ shape:
- 128 S/H
- 3.2 Gs/s
- $F_c = 500$ MHz





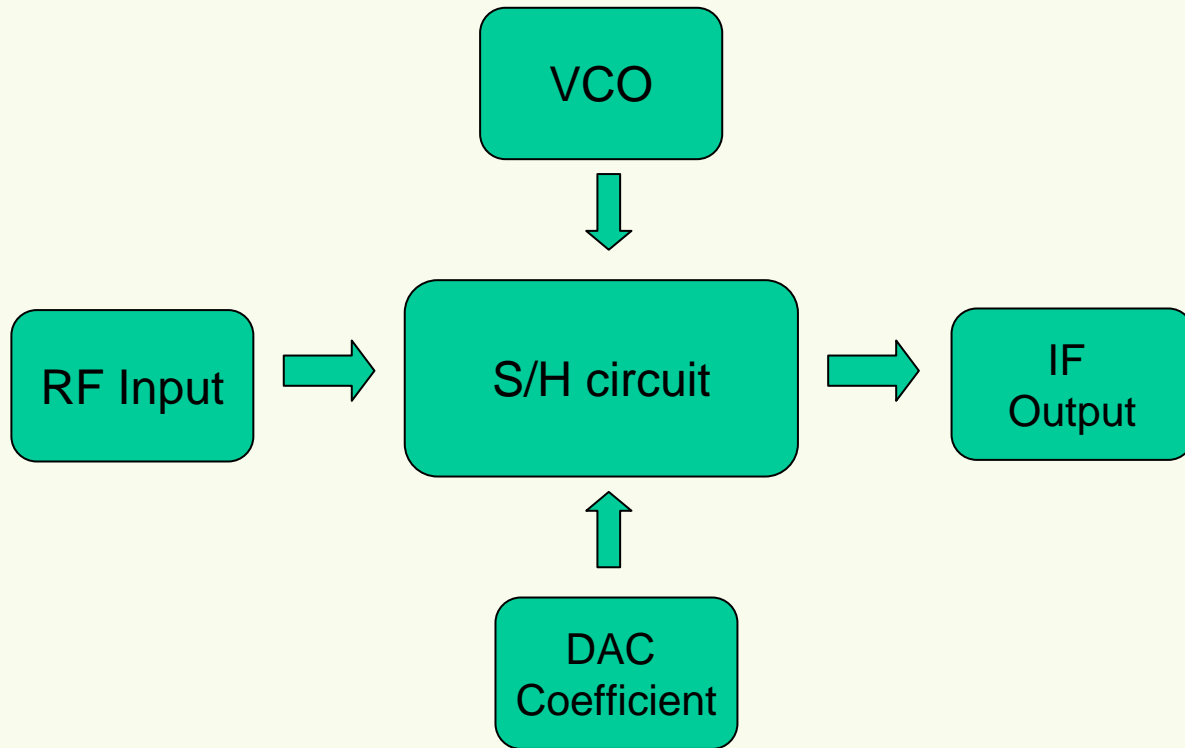
Advantages/constraints

- Advantages:
 - No high Q element required
 - Standard CMOS used
 - All circuits run slow
 - $\text{Sin}(x)/x$ filtering included
 - Topology can retune without a PLL
- Constraints:
 - Low noise ring oscillator required
 - Baseband bandwidth VS sample&hold
 - Nyquist theorem!





A Circuit Level Spice Example



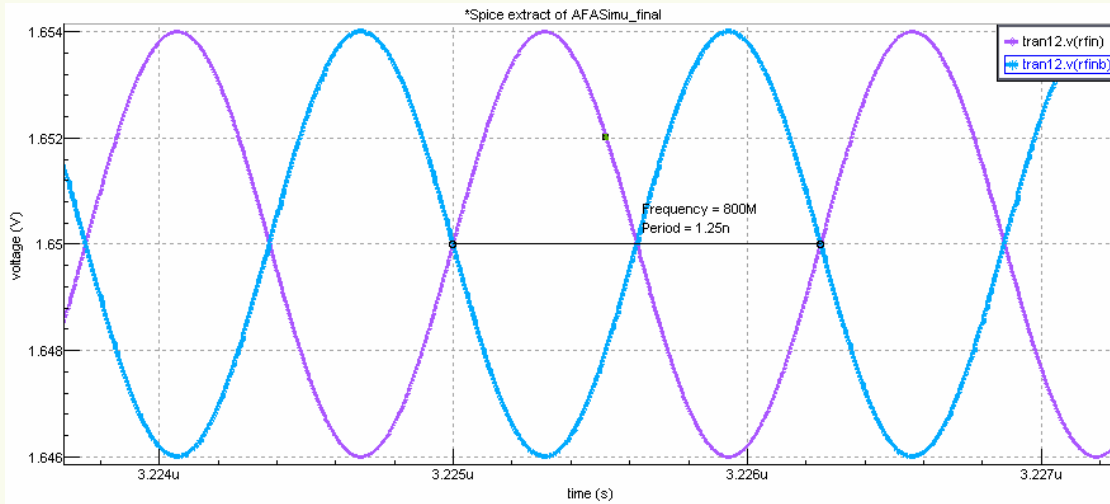


Simulation Parameters 1

Number of Sample and Hold Circuits	128
VCO Frequency	27.658MHz
Equivalent S/H Frequency	3.54GHz
Input Frequency	800MHz
Output Frequency	0.88MHz

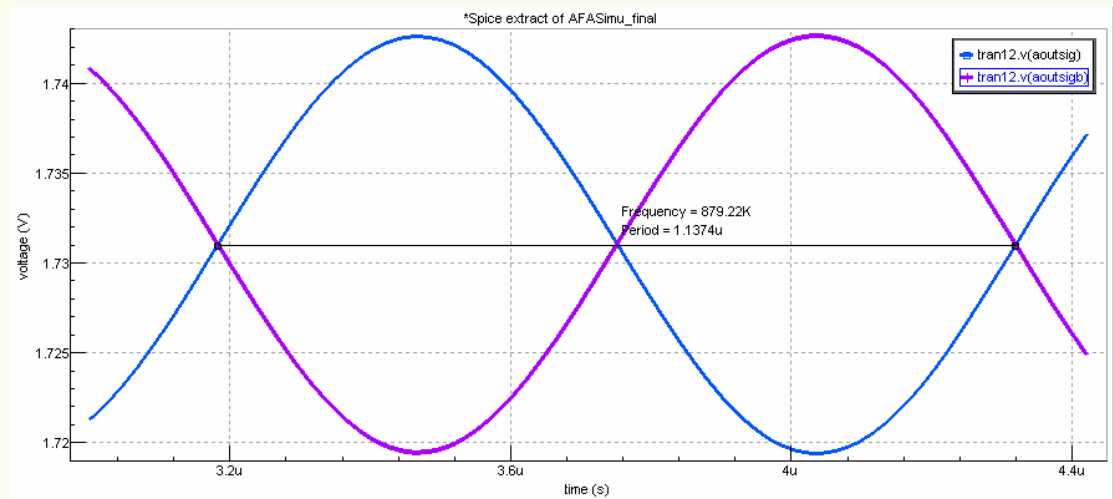


Time Domain Down Converted Signal



Input: 4 mV_p @
800 MHz

Output: 11.5 mV_p @
880 kHz





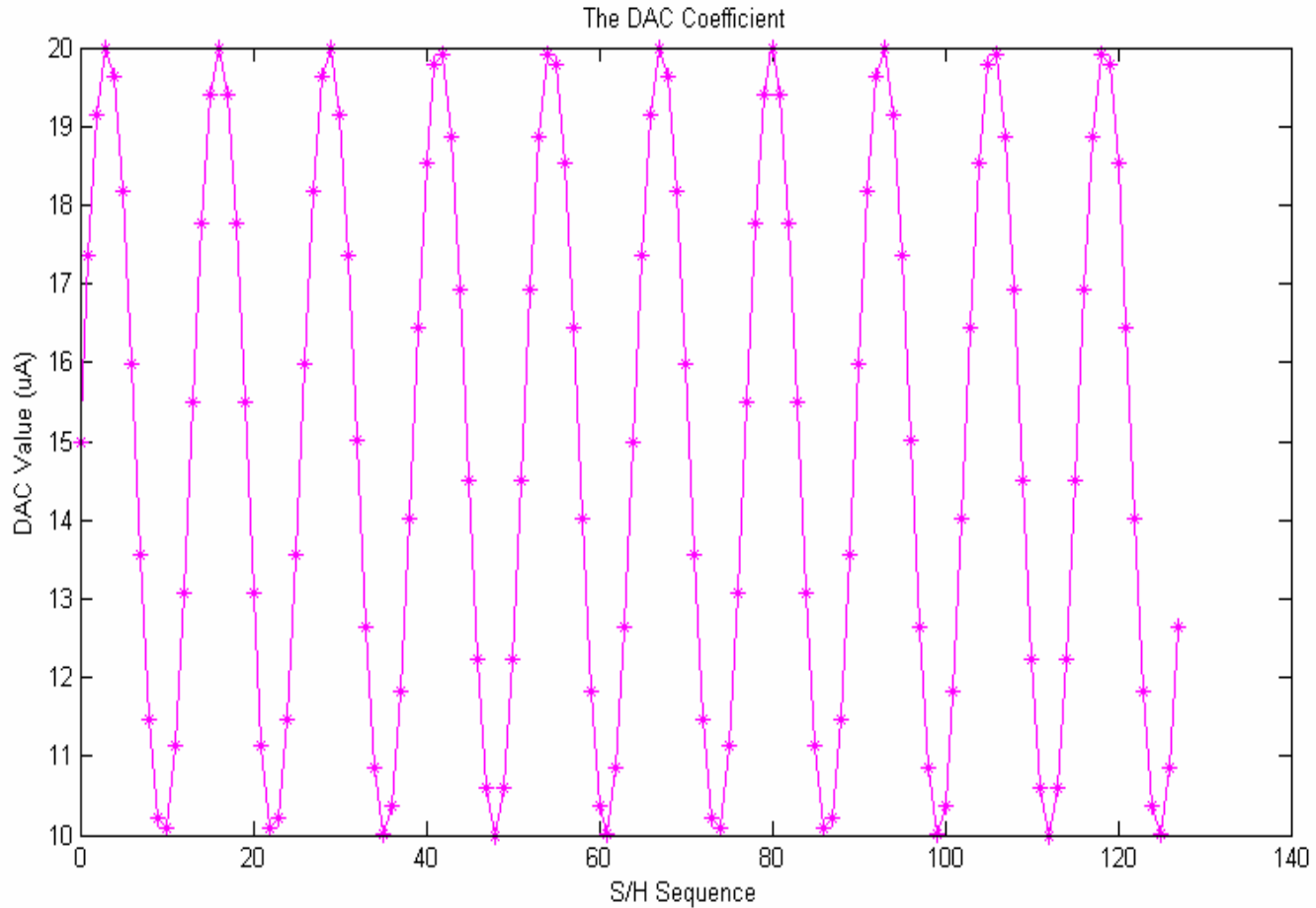
Simulation Parameters 2

Number of Sample and Hold Circuits	128
VCO Frequency	27.658MHz
Equivalent S/H Frequency	3.54GHz
Input Frequencies	264.33MHz ~275.33MHz
Output Frequencies	1MHz~12MHz



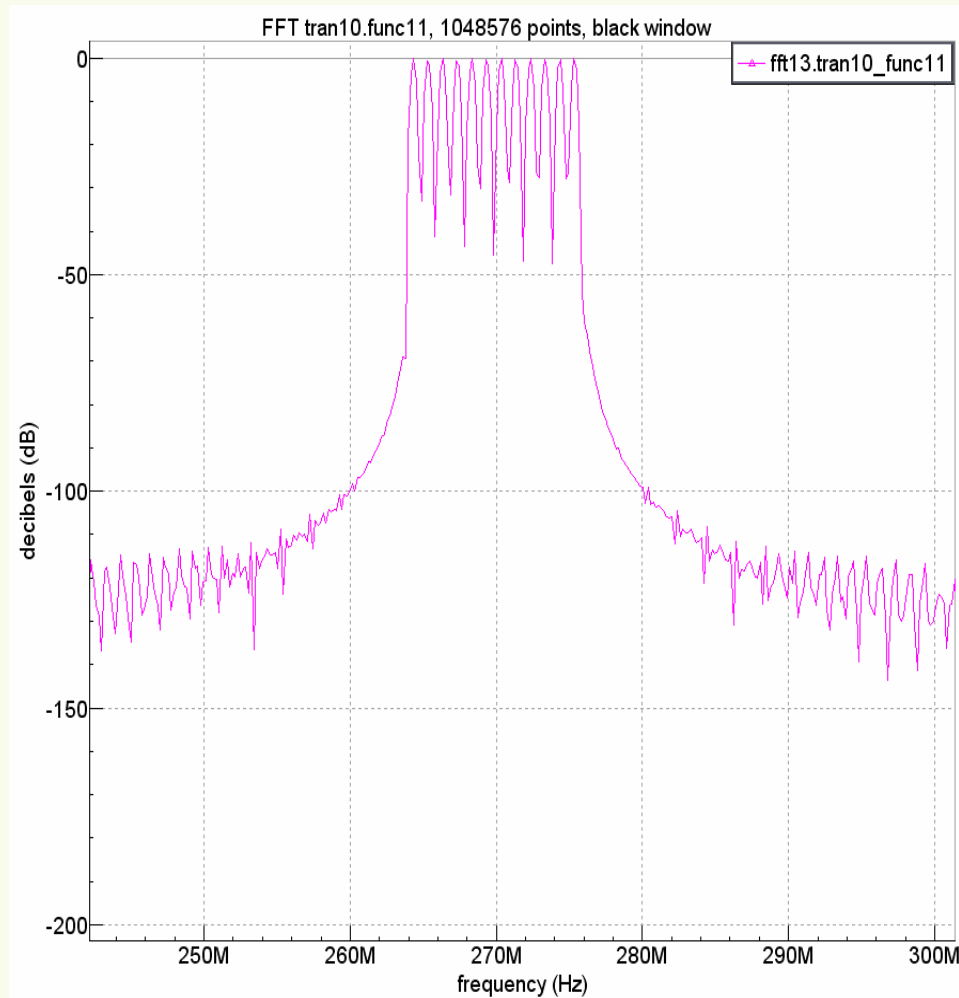


Virtual Oscillator Coefficient Value



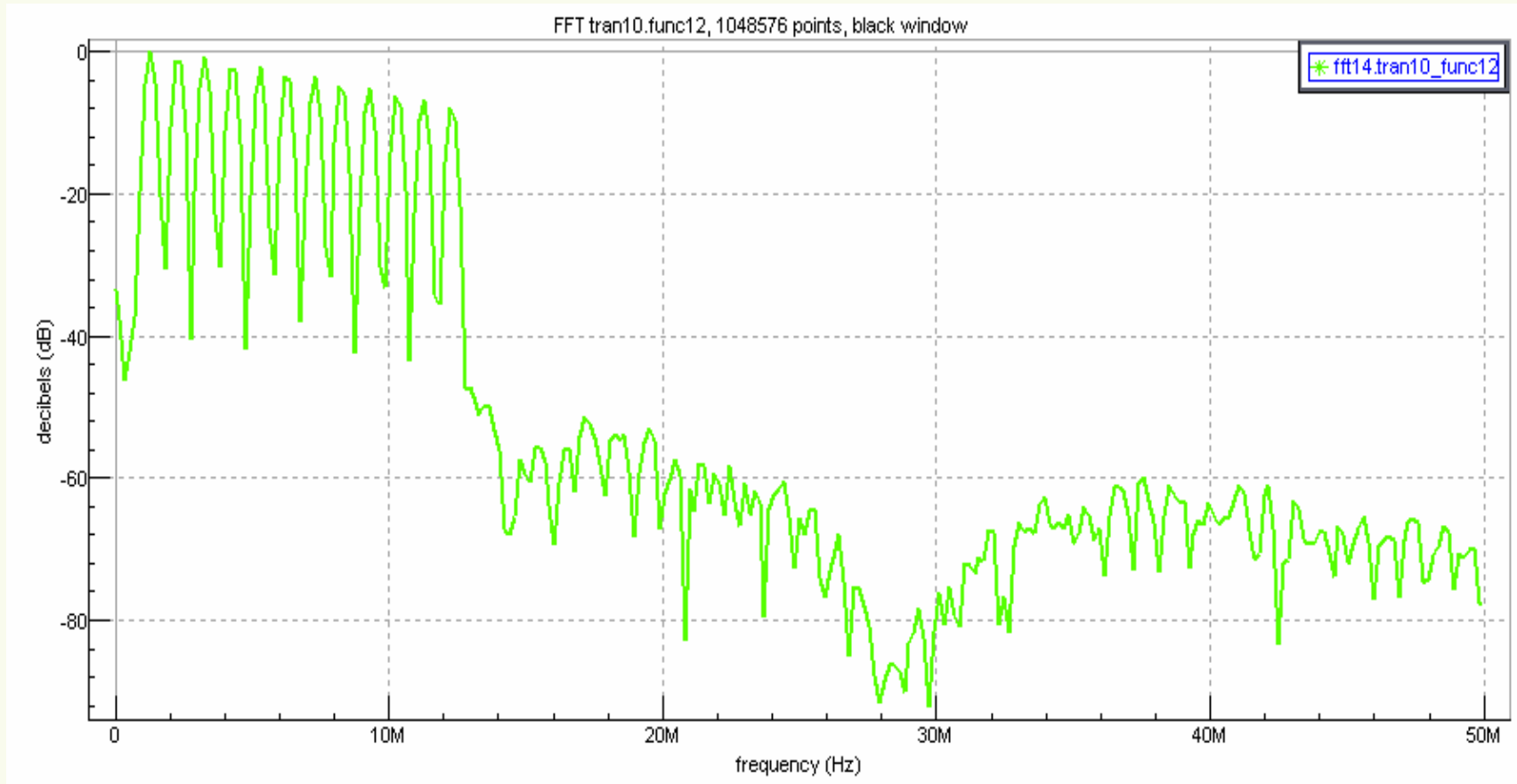


Input Signal and FFT





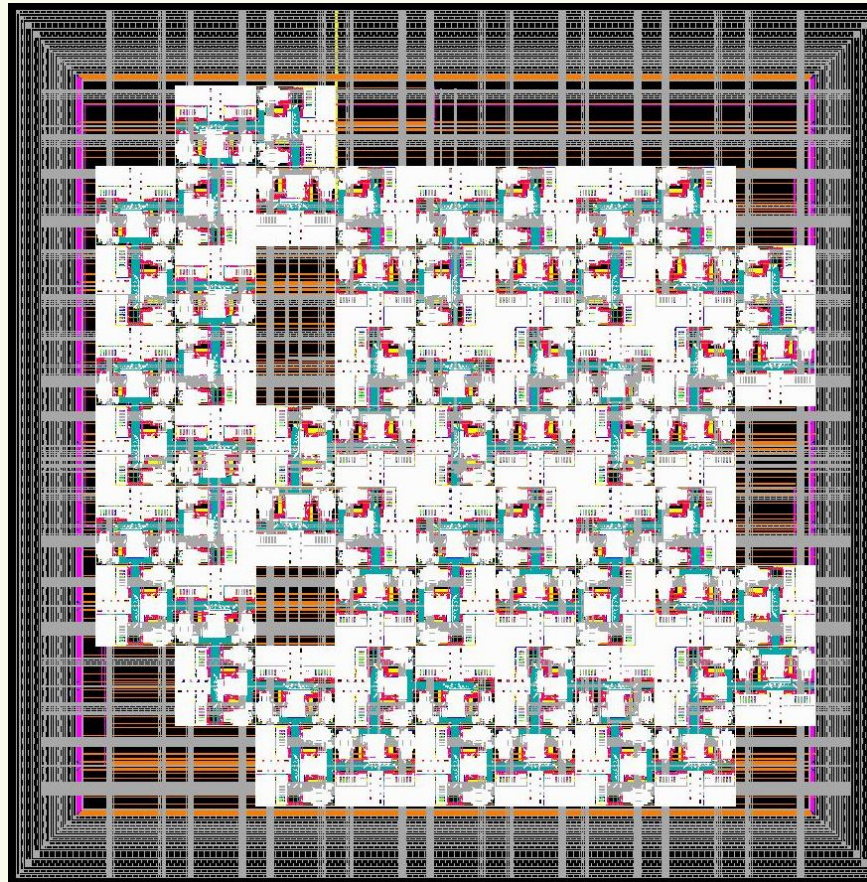
Output Signal and FFT





A Layout Implementation

- Ring oscillator, sample and hold and DAC circuit.





Other Considerations....

- We have analyzed:
 - Noise: corresponds to the noise of a large FET – the noise is low.
 - Input impedance: paradoxically it is high (since the S/H's are loaded with the same signal each time – the input impedance is equivalent that of an LC tuned circuit).
 - We have a breadboard constructed of discrete components and it works.
 - A IC version has gone to a Standard CMOS Digital FAB (July 10th).





Conclusion

- We have a new architecture that will down convert high frequency signals on a standard CMOS process...
- The rate off the circuit corresponds to the bandwidth of the signal – a high GHz carrier of a low bandwidth signal needs components operating only at the signal bandwidth – not the carrier bandwidth.
- The first implementation if targeted for ATSC/DVB-T applications (<800MHz).
- 5.7GHz (high ISM band) operation should also be possible.
- Much more work to do – many steps to a viable product.





Acknowledgements

- The team at ESS Technology Kelowna!

