

Circuit design with FinFET processes

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TEXAS INSTRUMENTS



atdf



Soitec

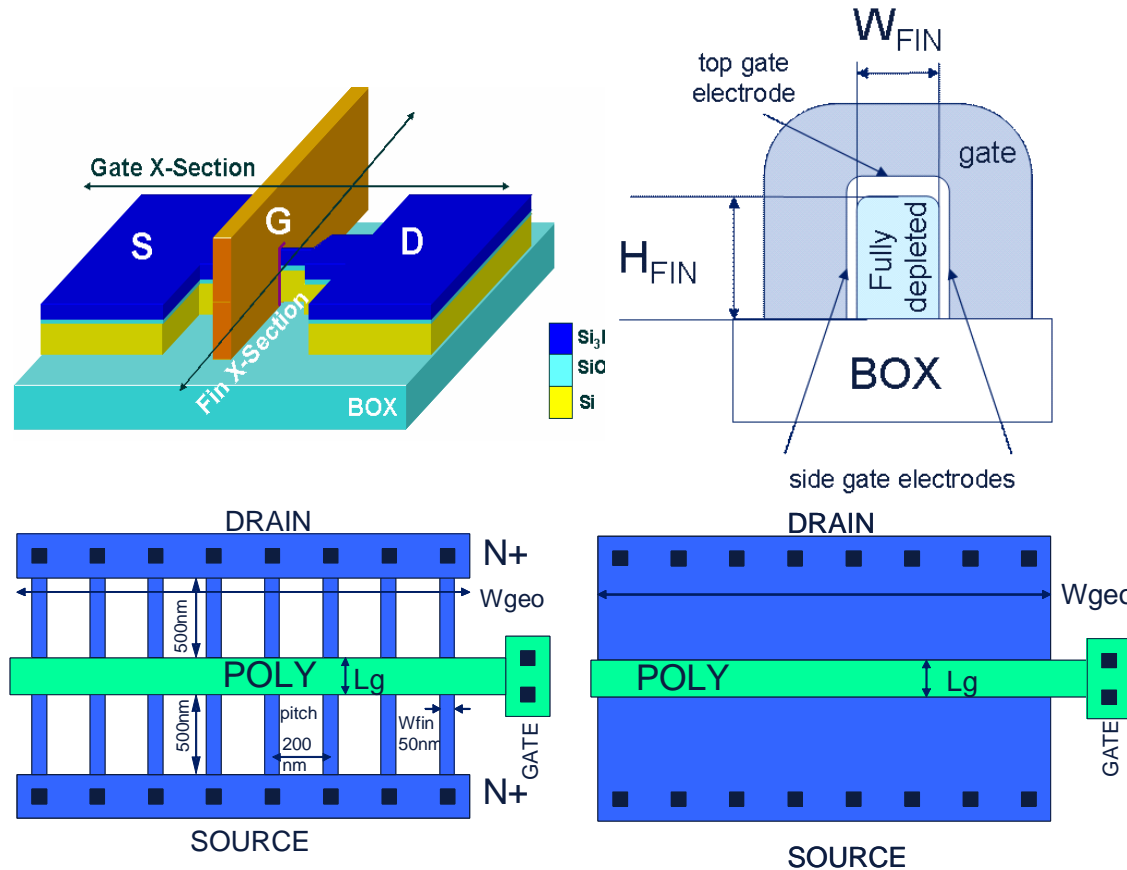
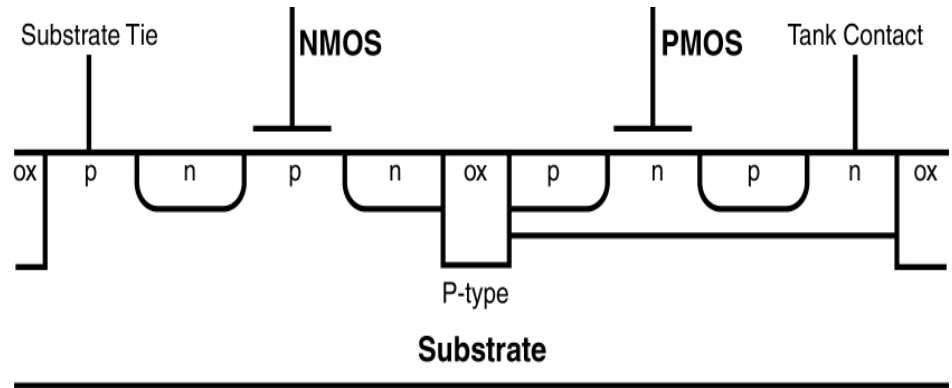
Presentation Overview

Introduction

- Bulk vs FinFET
- Active components
- Passive components

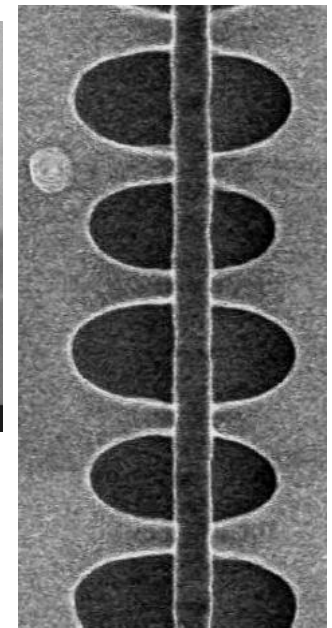
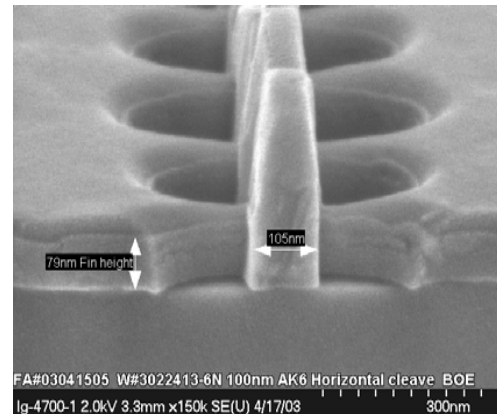
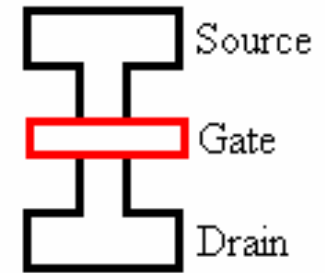
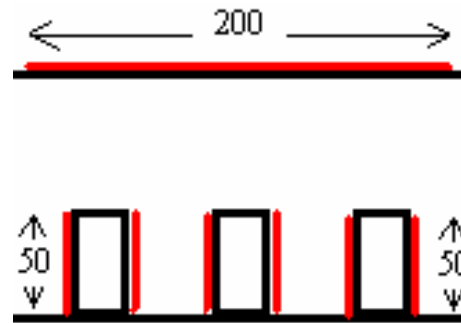
Circuit Techniques

- Digital Circuits
 - Stacked Gates
 - Ring Oscillators
- Analog design using FinFET
 - Current Mirror
 - Operational Amplifier



FinFET Gate Width

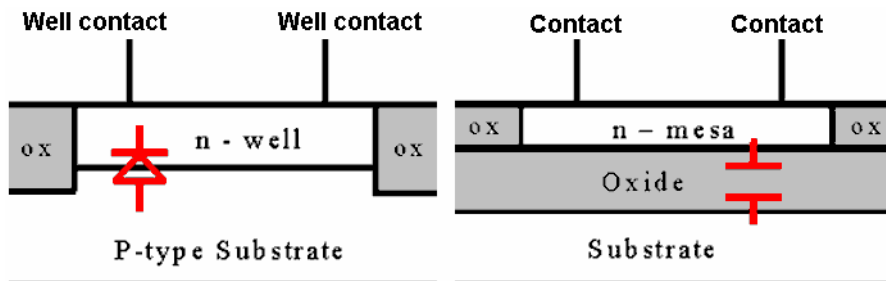
- Sidewalls become active channel width/length vs. planar surface for bulk.
- State of the art fin W is 20-60nm, fin/gate height 50-100nm, gate length \sim 30nm
- larger gate width / unit area
- With Fin height of 50nm, Fin width 20nm, pitch 80nm, 300nm of gate width can be squeezed into 200nm silicon width [1]
- Gate lengths of $<$ 20nm have been generated.
 - Issues S/D resistance / channel modulation
- Multiple fins permit larger widths, but gate width is quantized by fins gate width



Passive Components - Major passives: R's C's, diodes and L's

Resistors in SOI/FinFET - two forms

- Polysilicon - constructed same way on bulk and FinFET but lower substrate cap
- SOI Well resistors are different to their bulk counterparts.
 - In bulk n-type doping into p-type substrate, creates V dependent R/C
 - SOI mesa resistor has no parasitic diode to ground, low capacitance to ground, and R/C variation with respect to voltage is low



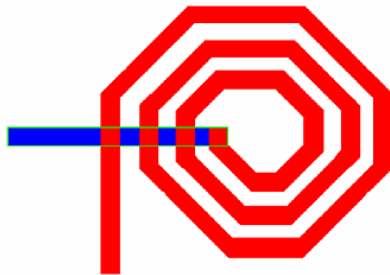
Capacitors

- Well caps not available in FinFET
- Gate caps usually have higher series resistance in SOI due to thinner silicon
 - Inferior resistance but lower parasitic capacitance to ground
 - Minimized with multiple-finger layout
- The metal capacitor is commonly used, formed with multiple interdigitated layers
 - Interdigitated for maximum capacitance
 - Alike in bulk and SOI, but reduced parasitics in SOI

Inductors

Often constructed in the top level of metal

- Since SOI is used for RF circuitry influence of finFET on integrated inductors is important
- The Q-factor of inductors improved on finFET (esp. high res substrates)
- Inductors and transformers are constructed as a spiral using one or more levels of metal

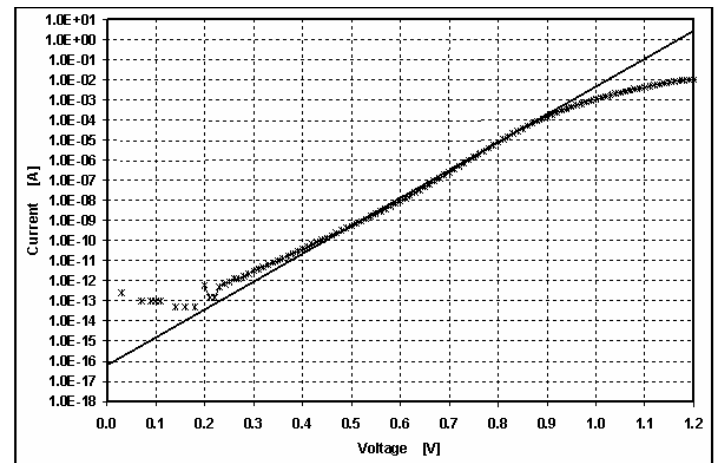
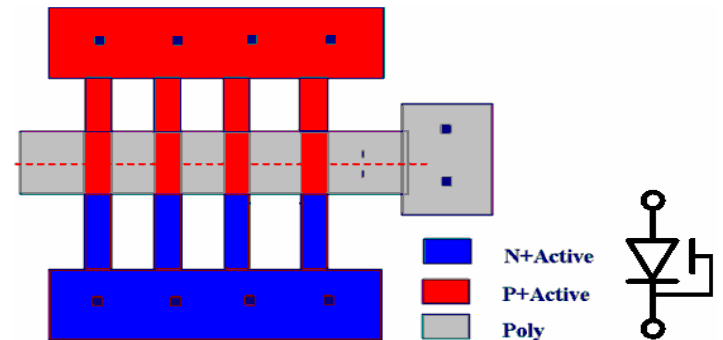


Monolithic inductor layout: Red trace represents one or more metal levels, center tap tunnels under the inductor [2]

Diodes

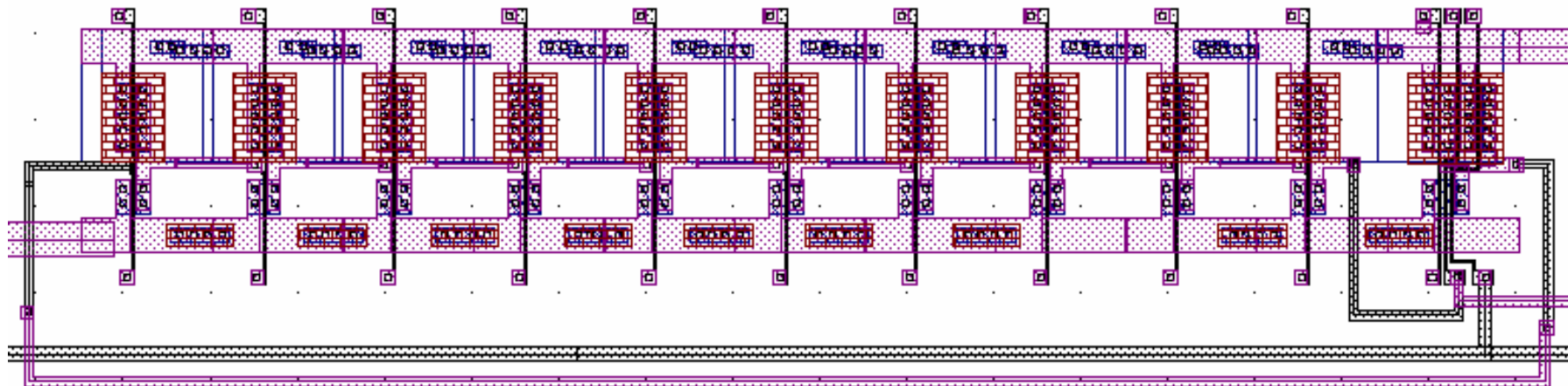
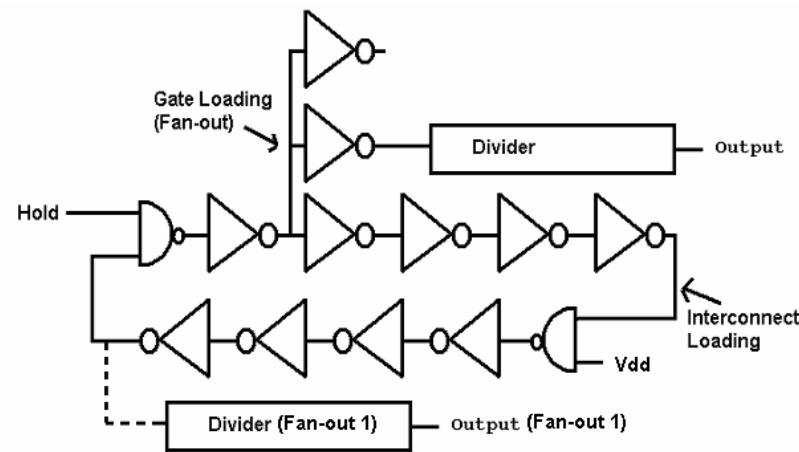
Conventional bulk well diodes are not readily available in FinFET

The Lubistor is a diode based on a MOS device [3]



Ring Oscillator Performance [4]

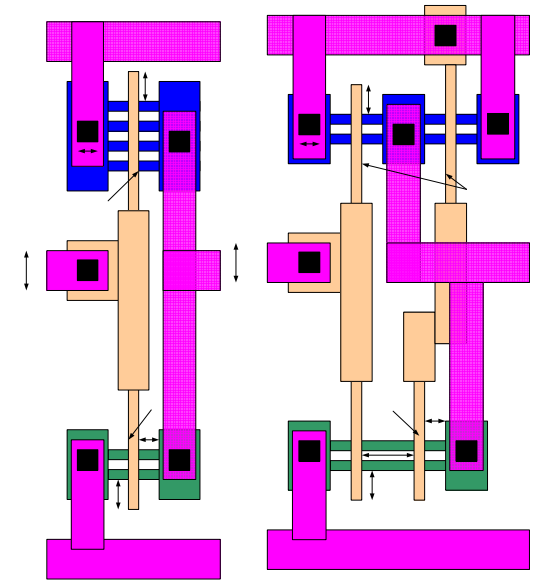
- Ring oscillators have long been used as a guide to process performance
- Fastest ring oscillator is a minimally loaded fan-out of 1 inverter (even these need to take account of minimum interconnect R/C)
- More realistic circuit operation indicators are larger fan-out NAND ROs
- Interconnect loaded ROs good for monitoring capacitive & resistive effects



FinFET Ring Oscillator Circuits Performance

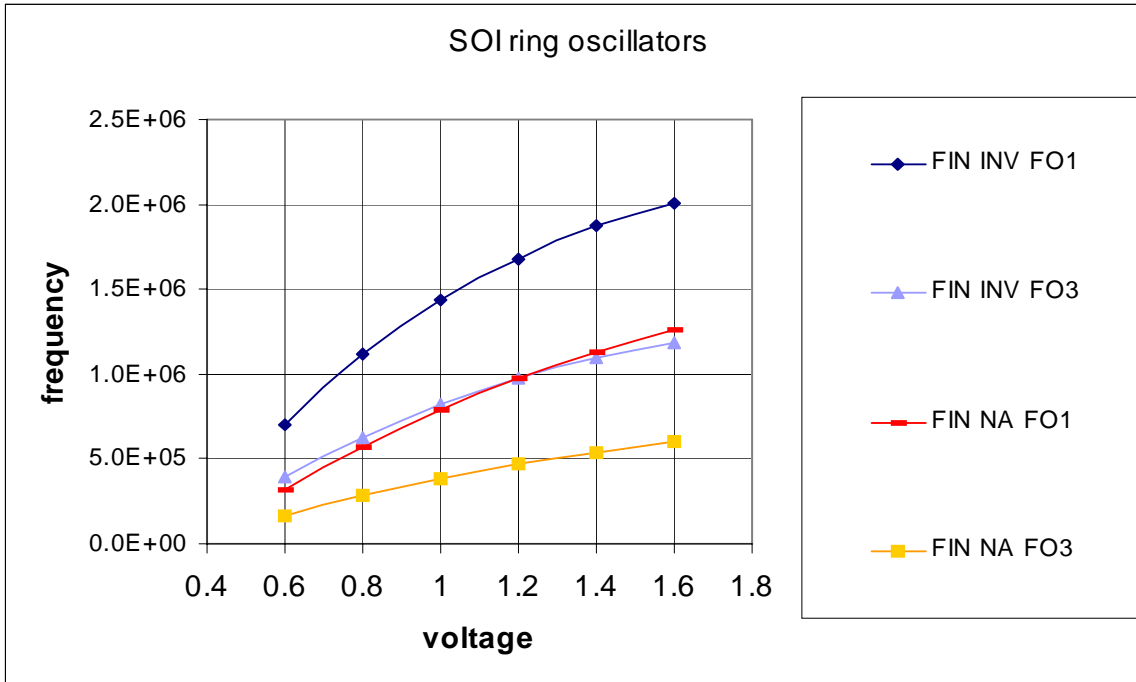
Approx 30 ROs on test chip with:

gate lengths 90-120nm
fin widths from 50 to 80nm
fin height ~ 80nm
fin numbers: 2-12 (NMOS) 2-18 (PMOS)
Invertor, Nand, Nor



INV1

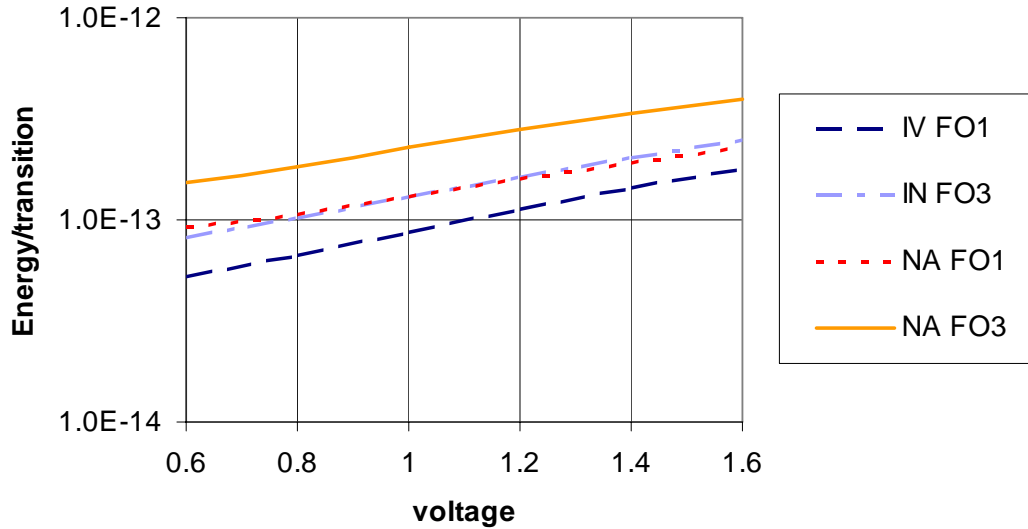
NAND2



Inv/Nand freq vs supply

-Operate from <0.6v to >1.6v

Gate energy



Energy per transition – includes switching and shoot-through

FO1 ~ 100fJ, FO3 ~ 150fJ

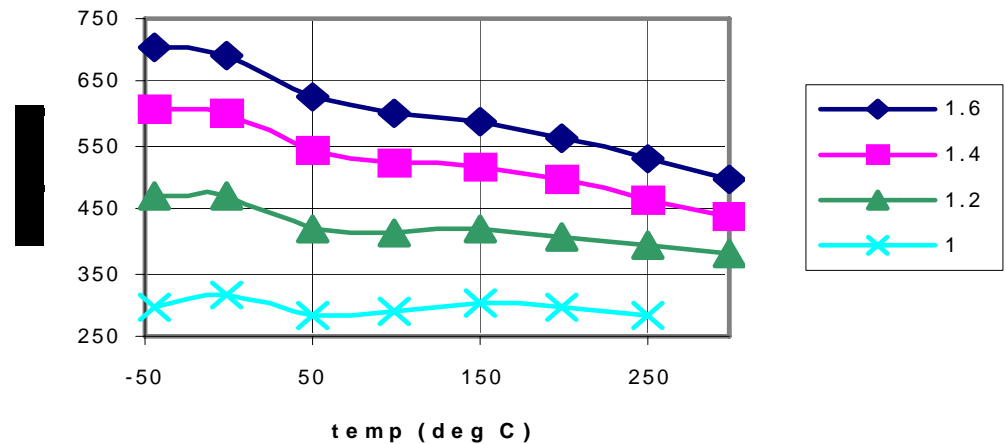
FO1 Nand / FO3 INV similar

RO Performance over Temperature

Performance gradually reduces with temperature due to mobility, except low temps, where V_t reduction offsets degradation

Operation to 300°C

RO performance



Analog Circuit Design - Overview

- Analog design requires consideration of:
 - Threshold voltage mismatch – due to different topography
 - Thermal management - due to Oxide thermal isolation
 - Power consumption
- Slow development of analog CAD tools for SOI applications has contributed to the slow acceptance of SOI for analog circuitry

Advantages of FinFET for Analog

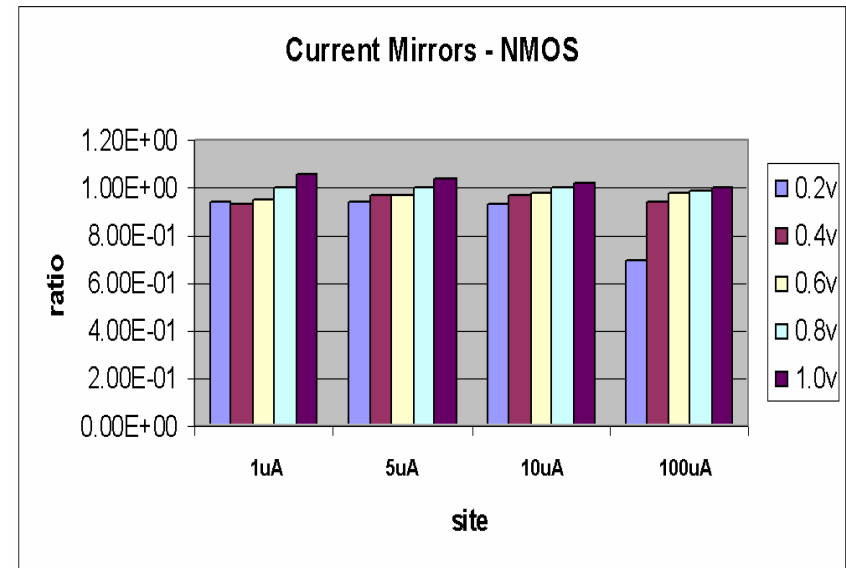
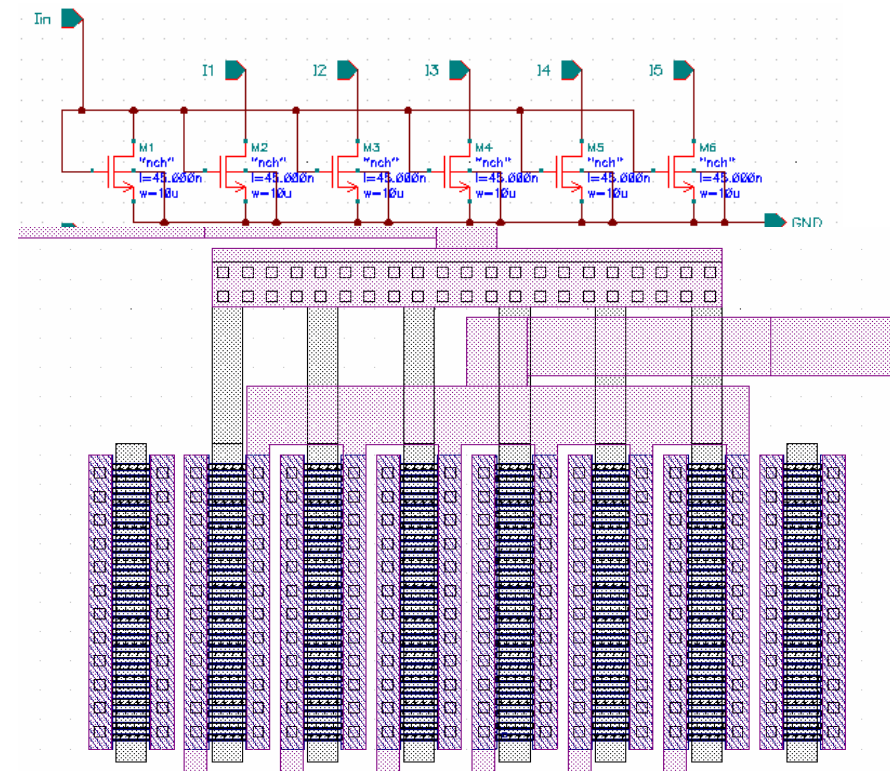
- Improved frequency performance
- Reduced capacitance
- Higher drive current
- Reduction in interconnect length / reduced interconnect capacitance
- Noise and latchup are minimized through reduced substrate coupling
- Silicon resistors have improved linearity with respect to absolute voltage
- No reverse biased diodes to substrate
- Inductor Q enhanced through use of very high resistivity substrates

Drawbacks to FinFET for Analog

- Poor thermal response due to buried oxide and trench isolation.
- Quantized widths

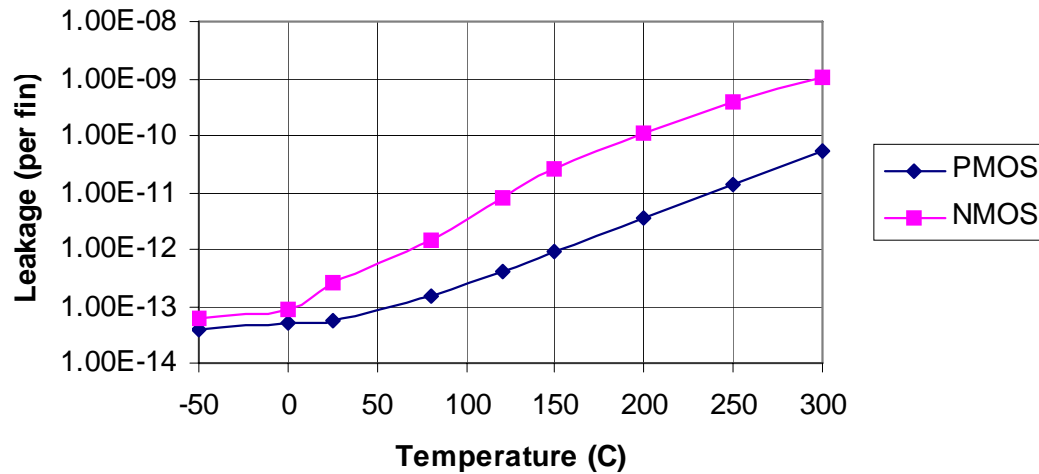
Current Mirrors

- NMOS and PMOS mirrors,
 - Input and 5 adjacent outputs
 - Lengths 1 μ m, 5 μ m
- Matching and leakage, in sat, lin and intermediate states
- Poly and Metal gates
- Analysis over temperature
- Good matching (better than 2.5%) for most of current range
- Matching retained over supply voltages, except for higher currents
- Similar performance from NMOS and PMOS, though PMOS leakier

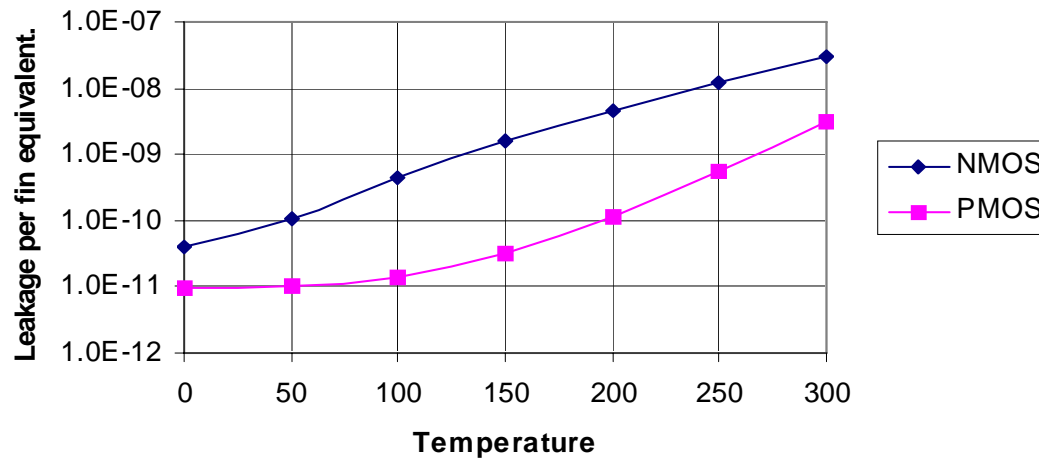


NMOS & PMOS fin and planar leakage as a function of temperature

MUGFET leakage



Planar Leakage



Fin

- leakage increase ~ 10x/100deg

- leakage/fin

NMOS 1nA/fin @ 300 degC

PMOS 80pA/fin @ 300 deg

- Ion/Ioff ratio better than 6000

Bulk Planar

- leakage increase ~ 10x/100deg

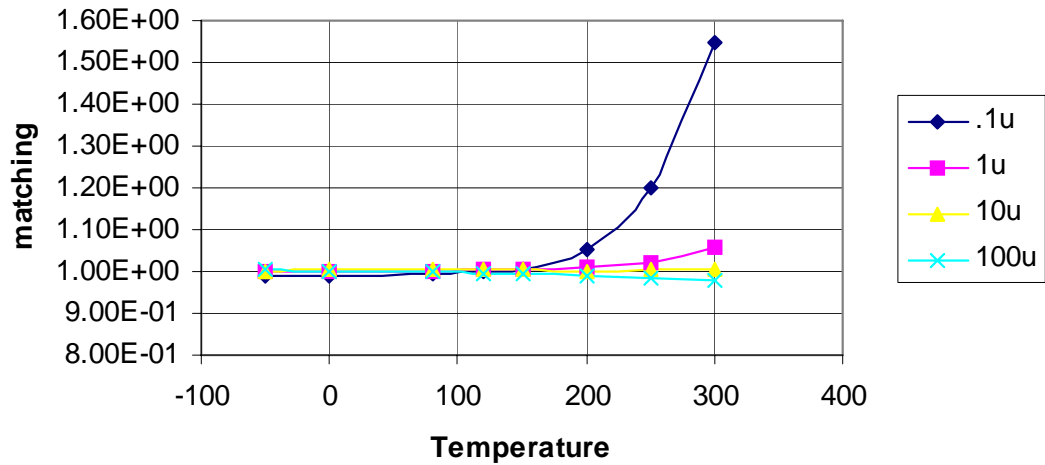
- leakage/fin equivalent

NMOS 30nA/fin @ 300 degC

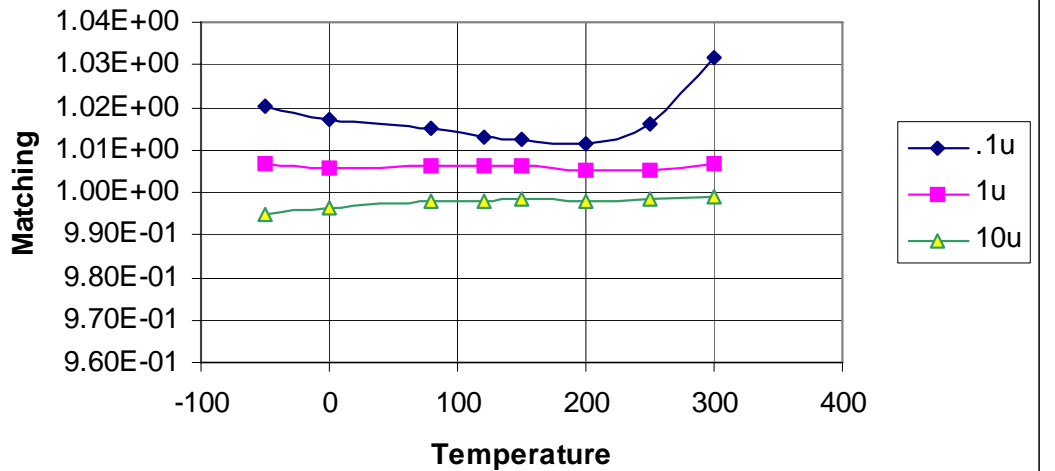
PMOS 4nA/fin @ 300 deg

- Ion/Ioff ratio about 220

NMOS - normalized matching



PMOS - normalized matching



Mirror-Matching

- Matching is better than 3% over all conditions of bias and temperatures, except for the following conditions:

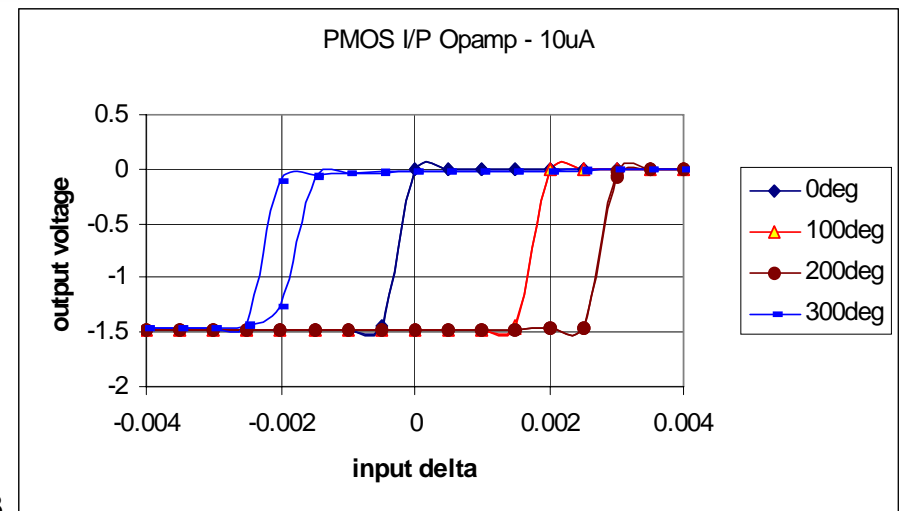
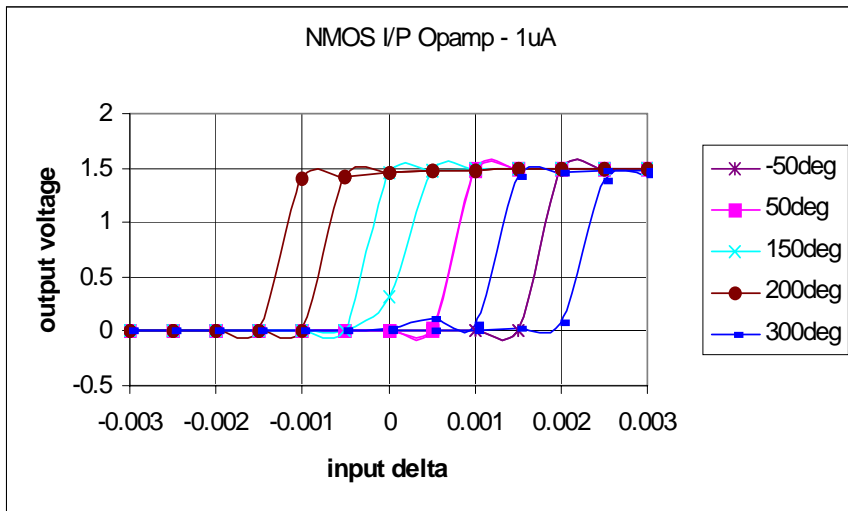
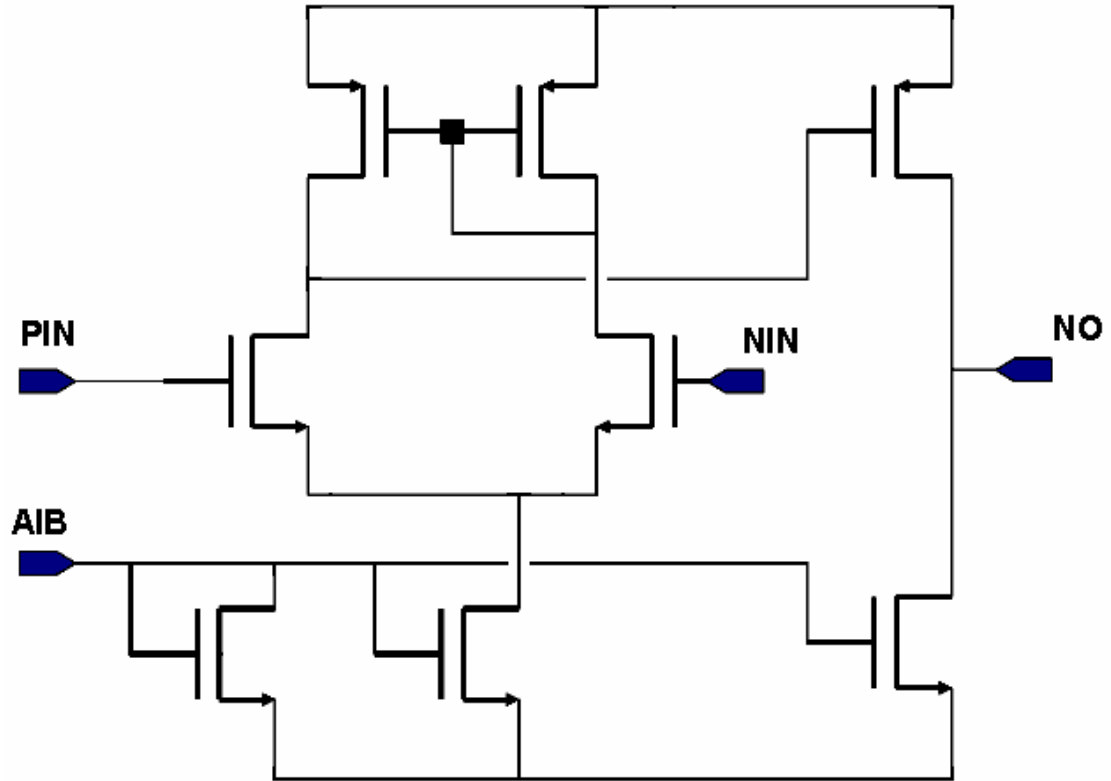
- At very low currents NMOS and to a lesser extent PMOS mirroring is affected by leakage at high temperatures.

- Easily fixed with scaling or low leakage transistor options

- PMOS shows similar trends, but with less mismatch, due to lower baseline PMOS leakage in this FinFET material

Opamps [5]

- NMOS and PMOS
- operation -50 to 300 C
- input offset better than 2mV
- open loop gain > 3000
- hysteresis < 0.5mV (except 300 degrees = 0.5mV)
- output switching 0-100%
- I/P current 1uA-30uA



Advantages of FinFET over Bulk

- Reduced D/S cap (oxide isolation vs junction isolation) – Lower power
- No MOS “reverse body effect” in stacked transistor devices
- Improved latchup, noise and current immunity through the substrate
- Simpler high V component design
- Improved high temp performance (lower device and parasitic leakage)
- Improved passive components – Inductor Q, parasitic capacitance
- Reduced capacitance from substrate to metal interconnect (reduced power)
- Fewer process steps (Pwell / NBL)
- SOC, High Perf, RF, High Freq, Low Leakage, Low Power, High Temp, Smaller area
- Adds extra dimension (height) for additional gate width

Disadvantages of finFET v Bulk

- Self heating, dissipation problems
- Reduced Vdd-GND capacitance for noise reduction on supply rail
- Start-up cost,
 - Engineering & Management Pushback,
 - Extra Design time
 - limited knowledgebase
- Quantization of width
- Substrate cost

Why consider FinFET?

- Scaling trends
 - Bulk requires increase in doping level with scaling, adversely affecting carrier mobility and junction capacitance.
 - May limit scaling to 25-35nm gate lengths
 - FinFET Scaling limits at least a generation beyond bulk

Summary

Ring Oscillators:

- Demonstrated Inverter and NAND FinFET ring oscillators of various fan-outs:
 - Gate delay of 25ps for Inv F01 at $V_{dd}=1.2V$
 - Performance from -50 to 300 C

Current Mirrors:

- Demonstration of current mirrors of 1-5um
 - Systematic matching approx 2.5% or better for 1um ring
 - Poly and Metal gate structures have similar performance
 - Performance from -50 to 300 C

Op Amps:

- Demonstration of NMOS/PMOS op amps
 - DC large signal performance from -50 to 300 degrees C
 - In line with or better than equivalent bulk op amps

References

- (1) X. Huang, et-al, "Sub-50nm FinFET:PMOS," IEDM Tech Digest, Dec 1999
- (2) A. Marshall & S. Natarajan, "SOI Design: Analog, Memory and Digital Techniques", Springer, ISBN 0-7923-7640-4
- (3) M-D Ker etal, "Novel Diode Structures and ESD Protection Circuits in a 1.8v 0.15um Partially Depleted SOI Salicided CMOS Process", Proc. 8th IPFA 2001, Singapore, pp91-96
- (4) N. Collaert et-al, "A Functional 41-Stage Ring Oscillator Using Scaled FinFET Devuces Wlth 25-nm Gate Lengths and 10-nm Fin Widths Applicable for the 45-nm CMOS Node", IEEE Electron Device Letters, Vol 25, No 8, August 2004, p568-570
- (5) G. Knoblinger et.al., "Design and Evaluation of Basic Analog Circuit in an Emerging MuGFET Technology", IEEE SOI Conference, Oct 4-6, 2005