

# Embedded Memories: Trends, Challenges & Roadmaps

Sreedhar Natarajan  
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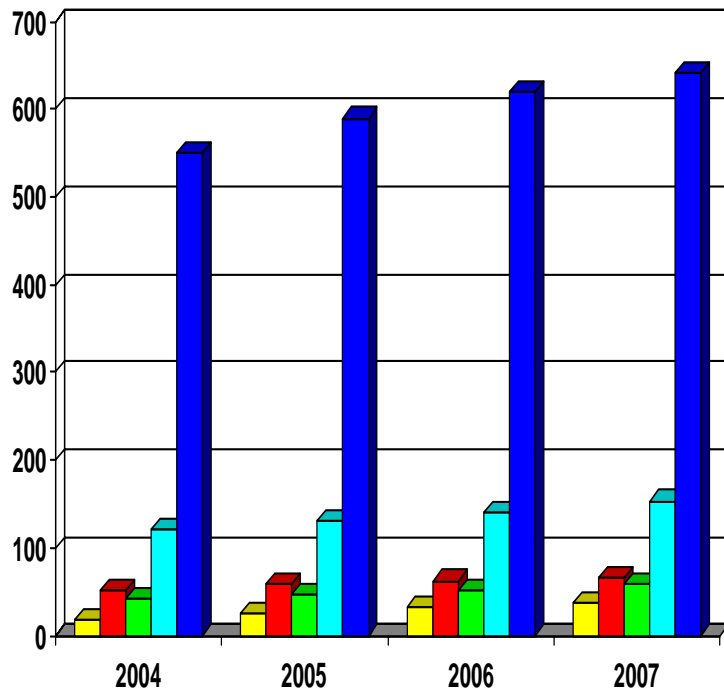
# Agenda

- Recent Trends and Market Evolution
- SRAM Factoids
- DRAM Inheritance
- Flash Dominance
- Conclusion
  - What's Next
  - Next Generation Challenges

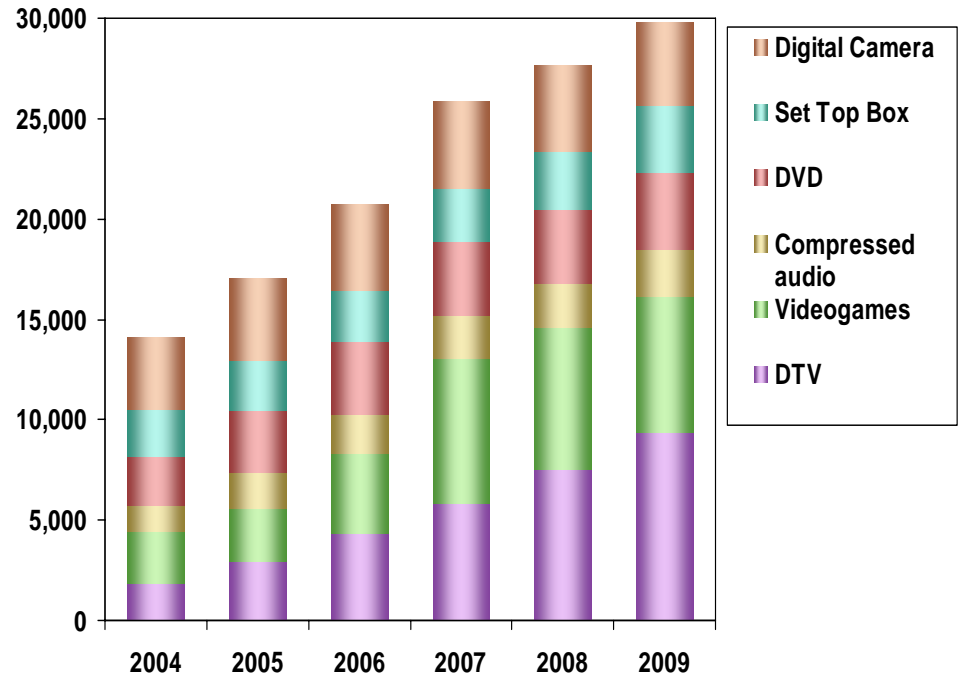
# Recent Trends

- Many applications motivated by Images
- Consumer products drive 50% of chip market and dominate growth
- Everything going digital, but everything digital needs analog
- Power has become key hurdle
- Integration should be to reduce cost

# Consumer Market

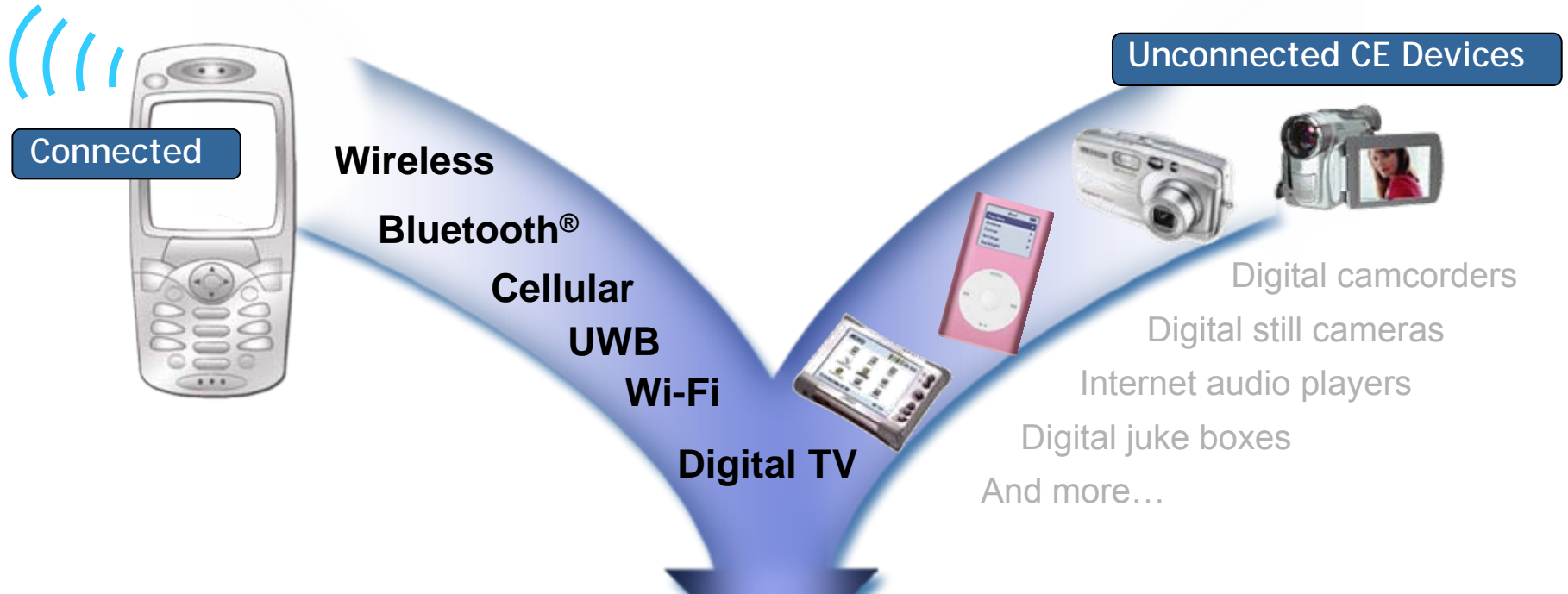


- Portable audio
- Notebook PC
- Cell Phone
- Digital Still Camera
- Desktop PC



# Wireless and Consumer Electronics are Key Growth Markets with Huge Opportunity

## COST IS KEY - \$\$\$\$\$



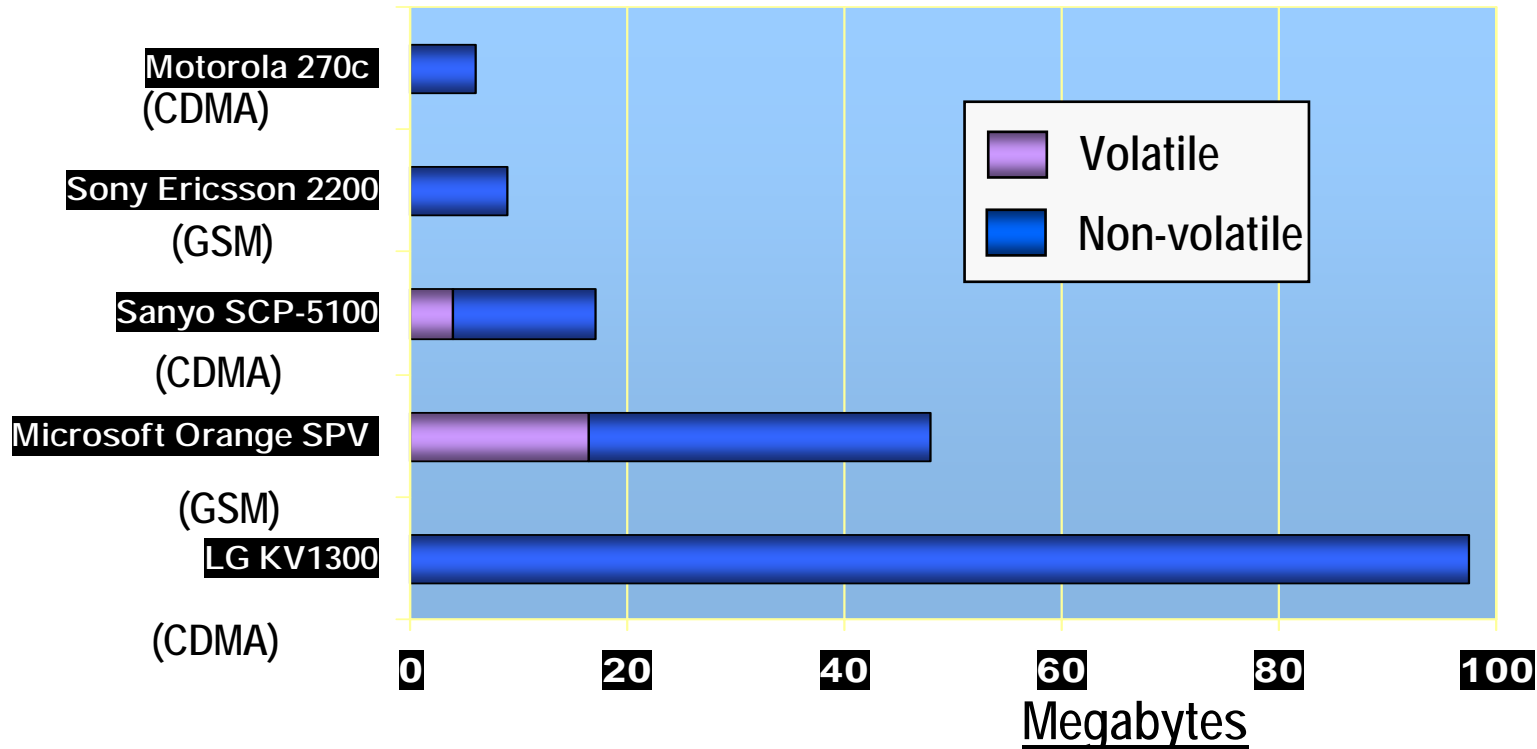
**Note: Cost SOI wafer = 3-5X cost of bulk wafer**

# Wireless Market Evolution

- **1G** – *Analog Cellular* (Voice, AMTS, TACS)
- **2G** – *Digital Cellular*
  - Voice, Pager, 10kbps data, GSM, TDMA, CDMAone
- **2.5/2.7G**- *Digital Cellular*
  - Voice, Email, Photos, Web(100Kbps), GPRS, CDMA 2000 1X
- **3G** – *Wideband Digital Cellular*
  - Video, M-pixel Camera, 3D, 300kpbs (14Mbps), UMTS, WCDMA, HSDPA, CDMA 1X EVDO
- **3.9G/OFDM** – *WDC*
  - Video, Highend Gaming, 100Mbps, Flexible bandwidth, Super 3G, HSOPA, MC-CDMA
- **4G** – *Wideband Network*
  - Ubiquitous Data, Flexible Spectrum Use, Enhanced apps, 100Mbps – 1Gbps

# System Memory Requirement is Exploding

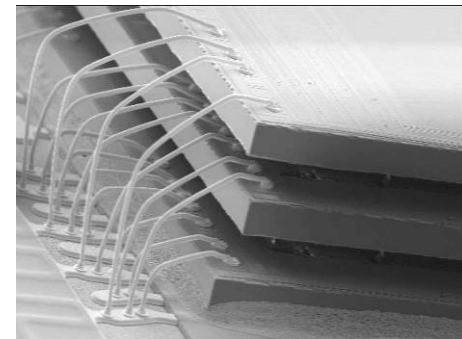
Solution must harness commodity memory cent/bit curve



- Average system memory in 2G cellphone is 10MB or 80Mb!! In 2.5G/3G this is exploding to 20-40MB!! Same is true for many other applications..
- This has spawned the SiP (stacked die or stacked package PoP) as a solution that meets BOM cost, time to market, footprint and flexibility goals of these applications.

July 20, 2006

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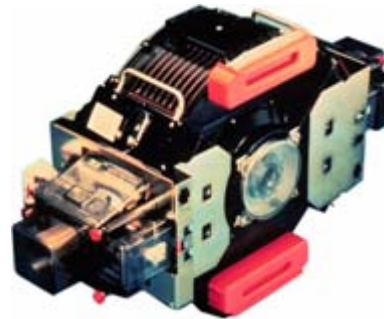
# Hard Disk Drives – Then and Now

1956 – RAMAC  
2 kbits/in<sup>2</sup>



5 MB, 70 kb/s  
50 x 24" dia disks

1981 – "3380"  
12 Mbits/in<sup>2</sup>

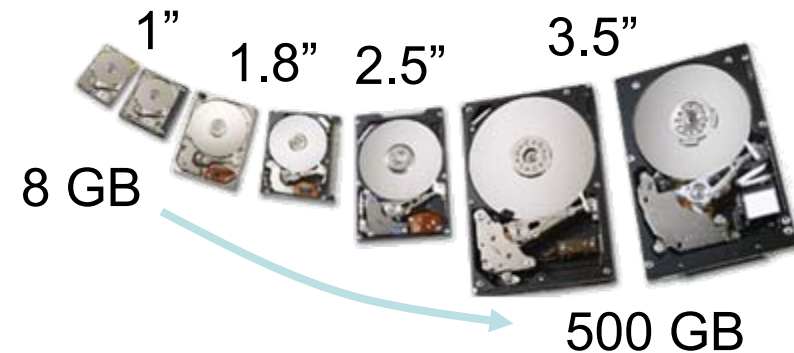


1.2 GB  
9 x 14" dia disks

2005 Microdrive  
105 Gbits/in<sup>2</sup>



8 GB, 130 Mb/s  
1 x 1" dia disk

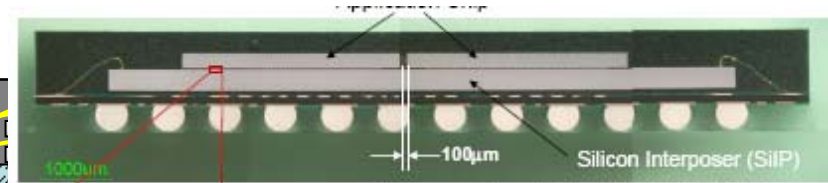
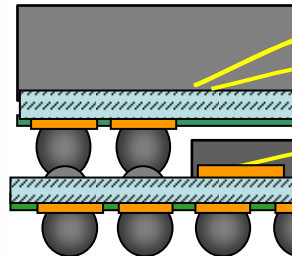
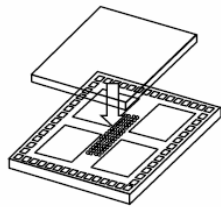


# Future of Memory is Embedded in Packages (The eDRAM and eNVM killer)

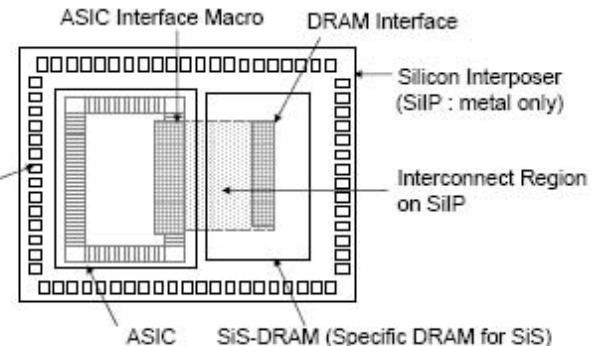
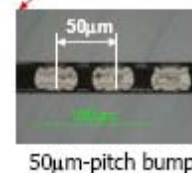
## SiP & PoP Options & SiS & ???

- 1<sup>st</sup> Gen:** Stacked Die Packages (SiP): Die are stacked on top of each other, allows mixing of wafer process technologies in small area.
- 2<sup>nd</sup> Gen:** Stacked Package on Package (PoP): Pre-packaged devices are stacked on top of each other (leadframe, PCB, flex-based, etc.), avoids multi-die package yield issues.
- 3<sup>rd</sup> Gen:** System-in-Silicon, Microbump, face to face solutions, etc.

Chip layout



Cross-section SEM of the TEST CHIP



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# Stacked package challenges

- Direct chip attach
  - Must underfill large dice
  - Ball reliability influenced by PCB geometry and metallurgy
- Stacked Packages
  - Packaged from multiple companies – multiple reliability hazards
  - Temp cycling, drop, bend failure isolation challenging

# New Technology – New Rules

- Technology Scaling trends not in our favour
  - New processes are expensive
  - Diminishing performance gains from process scaling
  - Dynamic power remains high
  - Leakage increases exponentially

# Power Management

## Battery Life

- Most notebooks are measured with BAPCO's Mobilemark 2002 benchmark
- Measures performance and battery life for productivity workload
  - Assumes typical usage system idle 80%, active 20%
- Future usage (two scenarios)
  - Today Usage: Sleep, active, idle
  - Always on – Low Power(connected), active, idle

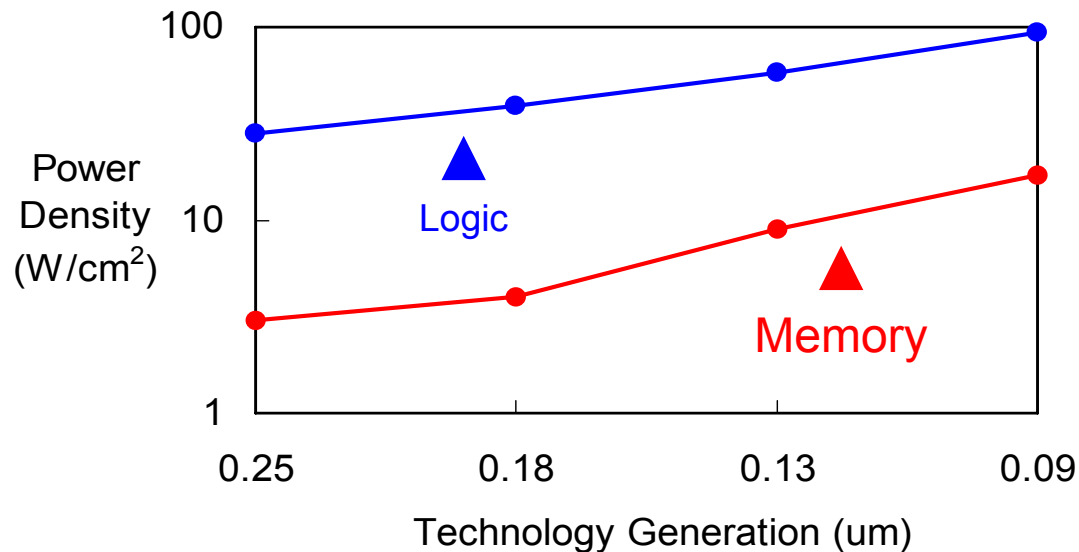
# Mobility is Happening

- *Mobility → Vision*
  - Simple secure wireless connectivity
  - Innovative form factor for life style
  - Best performance in form factor
  - Exceptional battery life
- *Mobility → Growth*
  - Mobile systems expected to be ~65% CAGR/2006
  - Strong notebook growth
- *Mobility → New lifestyle*
  - Usage Model Directions
    - Digital Office, On-the-go Lifestyle, Digital Home
  - Living Room in a handset

# Agenda

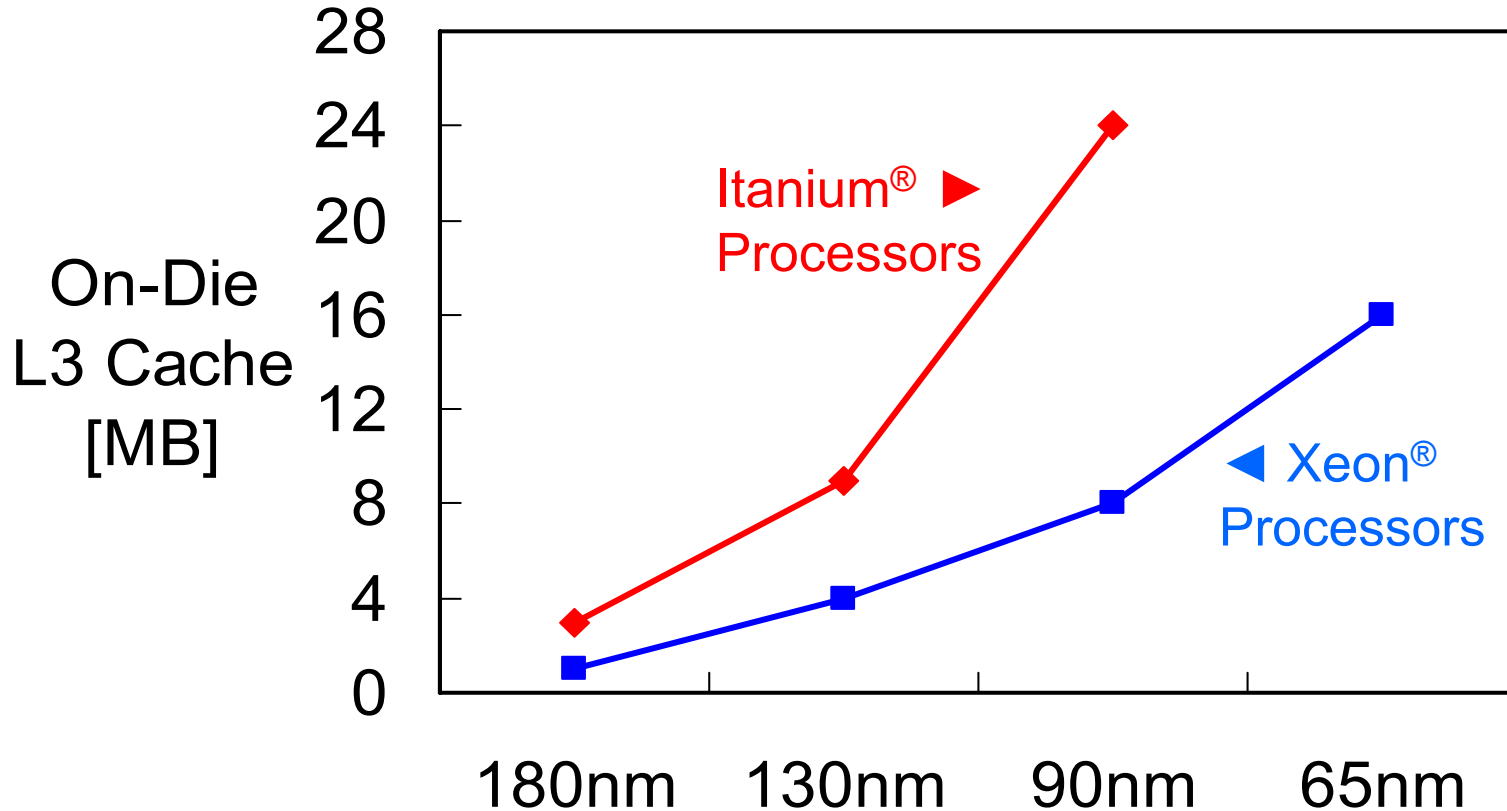
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# Exploit Memory Power Efficiency



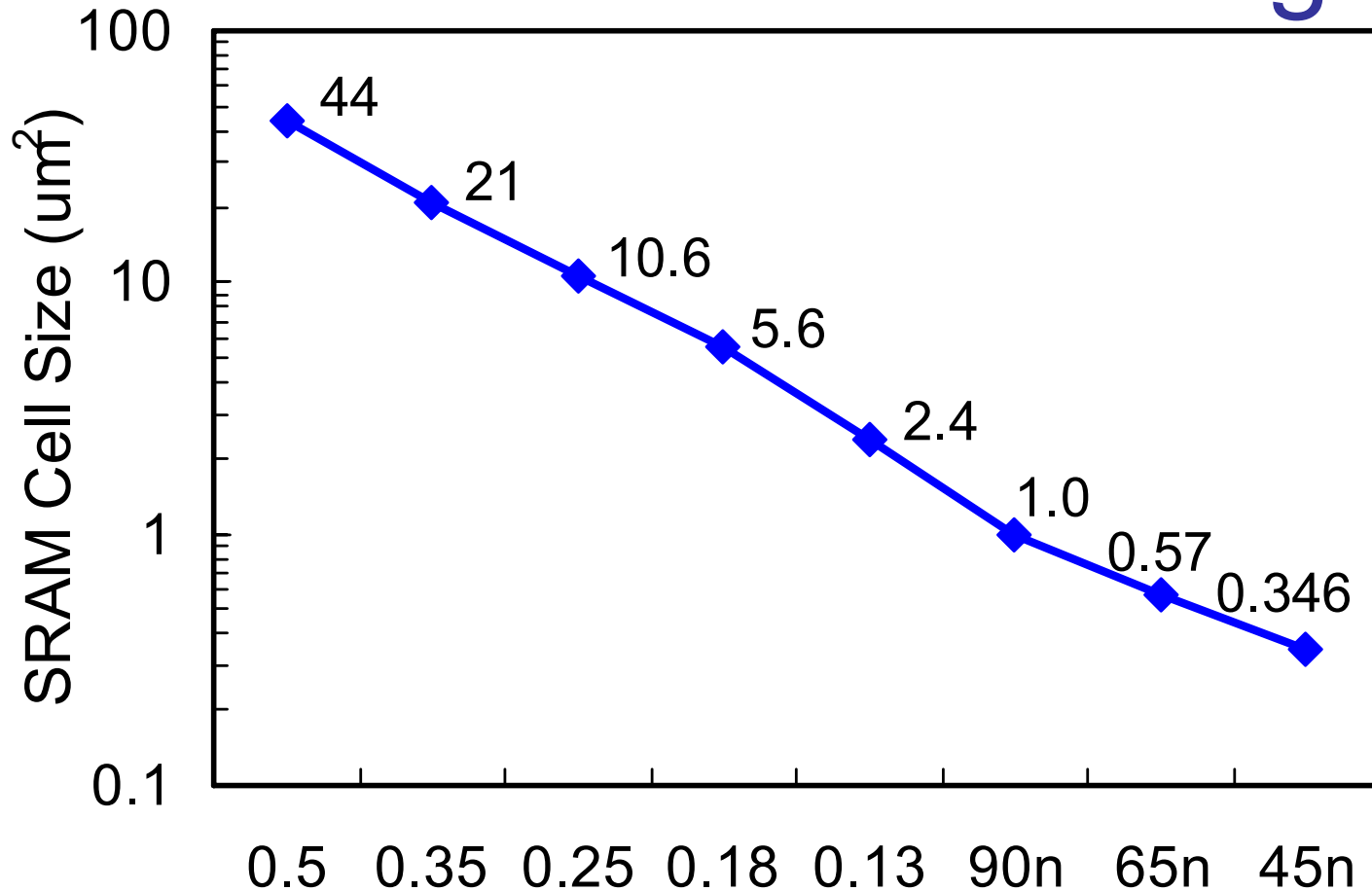
- Static memory has 10X lower active power density
- Lower leakage than logic
- On-die cache provides higher bandwidth and lower latency

# Server Processors L3 Cache Trend



Cache size doubles with every process generation

# SRAM Cell Size Scaling



SRAM cell size scales ~0.5x per generation

\*Source: S.Rusu, Intel

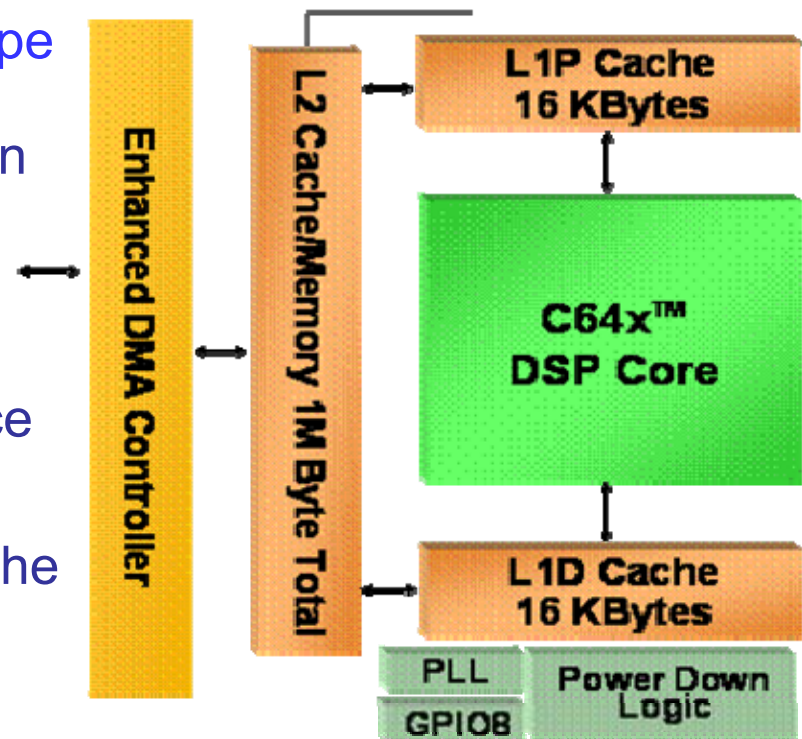
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# On-Chip 6T SRAM

Processor architectures will ALWAYS require Caches

- ◆ EVERY uP, uC, DSP, & PowerPC processor requires L1\$ & L2\$ SRAM-type memory architecture to keep the processor fed. These include Instruction \$, Data \$, Frame buffers, local buffers, etc.
- ◆ Migration of these cores & their architectures is of paramount importance as we go down the technology curve.
- ◆ Largest blocks of memory will move to the most economic solution, sometimes offchip.
- ◆ WE'LL ALWAYS NEED SRAM OR SRAM-like MEMORIES FOR CORE MIGRATIONS.



# High-Speed Memory Requirements at 65nm

- Can 6T SRAM be replaced for SoC applications?
- This is what SoC customers want at 65nm:
  - Fast Random Cycle and Access
    - 1GHz cycle and  $< 1\text{ns}$  access at “slow” process corner, 125C, VDD-10%
  - Large array efficiencies, even for small macros
    - Ex. complex SoC design:  $>300$  macros,  $<256\text{Kb}$  densities
  - Architecture flexibility (compiler options)
    - Many configurations: I/O widths, depth
    - Multiple aspect ratios with same configuration/density
- Functionality at low voltage

# Design & Process Solutions for SRAM

## ◆ Design Solutions:

- ◆ **Vtrip: use Dual voltage rails (Logic vs. Memory)**
- ◆ **Asymmetric Pass gates for Low Vt write**
- ◆ **8T cell: separate Read from Write**
- ◆ **Solutions: (WI & BL pulsing), (Read Assist), (Self Aligned Timing Control)**

	Transistor			
	W's	L's	Vtn	Vtp
Area:	↓	↓	—	—
Power:		↑	↑	↑
Iread:	↑	↓	↓	—
SNM:	↑	↑	↑	↓
Vtrip:	↑	↑	↓	↑

## ◆ Process Solutions:

- ◆ **FUSI w/ PNO - Xistor Vt variation reduced by > 20%.**
- ◆ **FinFETs — 1.5X Iread bump.**
- ◆ **FinFETs – reduced Vt scattering, reduced Vt variation due to Random Dopant fluctuation.**

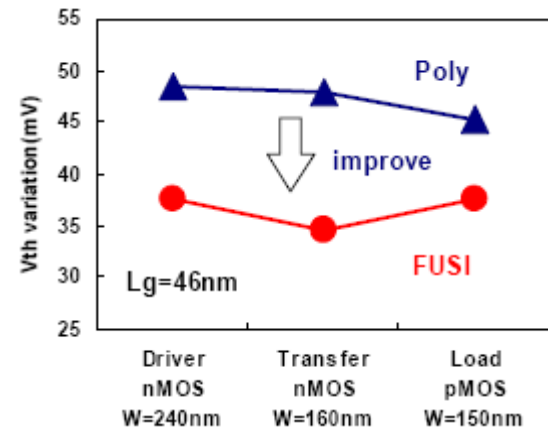
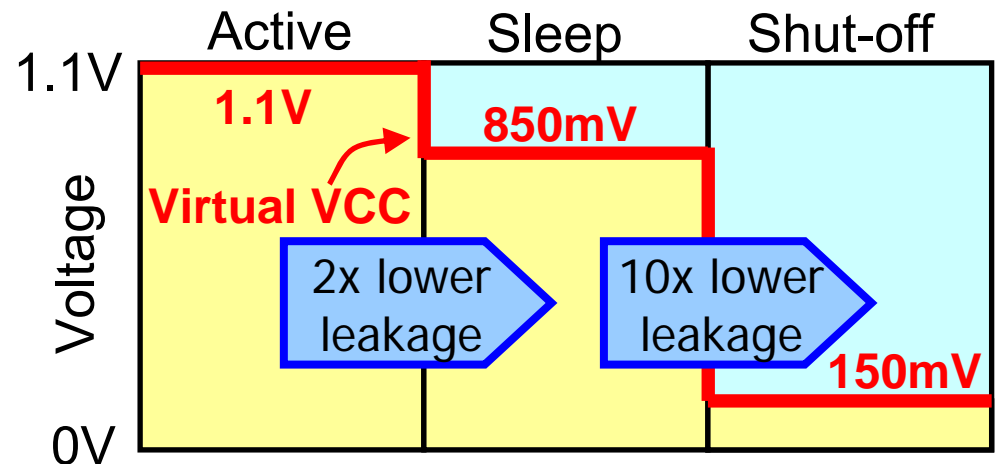
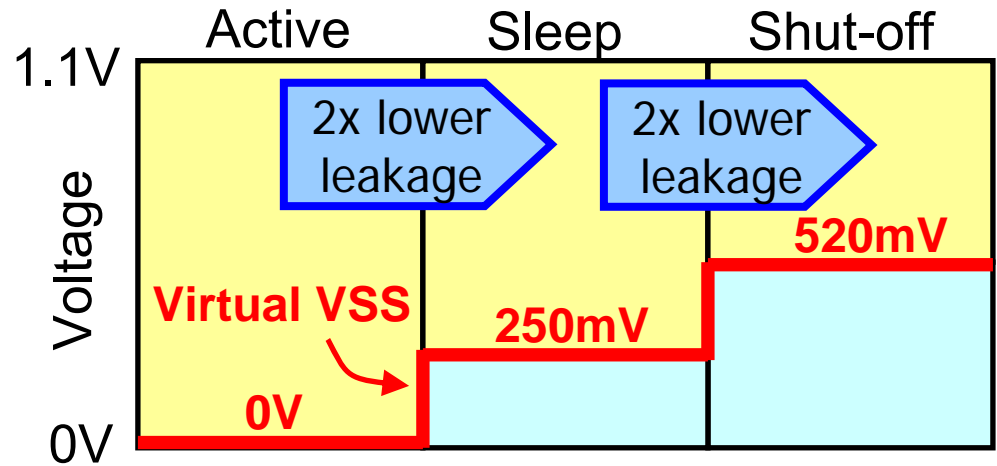
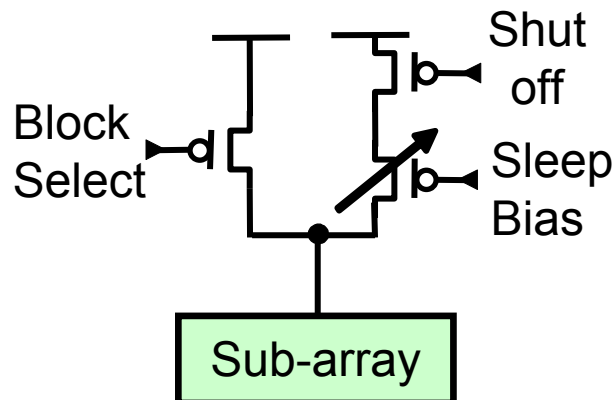
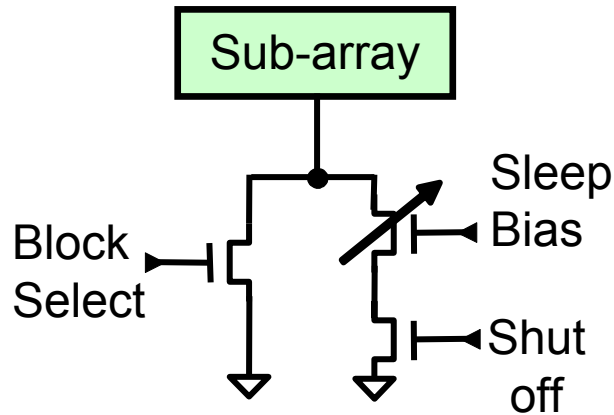


Fig.10 Vth variations improvement for small dimension transistors.

# Cache Sleep and Shut-off Modes



Sleep and shut-off modes reduce leakage in large caches

# Resolving SRAM's Challenges for 45nm and 32nm

- Improvement in application voltage tolerance and VDD droops
- Increase redundancy
- Improved timings, decrease Cells/BL
- Write/Read assist
- Separated array voltage to separate logic noise from SRAM array supply
- Higher array VDD (ex. +100mV over logic)
- Improved bit cell optimization
- **Minimize device fluctuation by limiting device-geometry scaling → larger cell**

# Alternate Memory Solutions

- 6T SRAM challenges must be resolved to meet SoC application requirements
- Other solutions can only fill dedicated niches
  - 8T SRAM
    - Faster, but not as dense → this may be acceptable
    - Improved VDDmin only if half-select operation is prevented → major architecture drawback
  - eDRAM
    - superior area, but only at higher densities (>4Mb?)
    - Can be as fast as SRAM (random cycle)[?]

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# Memory Contents in SoC

- <10% in 1998
- 20% in 2001
- 45% in 2005
- 70% in 2006/7
- Increasing trend – Will reach Saturation
  - Source: Gartner Dataquest

# Embedded Memory Requirements

- High Speed
- Easy to use
- High Bandwidth
- High Density
- High Reliability
- Low Power

# eDRAM Advantages

- Smaller Size[1/3 – 1/5]
- Low Current : 1/10, Active and 1/3.5, Standby
- High Speed (Compared to SRAM)
- Wider bandwidth (at low cost)
- Low Soft Errors (1/10x – 1/100x)
- Scalable
- Higher System Integration

# eDRAM Advantages

- High Speed
  - Devices have high driving capability
  - Silicide in WL and Storage nodes
  - 5-7 layers of metal
- High Bandwidth
  - Wide IO Bus
  - New embedded memory architecture
  - New type of Memory Interface
- High Density
- Low Power and better reliability

# eDRAM Applications

- Frame Buffer
  - Digital Camera
  - Graphic Display
  - Camcorder
- Cache Memory
- Application Processors

# eDRAM is more dense

- eDRAM cell size is 3-5x < 6T SRAM
- Enables higher system integration
- Increase product form factor, performance, cost and competitiveness

# Drawbacks of Standalone DRAM

- Low Speed
  - Conventional DRAM devices are slow
    - Process optimized for high capacity and low leakage
    - No Silicide in WL and Storage nodes
    - Min. 3 layers of metal
  - Slow comparable to SRAMs
- Low Bandwidth
  - Limit by pin counts
    - Because of multiplex address
    - Use DDR to increase bandwidth
    - Latencies are long and depend on access patterns
- Refresh
  - Reduce Memory utilization rate: increase overhead
- Standalone DRAMs are used ONLY as main memory in SoC

# eDRAM Interface

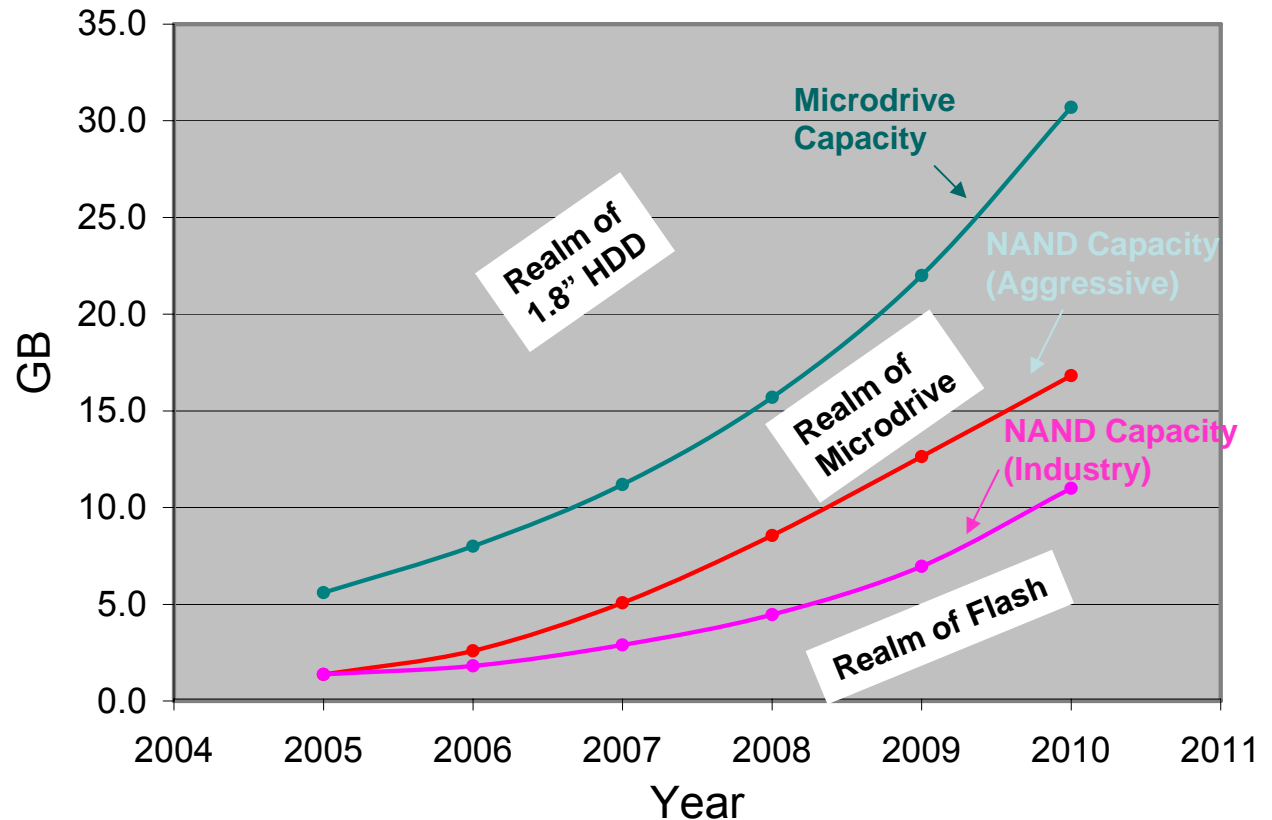
- Truly random accessible
  - Predictable delays and latencies for every access (Pipelined and FT)
- High Bandwidth
  - Standardized wide I/O buses
  - No need for DDR if integrated on-chip
  - 2X bandwidth by concurrent read/write
    - Multiple bank architecture
- Easy to use: Hidden refresh

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# FLASH vs. Microdrive

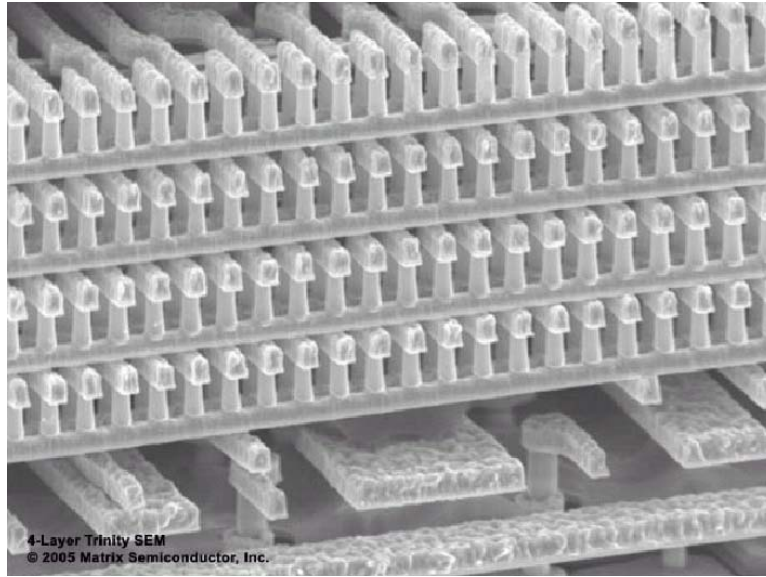
## Projected Capacity Breaking Points



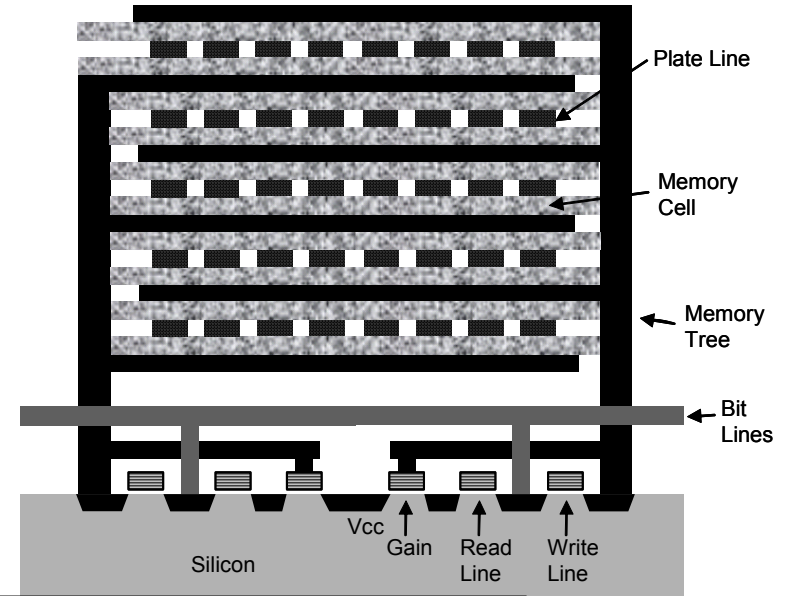
- NAND capacity is at the same price as Microdrive.
- Microdrive projection assumes 40% capacity growth per year.
- Aggressive NAND forecast assumes 2 bits-per-cell and DRAM-like commoditization.

# 3-D Cross-Point Memories

Matrix Semiconductor/TSMC 3-D anti-fuse PROM



Tree Structure FeRAM



Type	Capacity	F(nm)	Area(mm <sup>2</sup> )	Company	Type	Area(F <sup>2</sup> )/Cap
NAND	8Gb	70 (proto)	146	Toshiba	MLC	3.7 (36 Gb/in <sup>2</sup> )
PROM	1Gb	130	31	Matrix	4 layer	1.8

- **Could be up to 10 times cheaper than conventional FLASH.**
  - Small additional processing cost per layer of memory.
  - Peripheral circuits can go under array to save up to half of die area.
  - 4 layer write-once version now entering mass production.
  - Rewriteable version? 8 layer? 2 bits-per cell? 32nm pitch → 10 Tb/in<sup>2</sup>!

## ARIAL DENSITY CRITICAL TO LOW COST

Capacity	F(nm)	Area(mm <sup>2</sup> )	Company	Type	Area(F <sup>2</sup> )/Cap
<b>DRAM</b>					
256Mb	130	74	Micron	8F <sup>2</sup>	17.1
256Mb	110	45	Micron	6F <sup>2</sup>	14.5
512Mb	110	87	Infineon	8F <sup>2</sup>	14.0
512Mb	110	94	Micron	8F <sup>2</sup>	15.2
512Mb	110	78	Micron	6F <sup>2</sup>	12.6
512Mb	95	58	Micron	6F <sup>2</sup>	<b>12.6</b>
512Mb	110	81	Infineon	8F <sup>2</sup>	13.1
512Mb	100	92	Samsung	8F <sup>2</sup>	18.0
256Mb	100	50	Samsung	8F <sup>2</sup>	19.5
<b>NAND</b>					
2Gb	90	144	Samsung	SLC	8.9
4Gb	73	156	Samsung	SLC	7.3
2Gb	130	149	Toshiba	MLC	4.4
4Gb	90	136	Toshiba	MLC	4.2
8Gb	70 (proto)	146	Toshiba	MLC	<b>3.7</b>
8Gb	63 (proto)	133	Samsung	MLC	4.2
<b>AND</b>					
1Gb	130	95	Renesas	MLC	5.6
4Gb	90	126	Renesas	MLC	<b>3.9</b>
<b>PROM</b>					
512Mb	250	48	Matrix	3D/8 layer	<b>1.4</b>
1Gb	130	31	Matrix	3D/4 layer	1.8

- MLC NAND is more than three times denser than the most advanced DRAM.
- 3D cross-point memory (with 1 bit/cell) is more than six times denser than SLC NAND.

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# Innovation Enables SoC Integration

- Cost effective SoC integration requires re-optimization of system, design and process.
- Tradeoffs must be understood to find cost effective solution partition between where innovation needs to happen

# What's Next?



**Various Solid State Memory Type Characteristics**

	MRAM	FRAM	3DM	OUM	MEMs	Electrolyte
Cell Size	Large	Moderate	Very small	Small	Large & small	Very small
CMOS compatibility	Low temp New materials	H <sub>2</sub> intolerant New materials	New materials	New materials	New materials	New materials
Read Speed	Fast	Moderate Disruptive	Slow (random) Moderate (burst)	Moderate	Fast	Fast
Write Speed Write Power	Fast High	Moderate Moderate	Slow Moderate	Moderate Moderate	Moderate Moderate	Fast Low
R/Wr Cycles	High	High	n/a (read only)	High	High	Good
Scaleable	Moderate	More difficult	Good	Good	Moderate	Good
Maturity	1 <sup>st</sup> products	Low density Production	Initial Product coming	Prototyping	Millipede- experimental	Experimental

# Next Generation CMOS Challenges

- Immersion 193nm lithography with extensive resolution enhancement technology
- Low leakage and high performance sub-40nm transistors
  - Strain Engineering
  - High-k Gate dielectric and metal gate
- Copper interconnect with ultra low-k dielectric
- Process complexity
  - Integration and materials development
- Process and Design Interaction
  - Physical design impact on yield
  - Power mgmt

# The Next Big Thing: Converged Devices



**Small-Form-Factor HDDs will be a key enabler of converged mobile phones**

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# Thank You

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