



SRDC IBM Microelectronics

Scaled CMOS Technology and Models to Support Wireless Applications

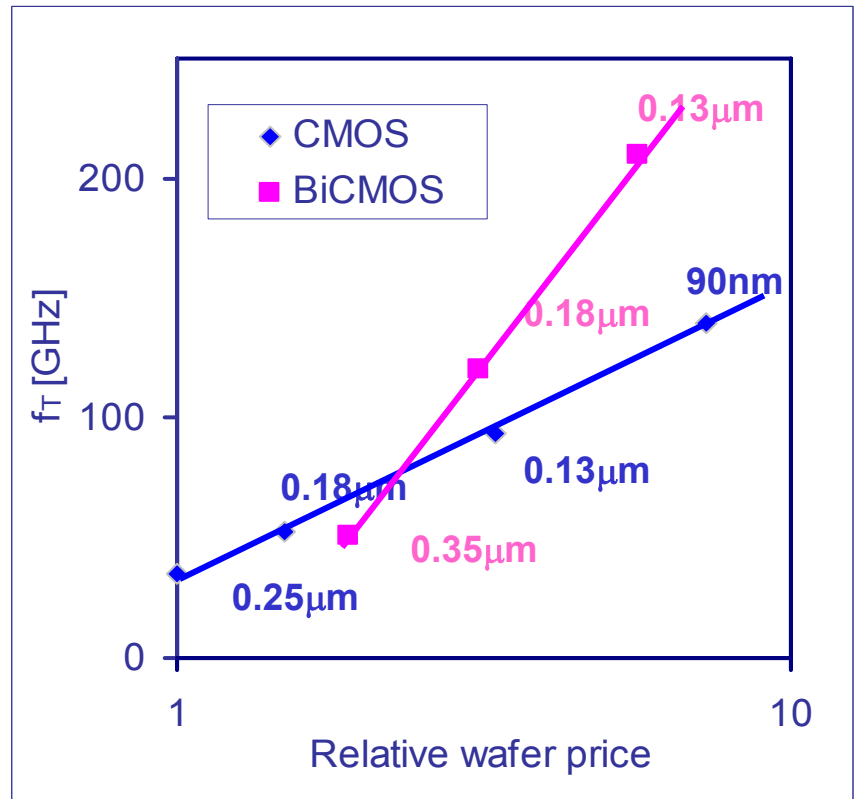
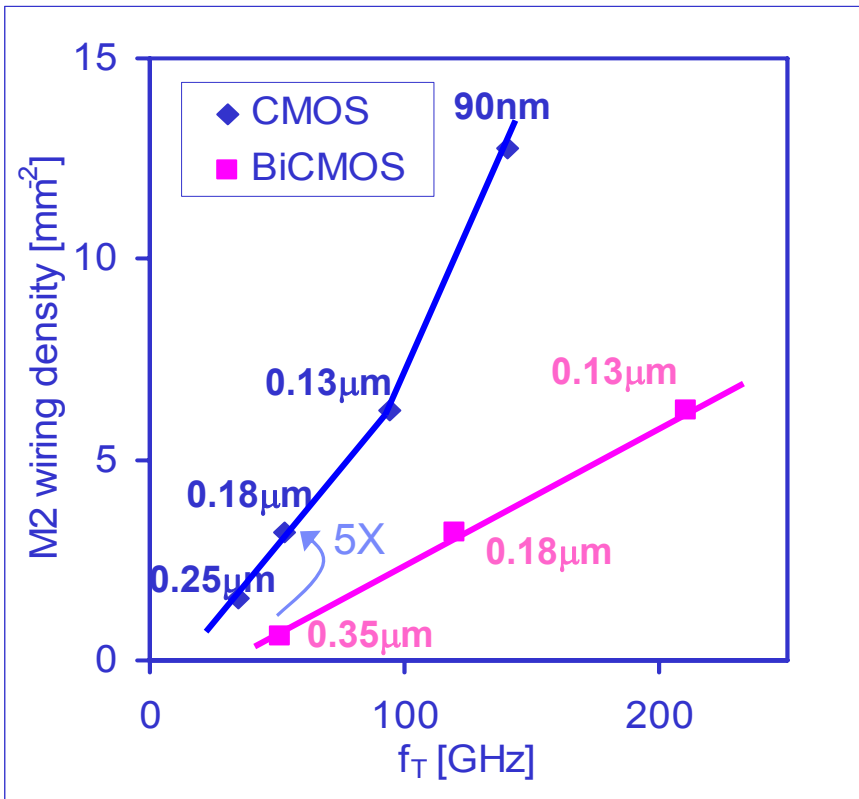
John J. Pekarik

- **Motivation & challenges**
 - RF CMOS an emerging technology?
 - Scaling: challenges and benefits
 - Materials engineering
- **Technology Features**
 - Base and high performance devices
 - Lumped and distributed passives
- **Models and coordinated design tools**
 - High-frequency
 - Noise
 - Linearity
- **Summary**

- **Wireless News: Intel touts dual-band CMOS Wi-Fi transceiver**
 - Posted by Tim [2005-06-17 12:37:20]
 - Intel Corporation today announced it has developed a prototype of an all-CMOS direct conversion dual-band radio transceiver capable of supporting "every current Wi-Fi standard" in the 2.4 and 5GHz bands.
- **QUALCOMM Announces Industry's First Single-Chip, RF CMOS Transceiver with Integrated Receive Diversity and GPS for CDMA2000 Networks**
 - Posted: 4/5/2006 @ 8:46 AM
- **Realtek Develops UWB CMOS RFIC Transceiver**
 - Hsinchu, Taiwan, and San Francisco, California, USA – January 31, 2005
 - Realtek Semiconductor Corp. today announced that it has successfully developed a compact low-power CMOS RFIC transceiver for Ultra-Wideband (UWB) applications, marking a significant technological breakthrough.
- **Silicon Wave And RF Micro Devices Announce Availability Of Bare Die Single-Chip CMOS Bluetooth Components**
 - Business Wire, June 16, 2003
- **News Release from: NewLogic**
 - Edited by the Electronicstalk Editorial Team on 13 June 2002
 - NewLogic Technologies has released its Boost Radio IP core - a 2.4GHz CMOS Bluetooth transceiver featuring low power consumption and small die size.

HBT vs NFET: Area vs. cost vs. performance

- **CMOS advantage: integration density**
- **Digital function scales dramatically with node**
 - RF function not likely to scale in area
 - Chips with significant digital content area savings
- **SoC vs. SiP considerations**
 - Integration density
 - Die cost, Package cost
 - IP development, re-use



NFET Scaling in Bulk CMOS nodes

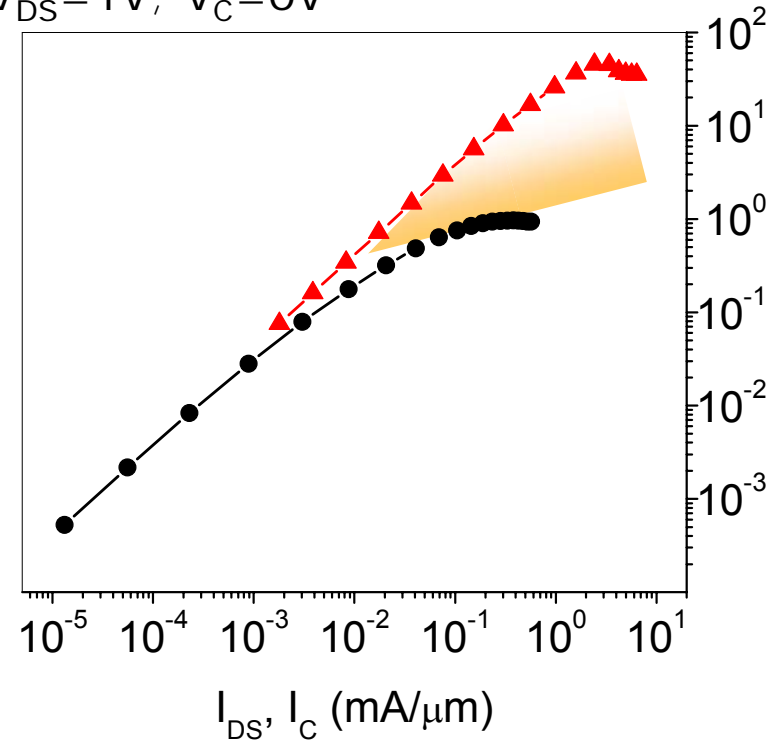
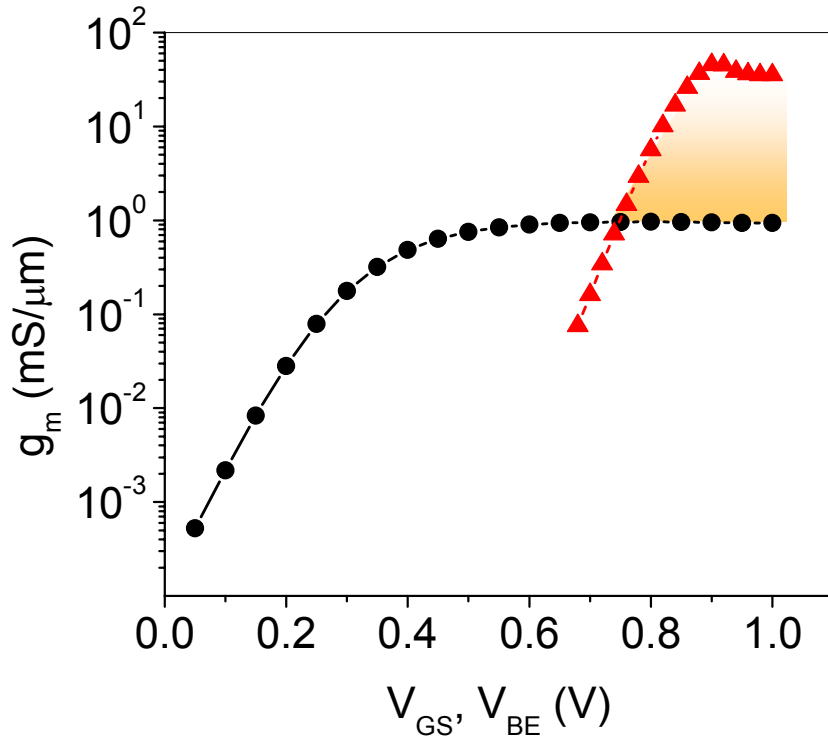
Node	nm	250	180	130	90	65
L_{GATE}	nm	180	130	92	63	43
$t_{\text{OX}}(\text{inv.})$	nm	6.2	4.45	3.12	2.2	1.95
V_{DD}	V	2.5	1.8	1.5	1.2	1
V_{T}	V	0.44	0.43	0.34	0.36	0.24
peak g_m	$\mu\text{S}/\mu\text{m}$	335	500	720	1060	1500
g_{ds} (@peak g_m)	$\mu\text{S}/\mu\text{m}$	22	40	65	100	240
g_m/g_{ds}	-	15.2	12.5	11.1	10.6	6.3
Peak f_{T}	GHz	35	53	94	140	250
M2 pitch	μm	0.8	0.56	0.4	0.28	0.2

- **L_{poly} scaled faster than t_{ox} and V_{dd}**
- **For velocity saturated case, $g_m \propto 1/t_{\text{ox}}$**
 - g_m scaling beyond 90nm augmented by mobility enhancing techniques
- **For velocity saturated case, $f_{\text{T}} \propto 1/L_{\text{poly}}$**
 - f_{T} scales faster beyond 90nm because of strong increase in g_m
- **Decreasing g_m/g_{ds} ratio a big concern for analog/rf design**

Challenges using scaled MOS

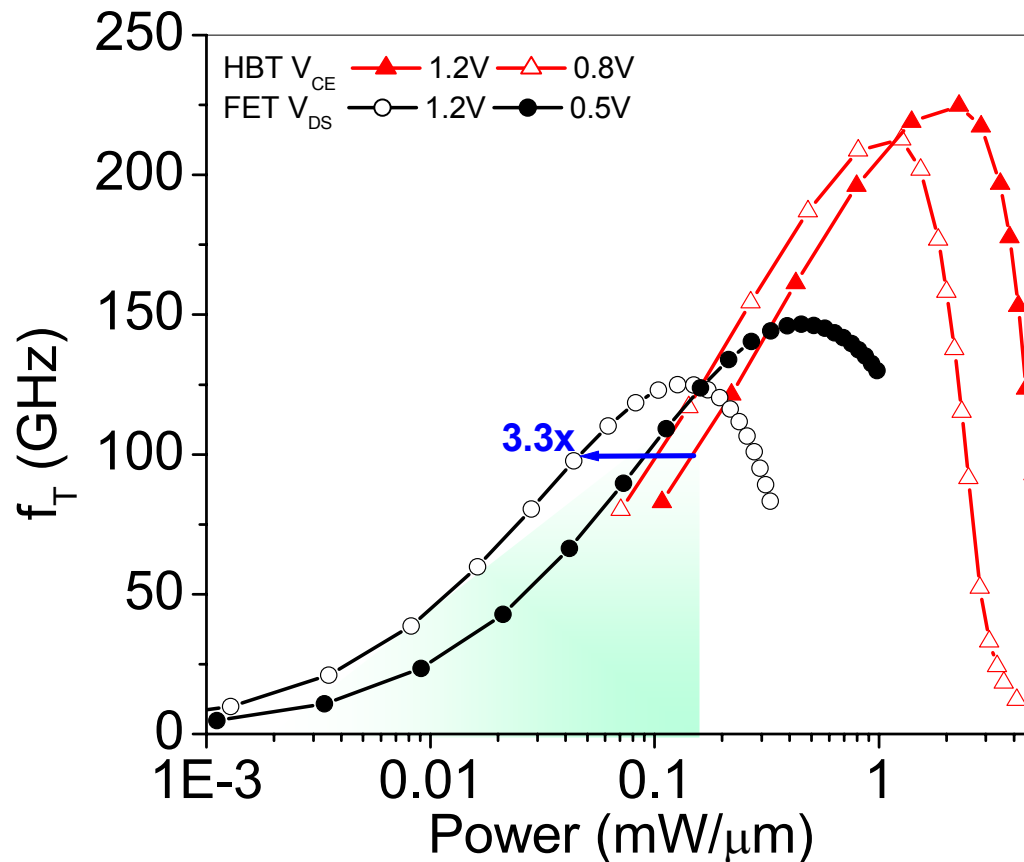
- **Higher flicker noise compared to HBT**
 - E.g. impact to VCO can be mitigated by
 - Symmetrical design and noise cancellation techniques
 - Larger devices
 - **Lower g_m compared to HBT**
 - Requires using wider devices
 - **Higher g_{ds} compared to HBT**
 - Further aggravated by technology scaling
 - Use of cascoded devices or “Analog FETs ” in some applications
 - **Lower maximum voltage compared to HBT**
 - Further aggravated by technology scaling
 - Results in lower supply voltage
 - Innovative circuit architecture required
 - **High input impedance**
 - Difficulty with impedance matching
 - Difficulty with measuring/extracting model parameters
 - **Analog/RF model accuracy approaching that of HBT**
 - Linearity, Noise parameters
- **Could affect design cycle**

• nFET ▲ HBT $V_{DS}=1V$; $V_C=0V$



- $V_T < V_{BE}$: FETs g_m can be obtained at low voltage
- HBT $g_m \gg$ FET g_m

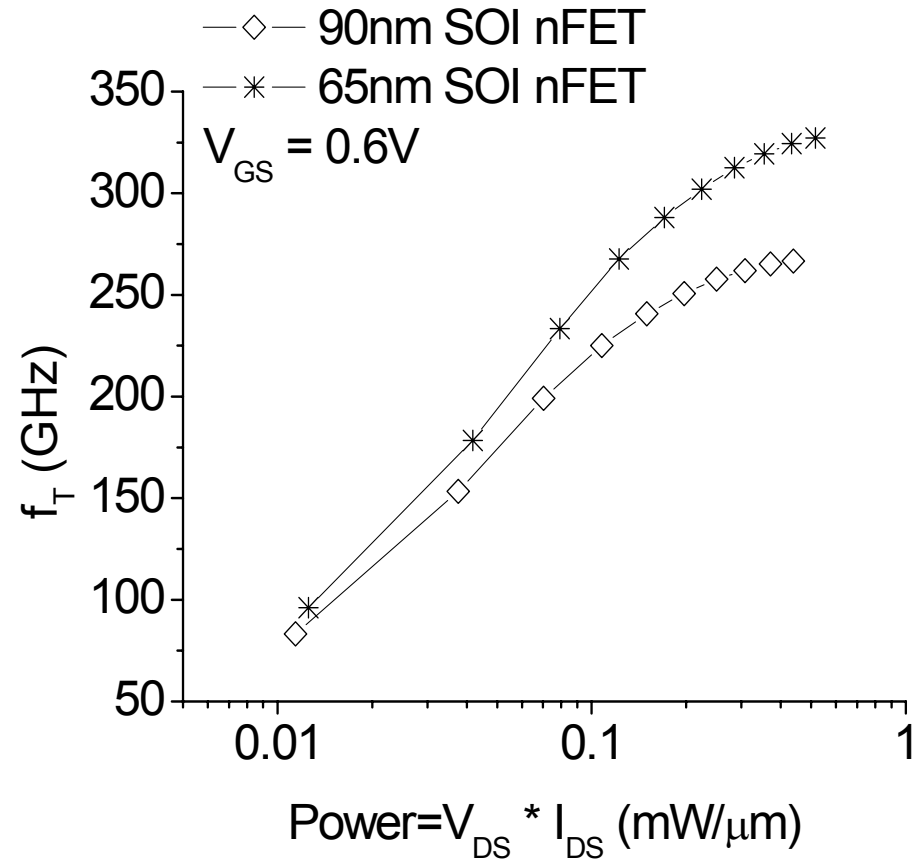
Device f_T -Power Comparison



- V_{CE} in HBT limited by CB junction forward-bias concern
- High f_T in FET possible at low supply voltage
- Power reduction by V_{DS} lowering effective in FET

90nm/65nm FETs: Low Power Performance

- **Potential for very low power in CMOS technologies**
 - $f_T = 100\text{GHz}$ @ $12 \mu\text{W}/\mu\text{m}$
 - $f_T = 330\text{GHz}$ @ $0.5 \text{mW}/\mu\text{m}$
- f_T @ $< 1/10^{\text{th}}$ power of SiGe or III-V technologies



- **Substrate Induced Strain**, *VLSI 2002*

Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs

K. Rim, J. Chu, H. Chen*, K.A. Jenkins, T. Kanarsky*, K. Lee, A. Mocuta*, H. Zhu*, R. Roy, J. Newbury, J. Ott, K. Petrarca*, P. Mooney, D. Lacey, S. Koester, K. Chan, D. Boyd*, M. Jeong*, and H.-S. Wong

- **Liner Induced Strain**, *IEDM 2000*

Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design

Shinya Ito, Hiroaki Namba, Kensuke Yamaguchi, Tsuyoshi Hirata, Koichi Ando, Shin Koyama, Shunichiro Kuroki, Nobuyuki Ikezawa, Tatsuya Suzuki, Takehiro Saitoh, and Tadahiko Horiuchi

- **Stress Memorization Technique**, *IEDM 2002*

Novel Locally Strained Channel Technique for High Performance 55nm CMOS

K. Ota, K. Sugihara, H. Sayama, T. Uchida, H. Oda, T. Eimori, H. Morimoto and Y. Inoue

- **Embedded SiGe**, *IEDM 2003*

A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors

T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann*, K. Johnson*, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson and M. Bohr

- **Channel Orientation**, *VLSI 2004*

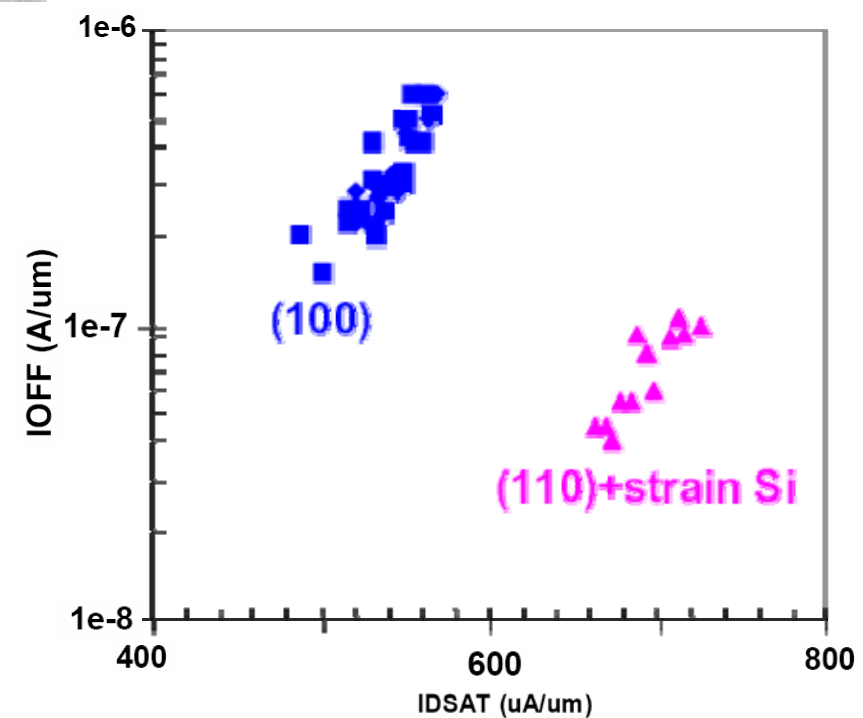
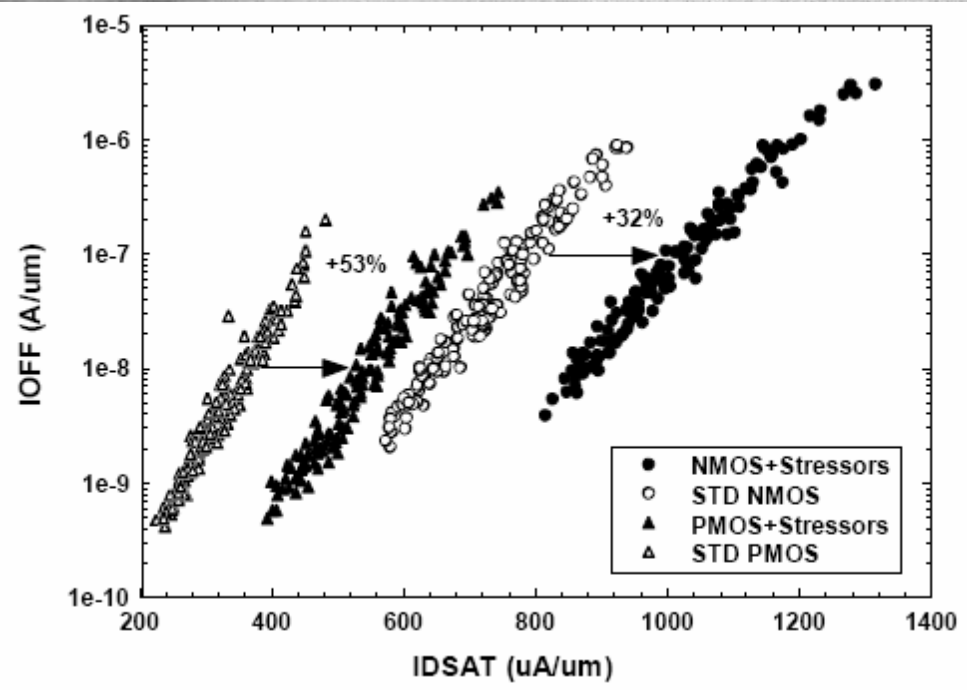
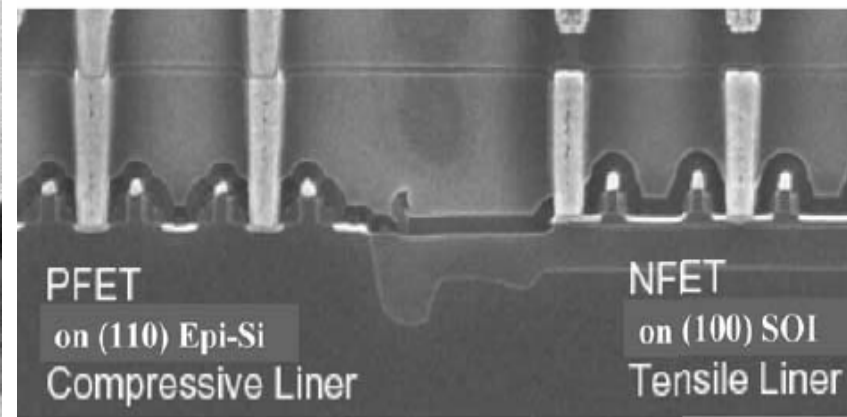
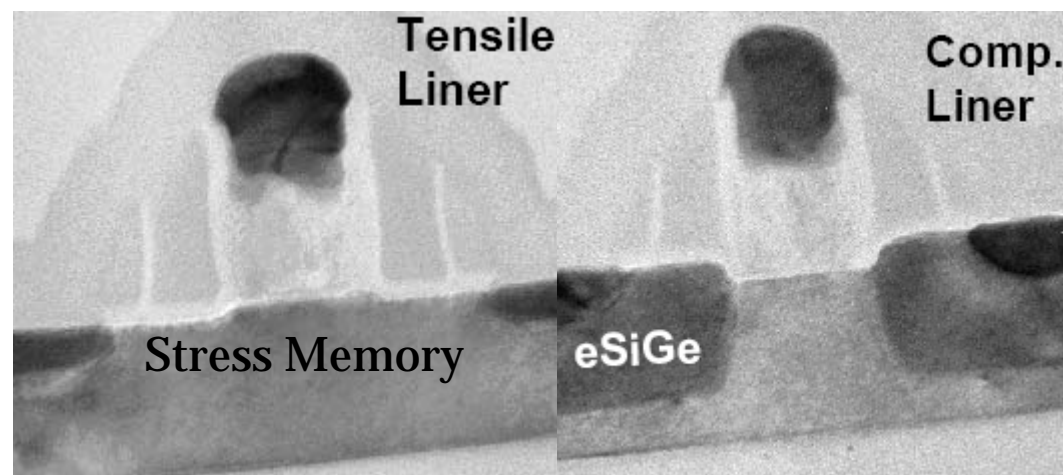
On the Integration of CMOS with Hybrid Crystal Orientations

M. Yang, V. Chan⁺, S. H. Ku⁺, M. Jeong⁺, L. Shi, K. K. Chan, C. S. Murthy⁺, R. T. Mo⁺, H. S. Yang⁺, E. A. Lehner⁺, Y. Surpris⁺, F. F. Jamin⁺, P. Oldiges⁺, Y. Zhang, B. N. To, J. R. Holt⁺, S. E. Steen, M. P. Chudzick⁺, D. M. Fried⁺, K. Bernstein, H. Zhu⁺, C. Y. Sung⁺, J. A. Ott, D. C. Boyd⁺, and N. Rovedo⁺

Combining Techniques to Maximize I_{dsat}

[Horstmann, IEDM' 05]

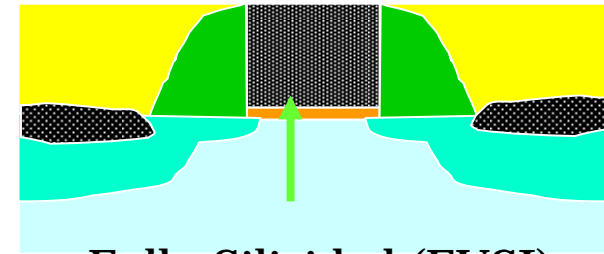
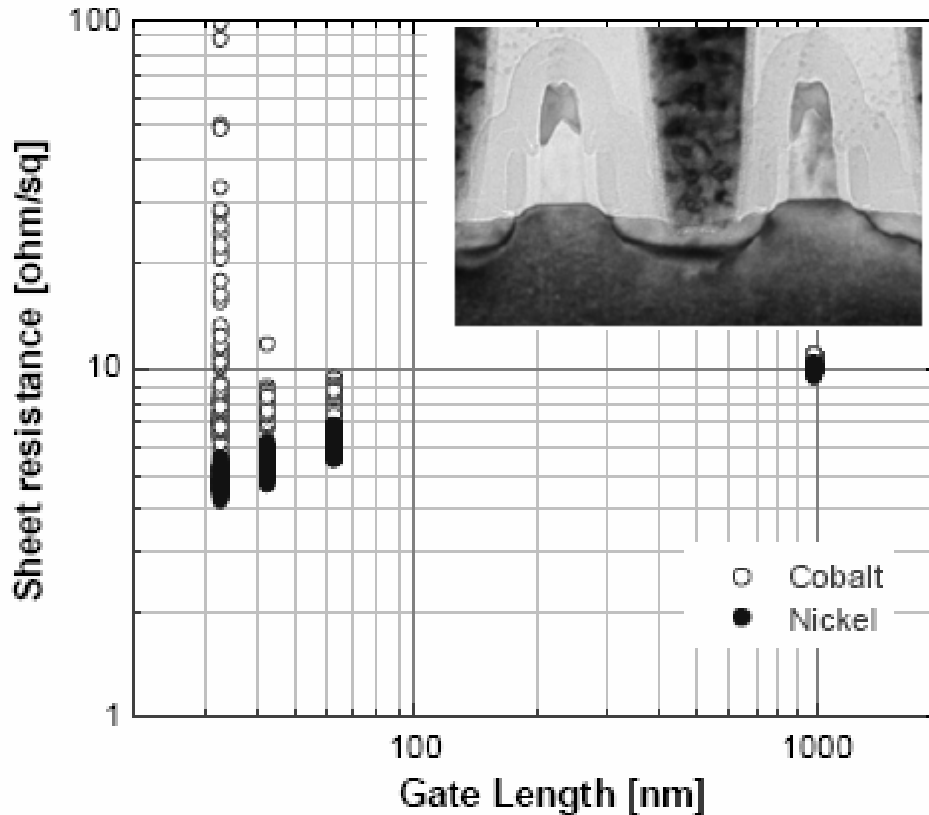
[Yang, VLSI' 04]



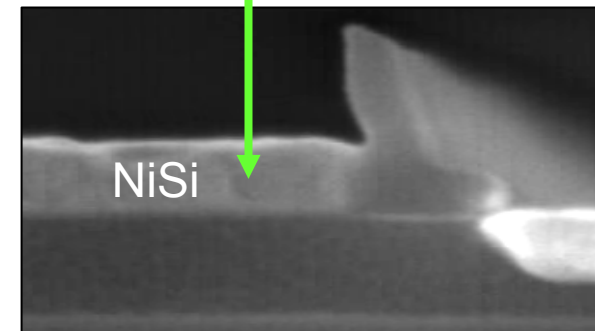
[Steege, IEDM '05]

[Kedzierski, IEDM '02]

Silicide Resistance in 65nm node



Fully-Silicided (FUSI) gate



- **NiSi: Lower resistivity & better uniformity**
 - Better f_{MAX} & NF
- **FUSI expected to provide more relief with f_{MAX} scaling**

- **Digital CMOS = low cost & integration**
 - FETS: logic & IO
 - “Parasitic” devices
 - Varactors, resistors, diodes, inductors, capacitors
- **Optional high-performance features**
 - If required or leads to lower cost
- **High-frequency models**
- **Coordinated design tools**

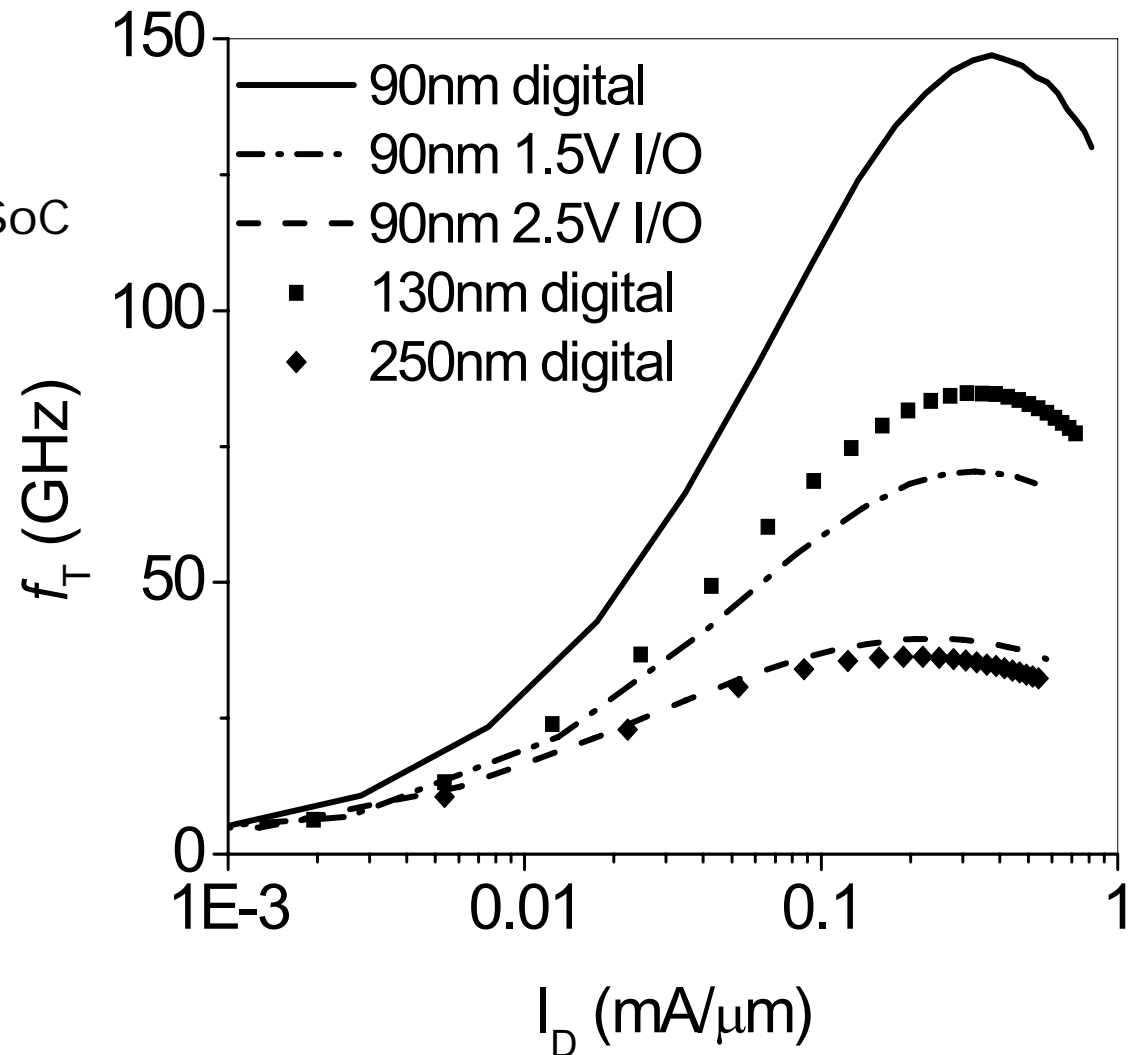
Features – optional FETs

- **IO FETs**

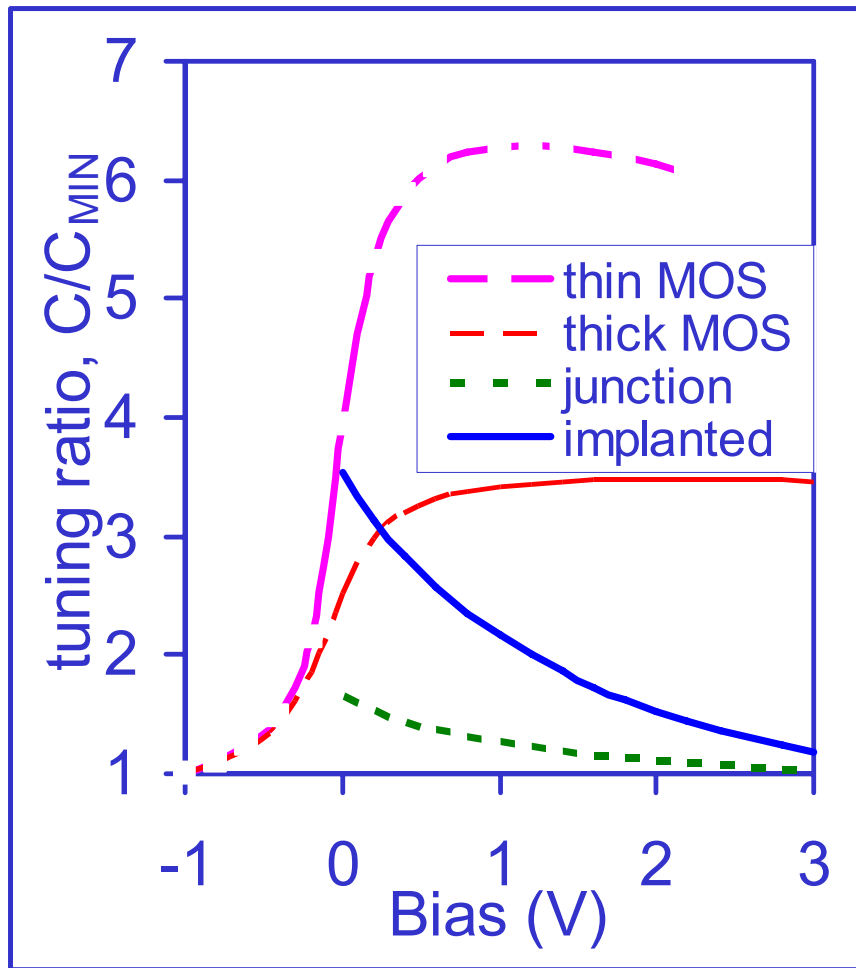
- Higher-voltage
- Technology Migration for SoC

- **Other options**

- V_T options
- High-voltage tolerant
- Analog-friendly

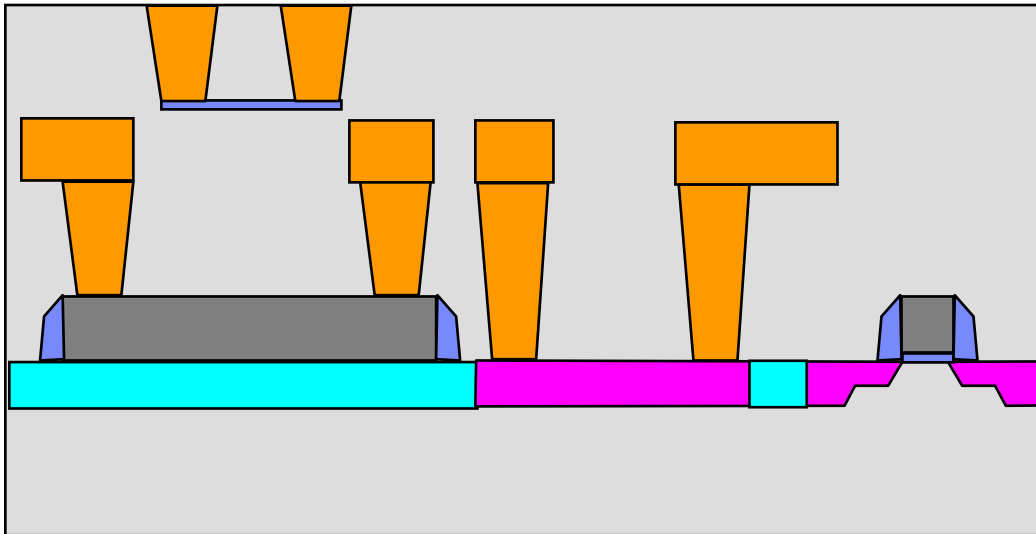


Features – MOS and junction varactors

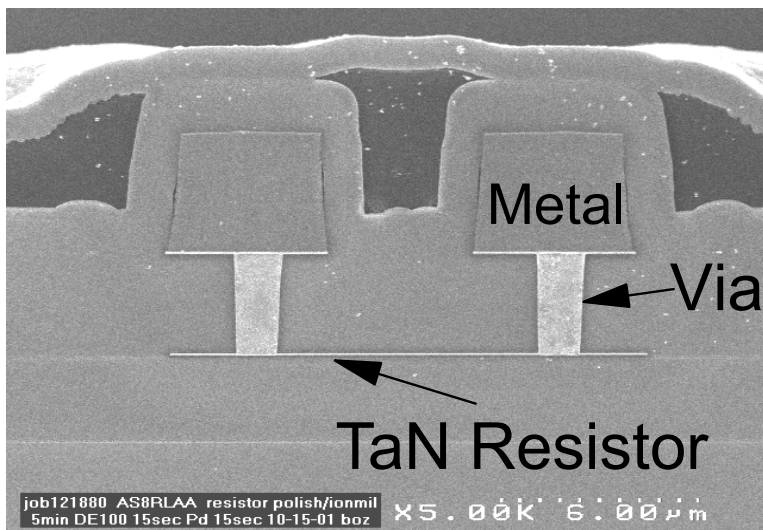


- **Desire large tuning ratio and low tuning rate**
- **MOS varactors have high tuning ratio**
 - Large tuning rate
- **Junction varactors have low tuning rate**
 - Low tuning ratio
- **Added doping in junction varactor gives both**

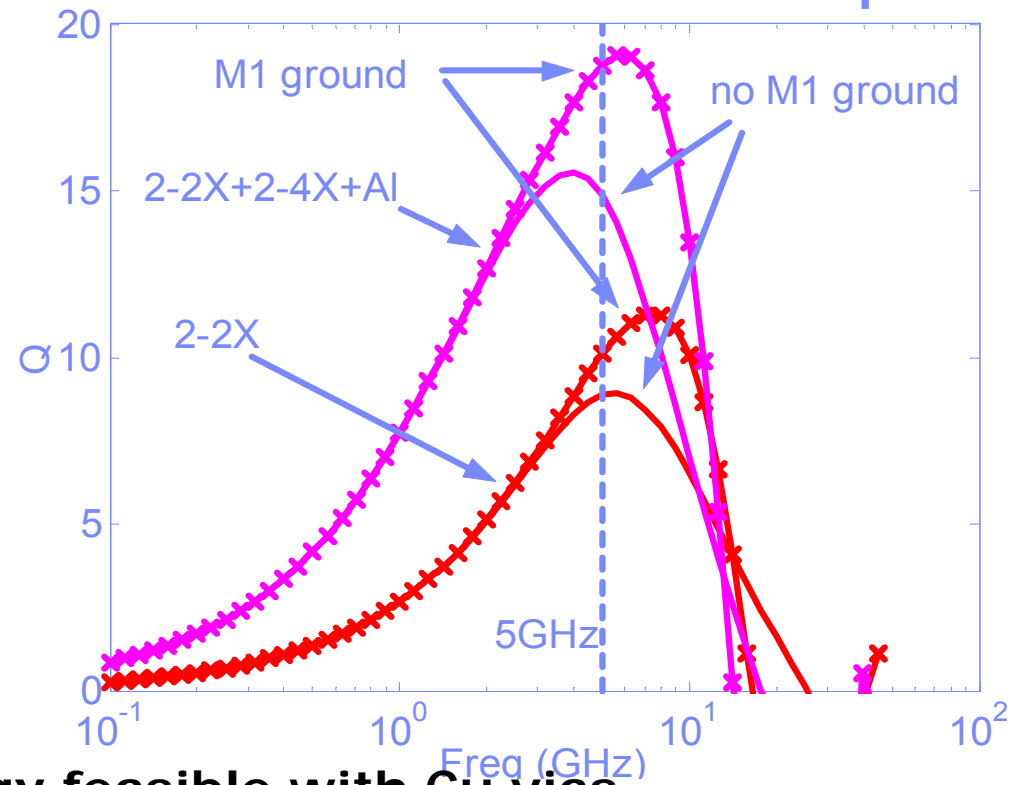
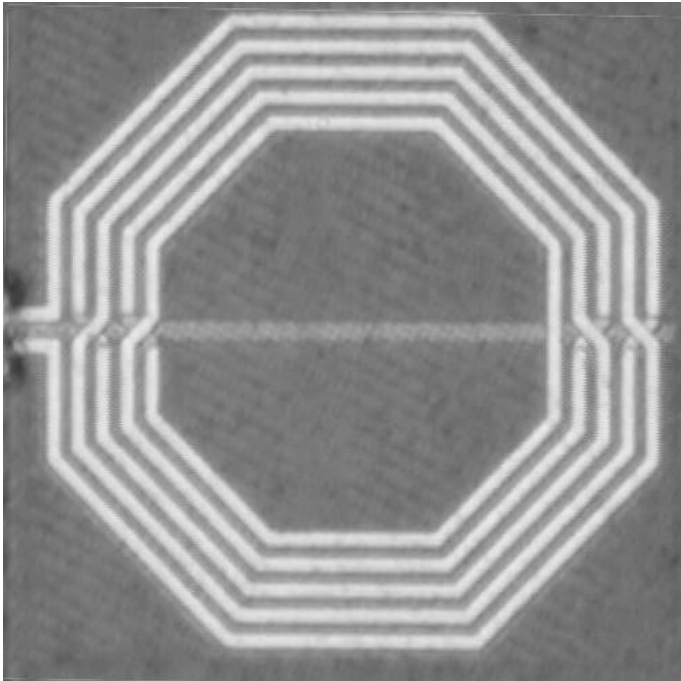
Features – resistors



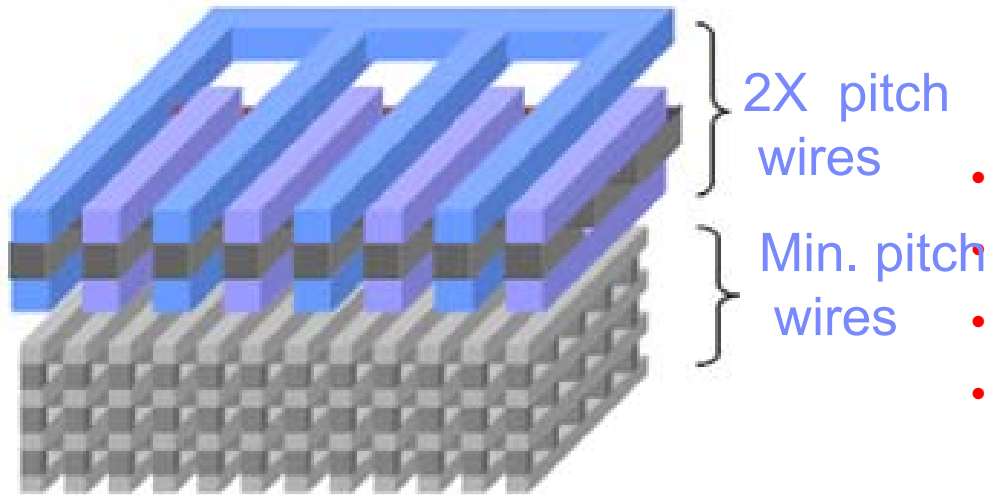
- **Silicided poly & active Wells**
- **Silicide blocked**
- **Thin-film resistor**
 - tolerance of ~8%
 - Low capacitance
- **Polysilicon resistor**
 - Dedicated mask => low tolerance



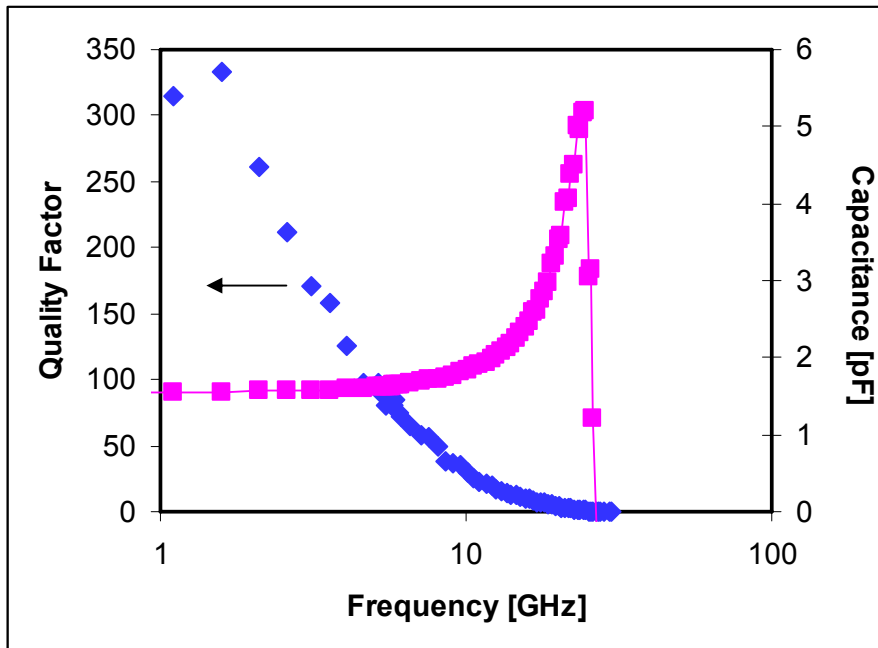
IBM 90nm CMOS example



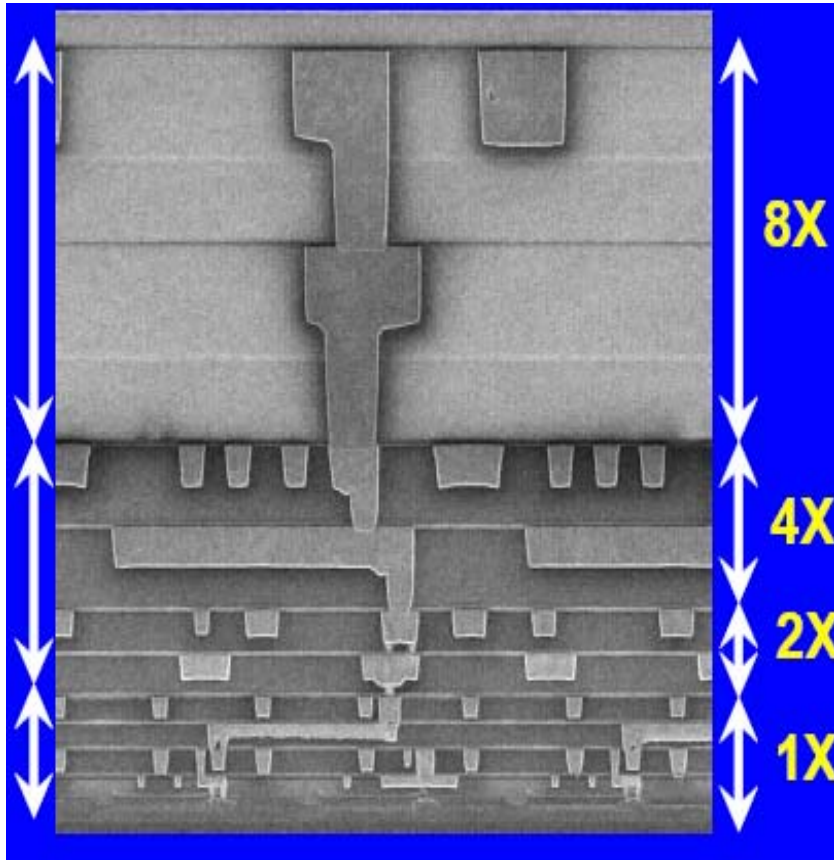
- **Symmetric-spiral topology feasible with Cu vias**
 - Saves chip area for differential applications
 - High-quality inductors in std. wiring levels
 - Model-linked p-cell interface



- Capacitor from std. wiring
- Intra-level capacitance
- Symmetric device
- This wire stack gives 1.7 fF/um² in oxide
- Low leakage current <1pA
- Superior RF characteristics
- Also known as VPP, MOM
- Low-cost alternative to high-K MIM

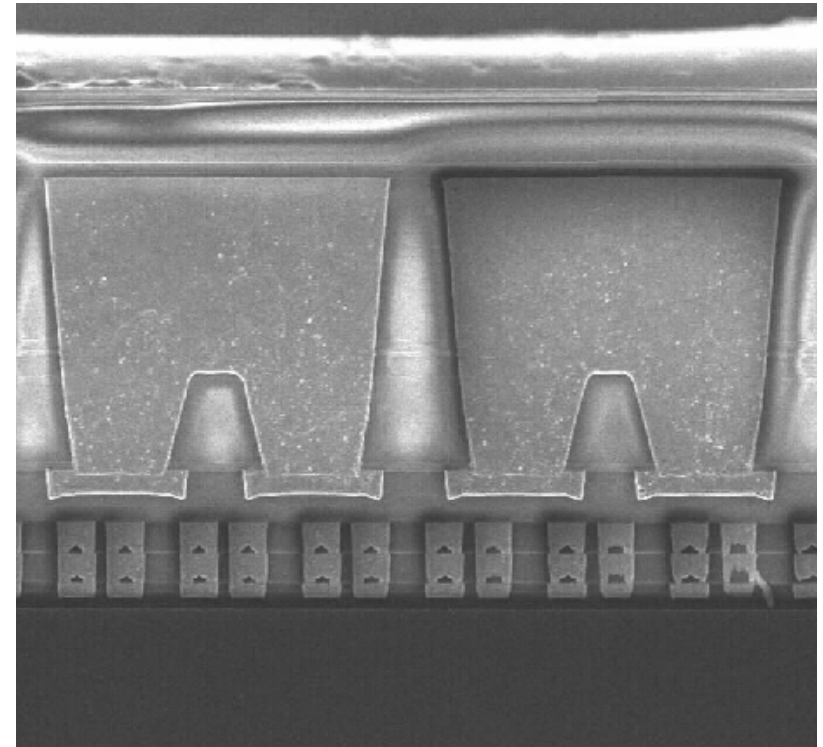


65nm Cu BEOL

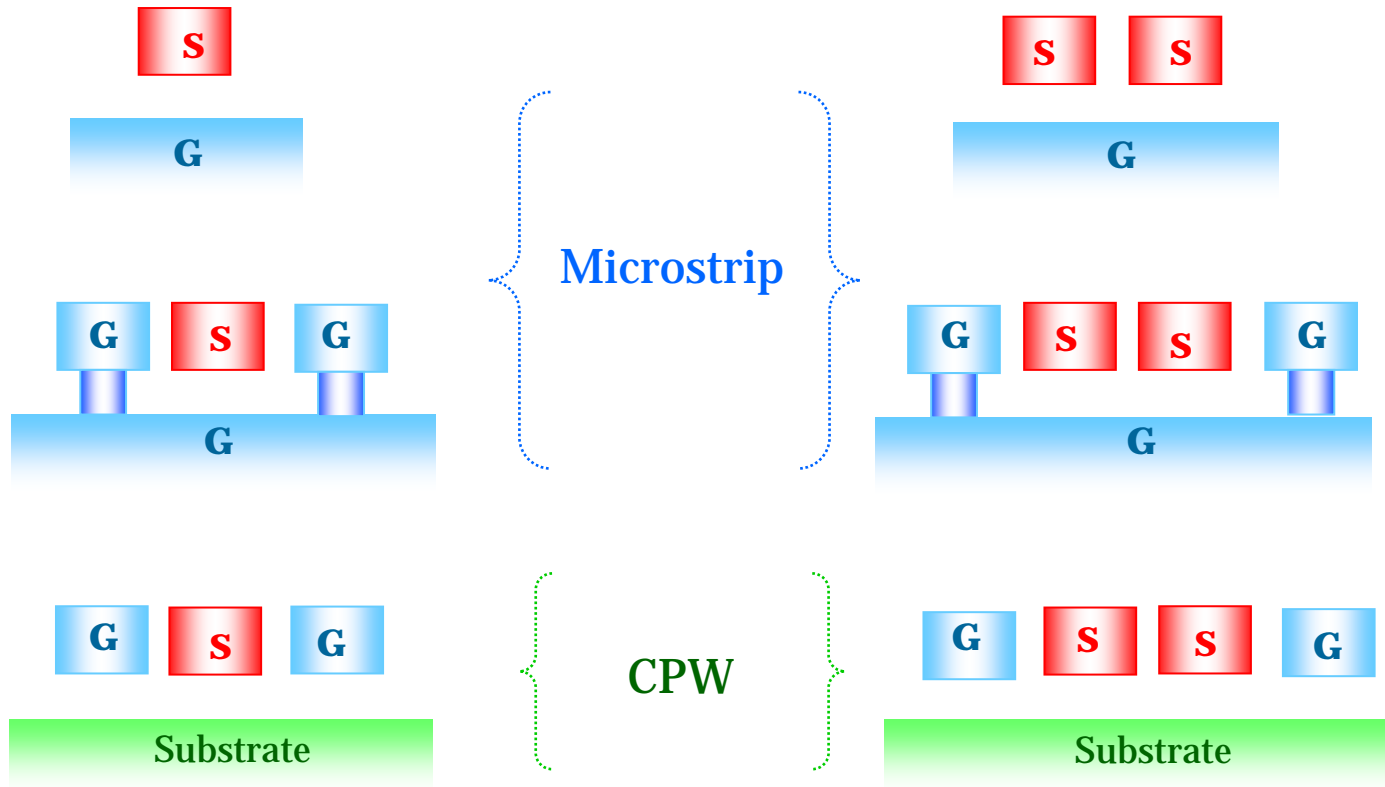


[Jagannathan, SiRF, '06]

3 μ m Cu

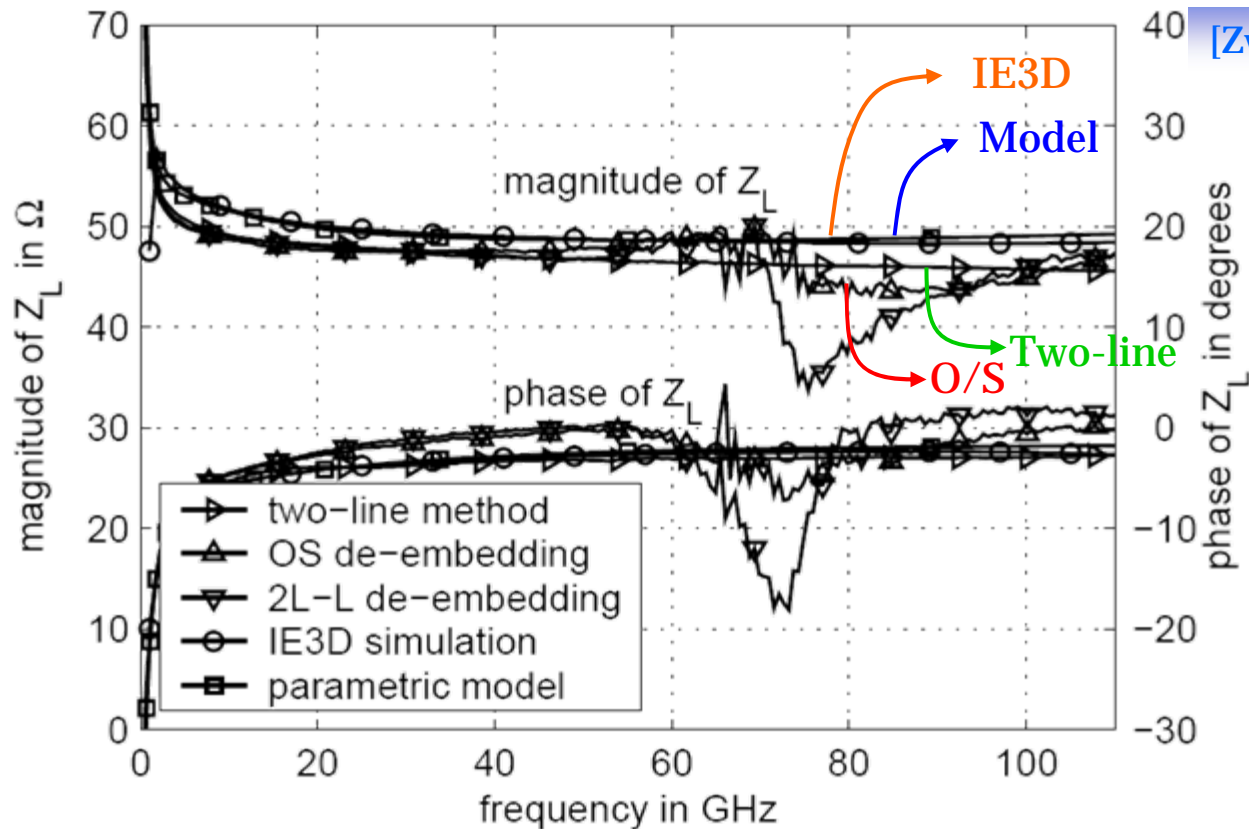


- Total BEOL stack height nearly $\sim 10\mu\text{m}$
- 3 μm Cu wire as optional integrated element



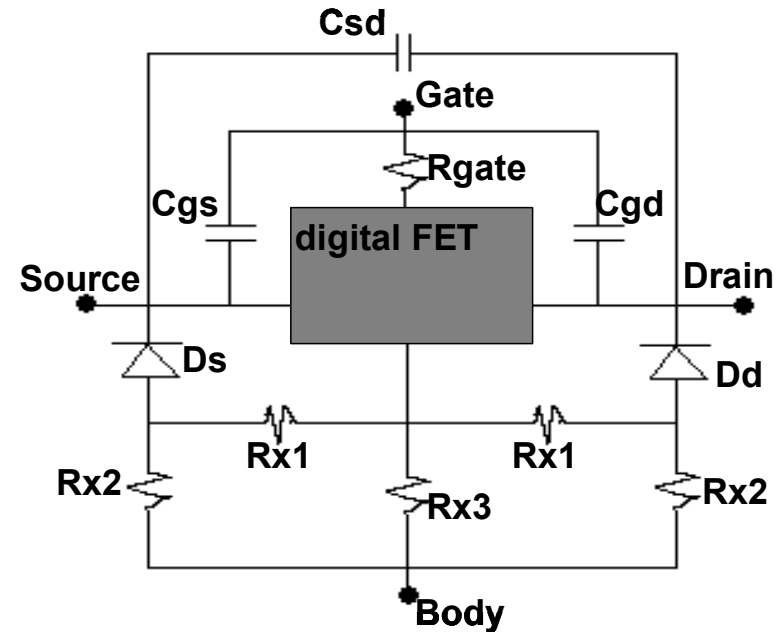
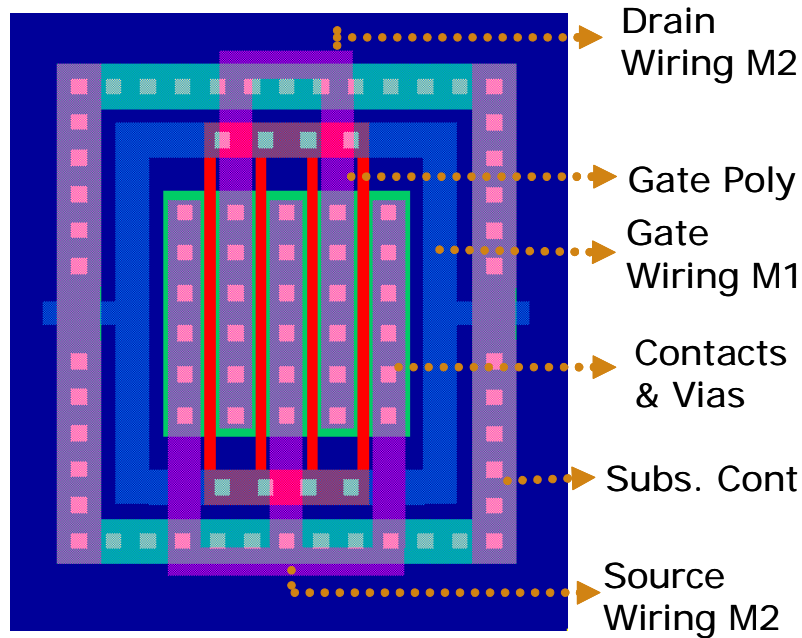
- T-line P- cells with broadband models in design kits
- Microstrip and CPW line for single & differential operation
- Minimize silicon losses and present closed EM environment

T-Lines: De-embedding & Modeling

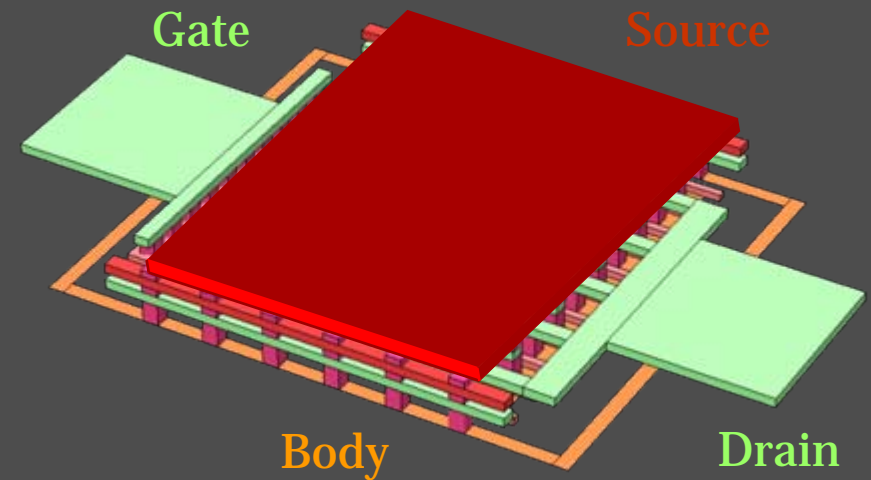
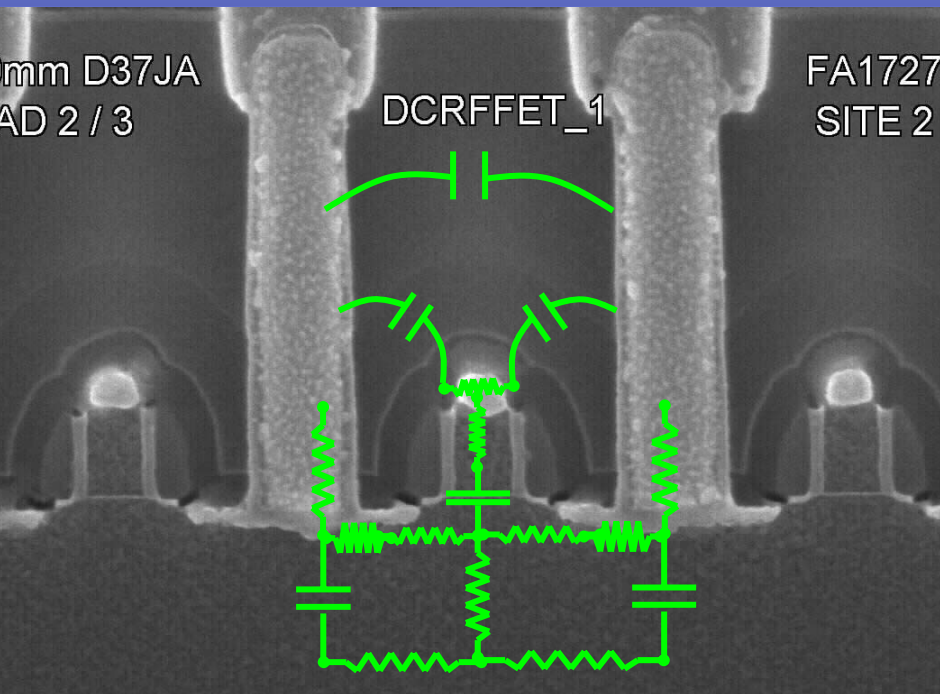


- **Need well designed deembedding stds. & method to determine γ & Z_0**
- **Accurate T-Line parametric model up to 100GHz**
 - Models capture skin effect, proximity effect and substrate effects
 - Model compared against HFSS till 250GHz

Models – RF MOSFET P-Cell and RF Model

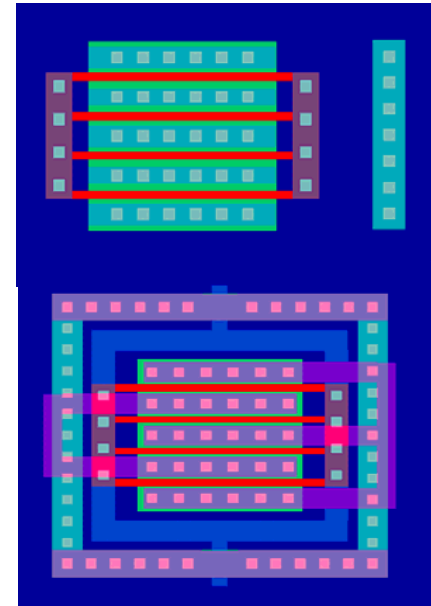
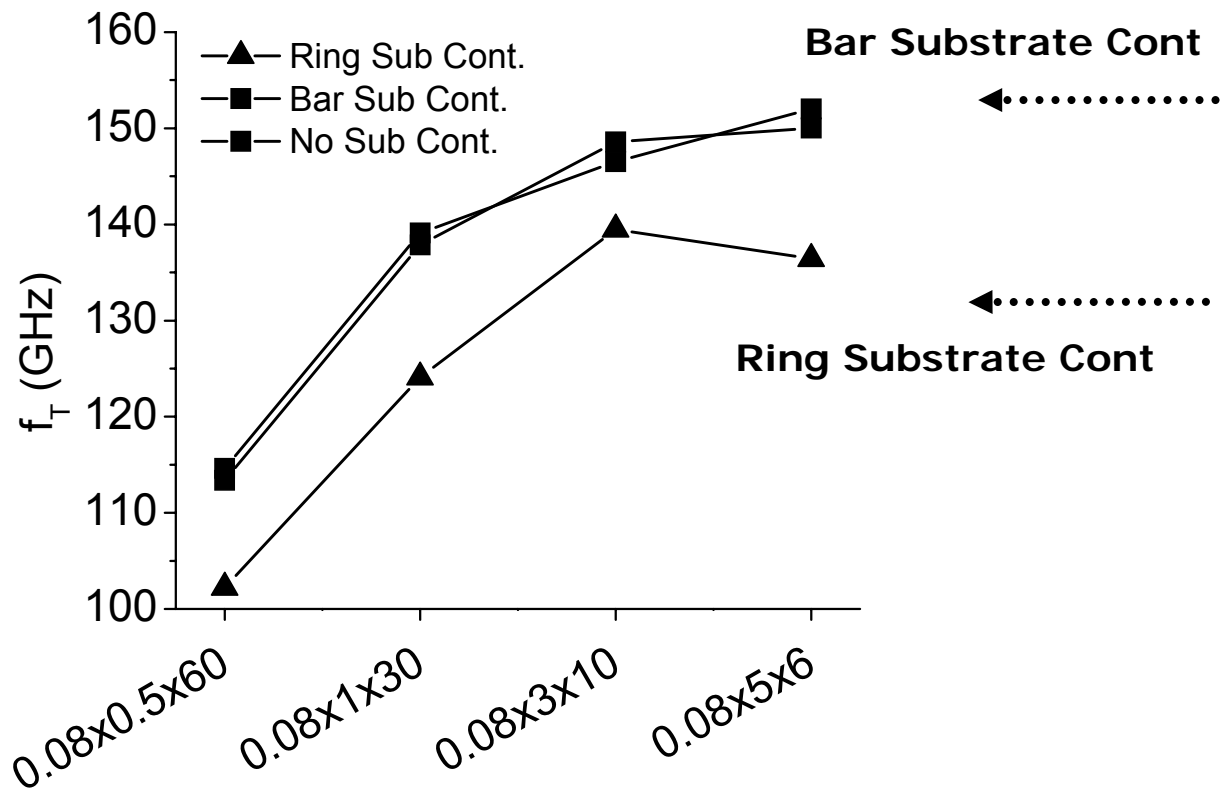


- Layouts that are not overwhelmed by parasitics
- Flexibility while targeting model accuracy
- P-cell and model should
 - be scalable within reasonable geometries
 - be consistent with parasitic extraction tools



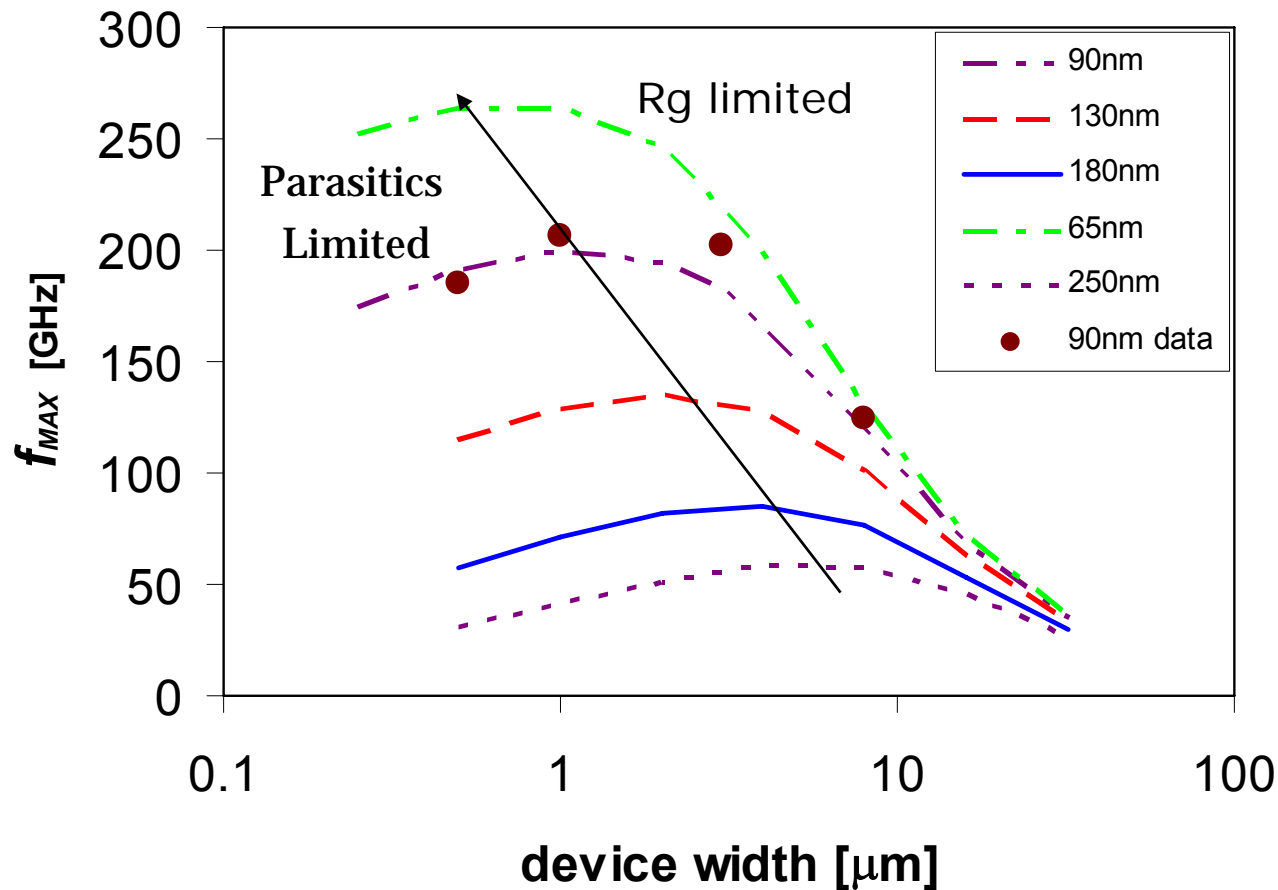
- **Performance enhancement by carefully minimizing parasitics**
 - Numerous sources of wiring parasitics
 - Parasitic influence grows every generation
- **Applications may need to balance potential trade-offs**

Parasitic Influence on f_T



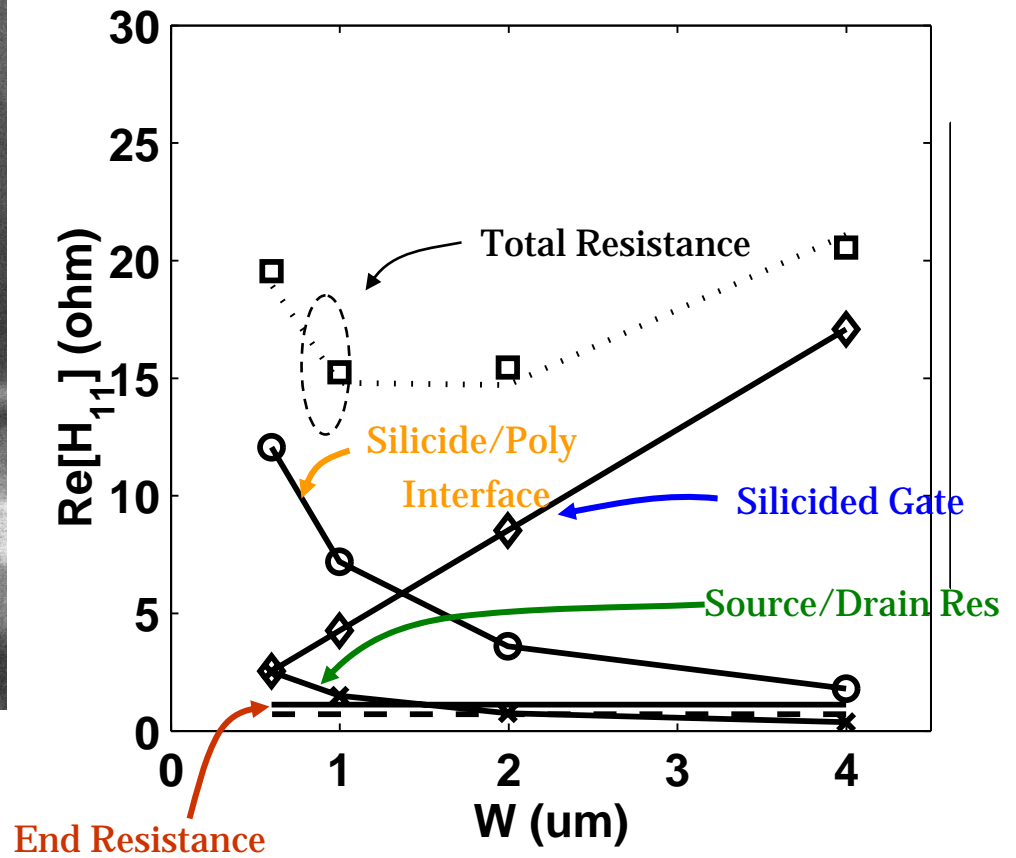
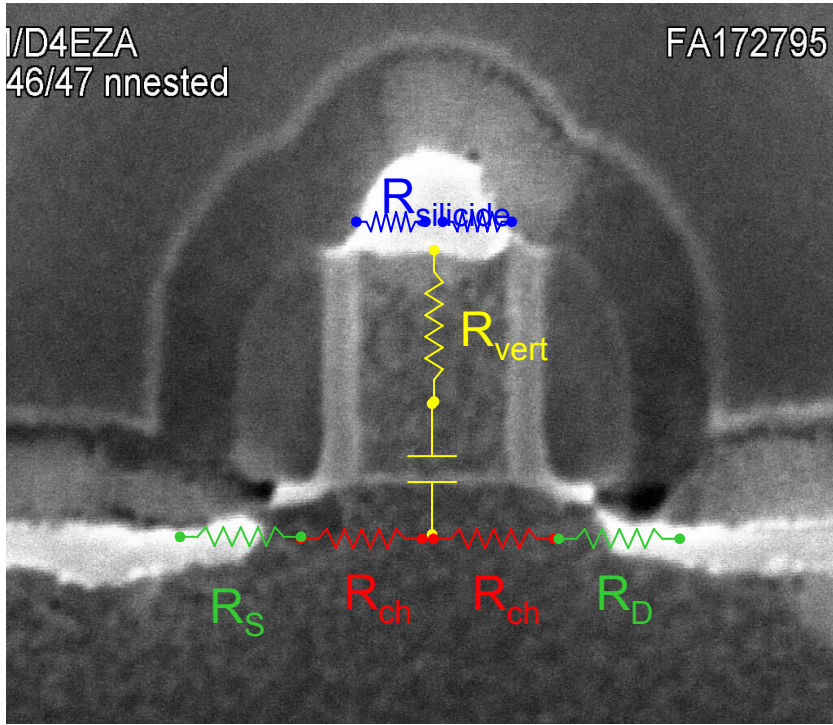
- "Close-in" capacitive parasitics significantly impact f_T
- As technology scales, optimal layout options may be quite different from "intuitive" assumptions

Parasitic Influence on f_{MAX}



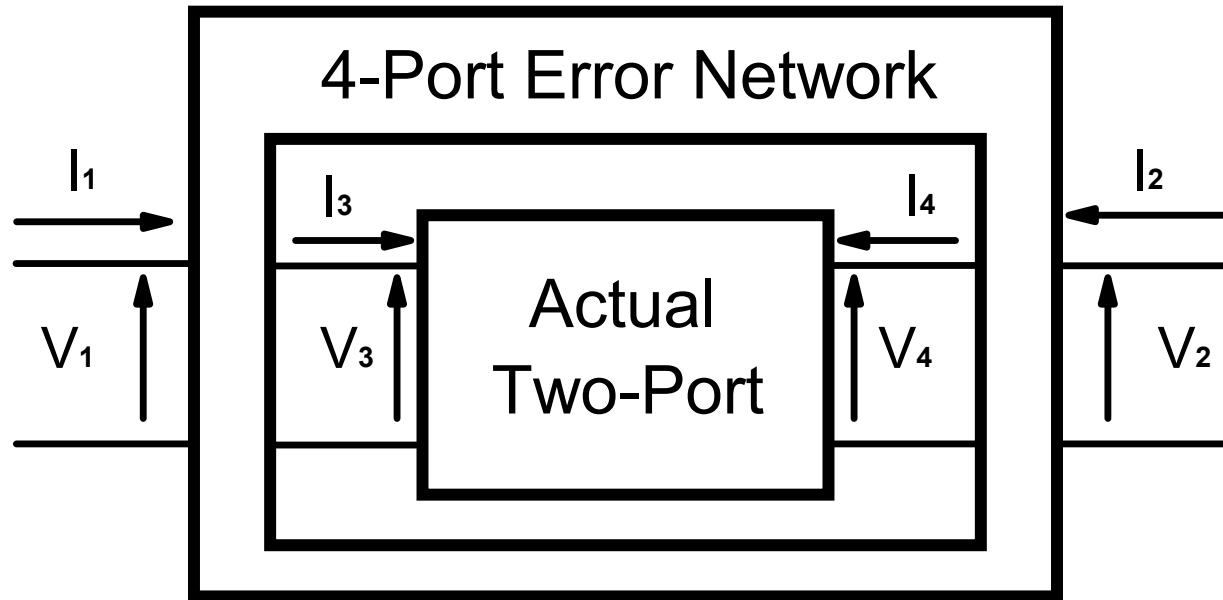
- Ideally, optimal device width should scale every generation
- f_{MAX} scaling adversely impacted by both resistive & capacitive parasitics

Optimal Device Width

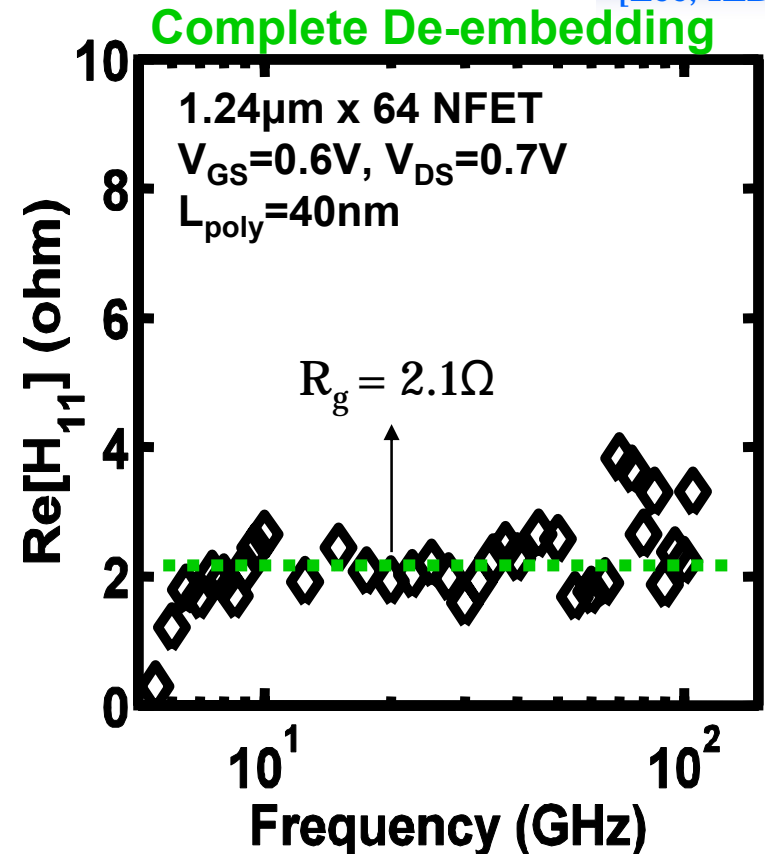
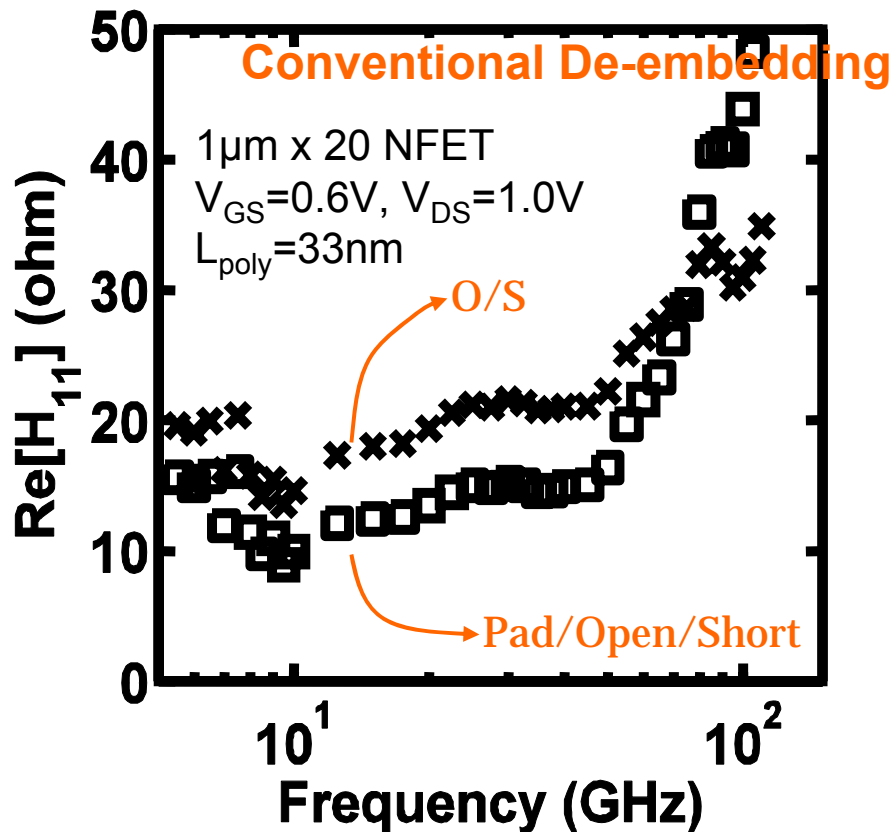


- Technology specific components could lead to high input resistance even in devices with small widths

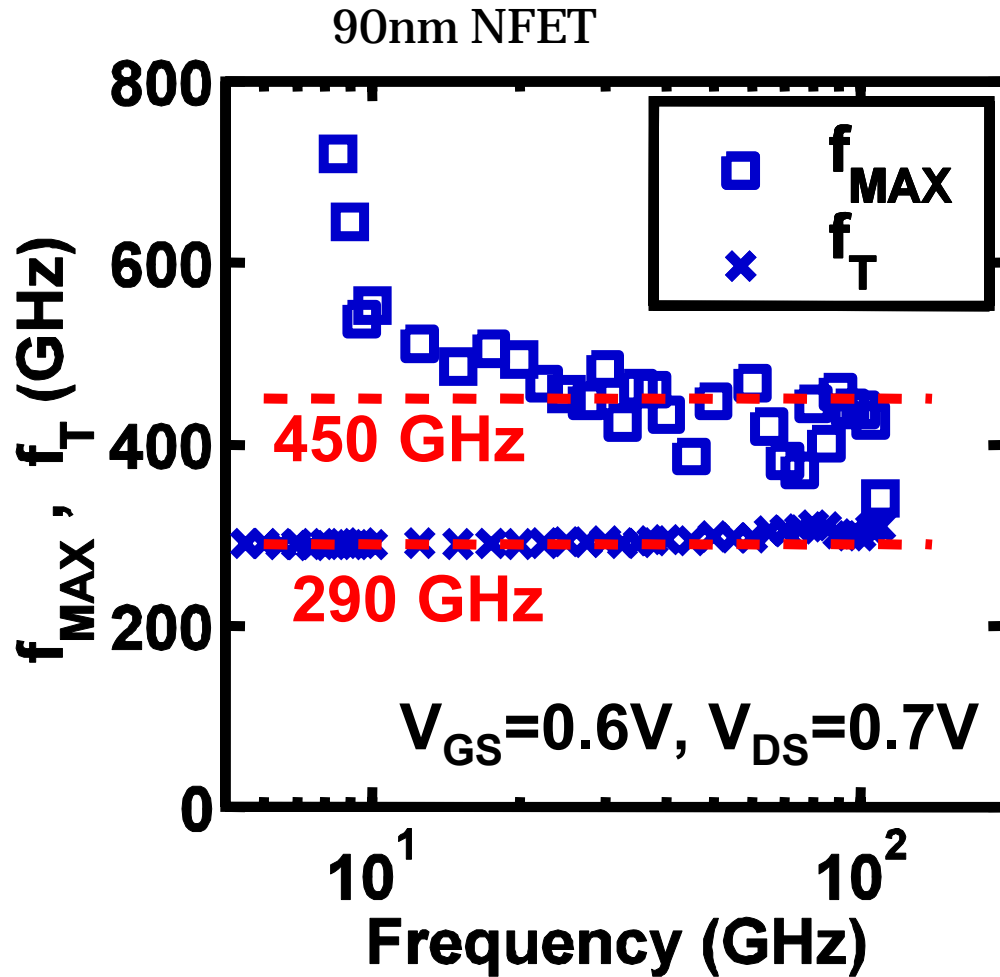
Two Port Calibration



- 16 elements of the 4-Port parasitic network explicitly determined
- Additional de-embedding standards required
 - 6 standards for a homogeneous solution
 - 4 standards, if reciprocity can be enforced



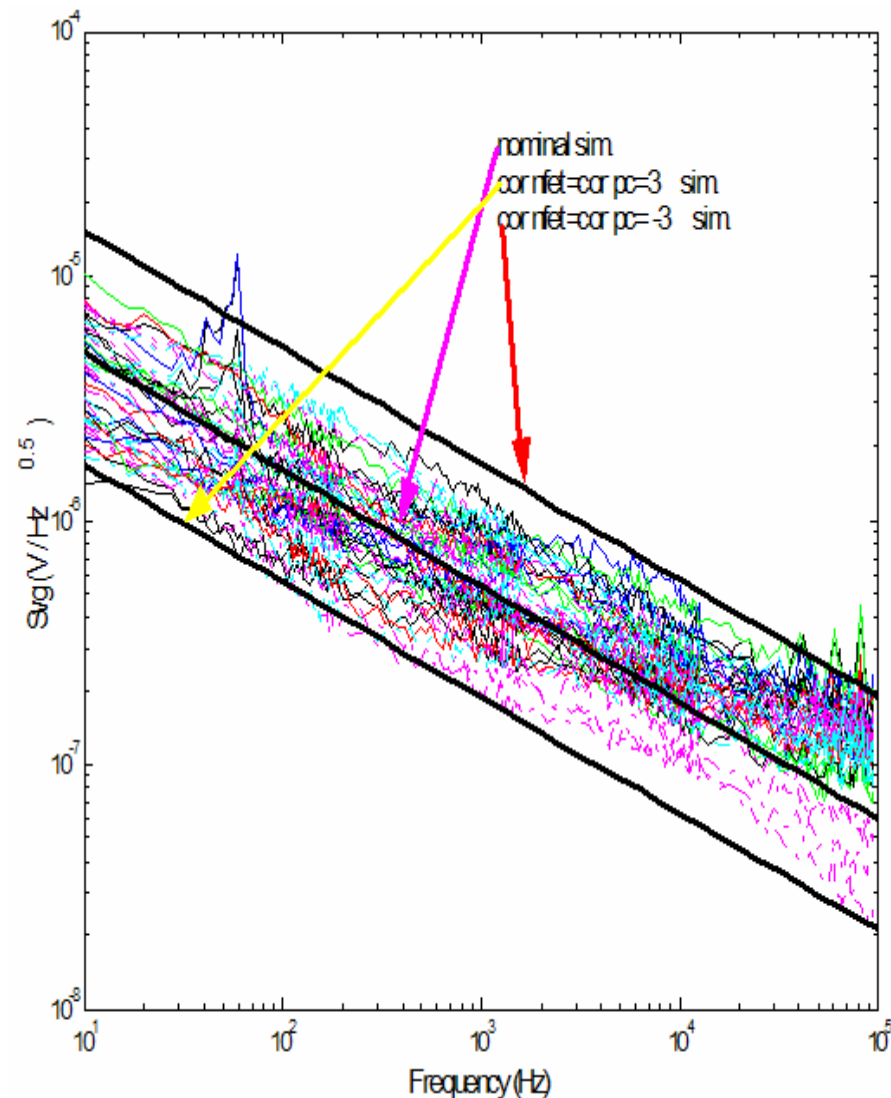
- Pad design & device layout impacts de-embedding
- Distribution of parasitics affects resistance and capacitance extraction
 - Errors could be across the whole frequency span
- Accurate extraction is possible with complete de-embedding



Intrinsic device characterized by complete de-embedding

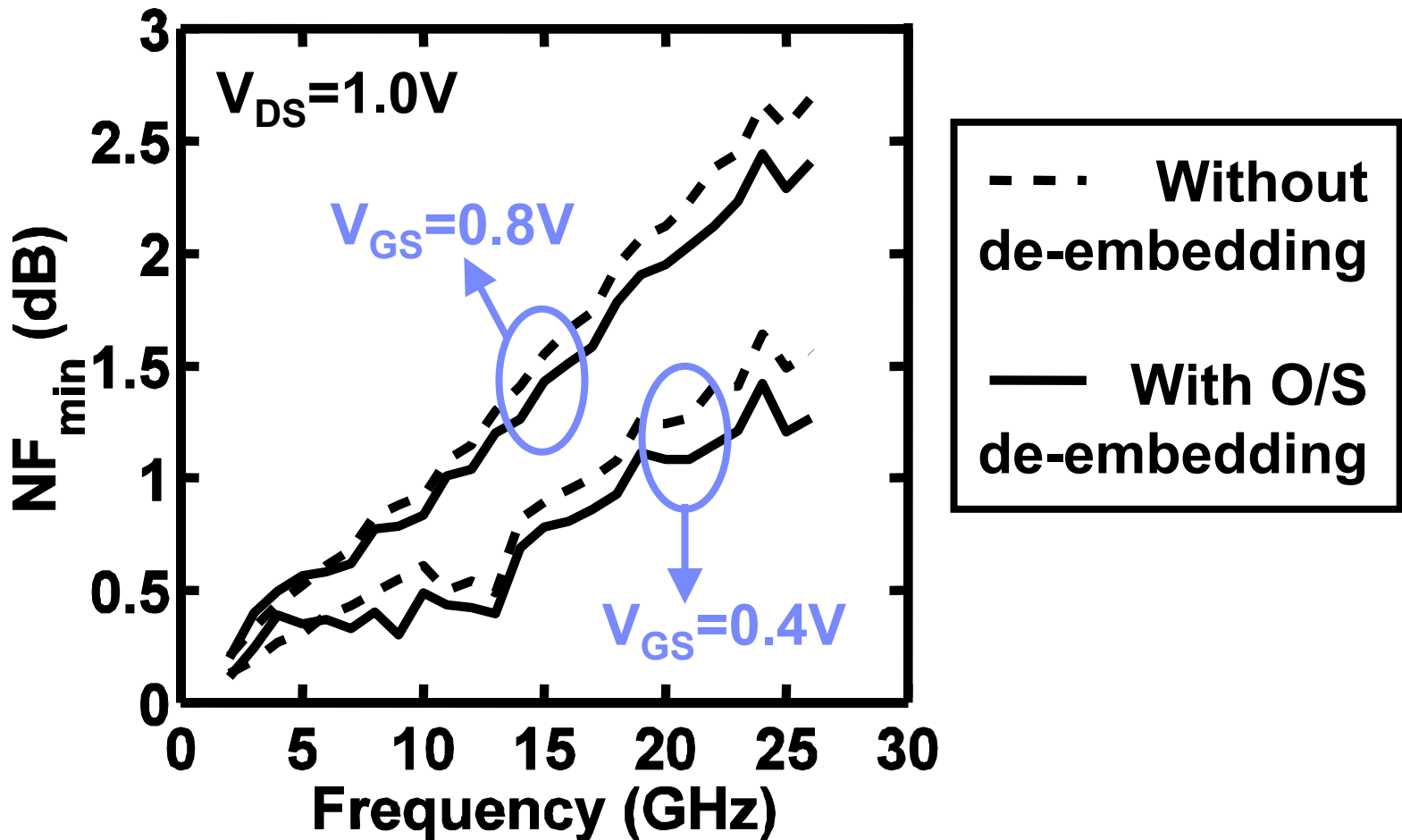
- 450GHz f_{MAX} & 290 GHz f_T for intrinsic device
- 320GHz f_{MAX} & 220 GHz f_T with wiring parasitics

- Variance of noise $\sim 1/\text{area}$.
 - **No strong bias dependence**
 - **Brederlow, et al. \Rightarrow Trap density variation**
- Add statistics to BSIM noise parameters
- Statistical noise simulations
- E.g. $0.18\mu\text{m}$ CMOS data



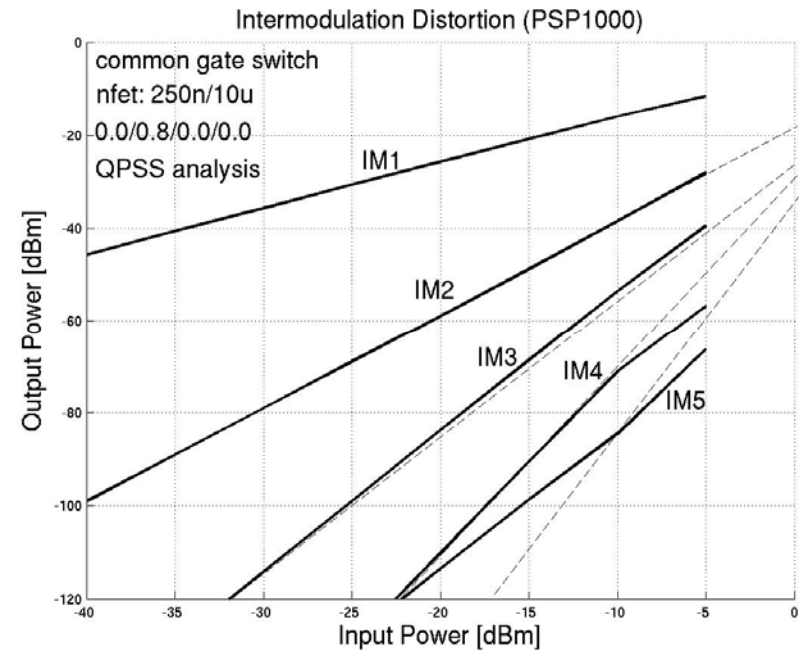
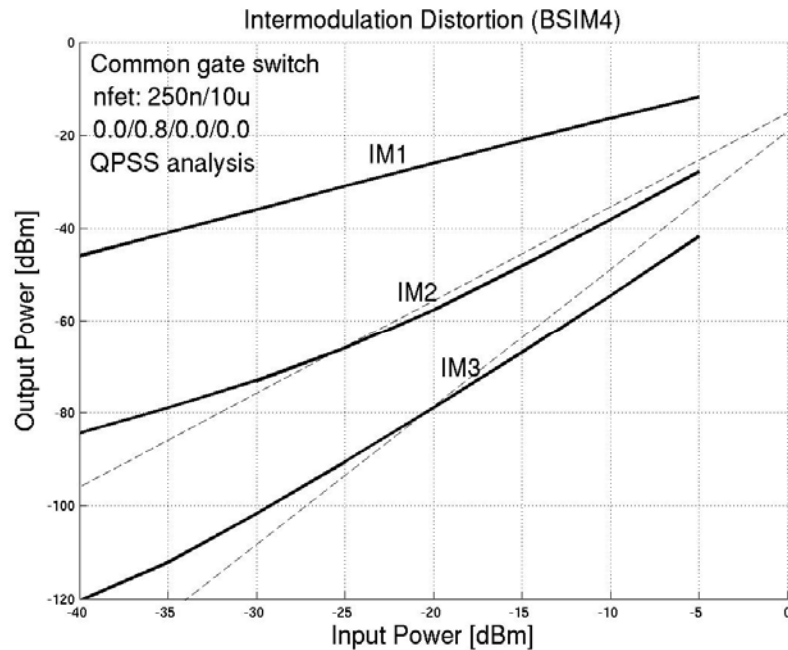
• R. Brederlow et al., IEDM 1999

RF Noise Figure



- 80 μm -wide 90-nm SOI NFET
- Well-behaved frequency dependence
- Modeled well with channel thermal noise term

Common gate switch: $V_{ds}=0$, $V_{sub}=0$.



- Discontinuities in modeled I-V derivatives affect IM simulation
- Surface potential models; improve I-V relationships*
- Limited use work-around solutions proposed

*(See Bendix, et al., CICC'04 for a good discussion)

- **Scaled CMOS is capable of supporting many emerging RF applications**
 - High levels of integration
 - Circuits benefiting from V_T & supply voltage lowering
- **RF applications present a challenge for CMOS designs**
 - FET gain limited by its g_m and g_{ds}
 - Input/Output matching contributes to power loss
- **Rich menu of features supported by schematic-based design flows**
 - Passive devices – Base & High-performance, lumped & distributed
 - One-pass design successes are common
- **Models and design tools**
 - Optimized, parasitic-aware device library
 - Accurate high-frequency parameter extraction
 - Advances in MOS model capability