



# Carbon Nanotube Transistors for Digital Circuits

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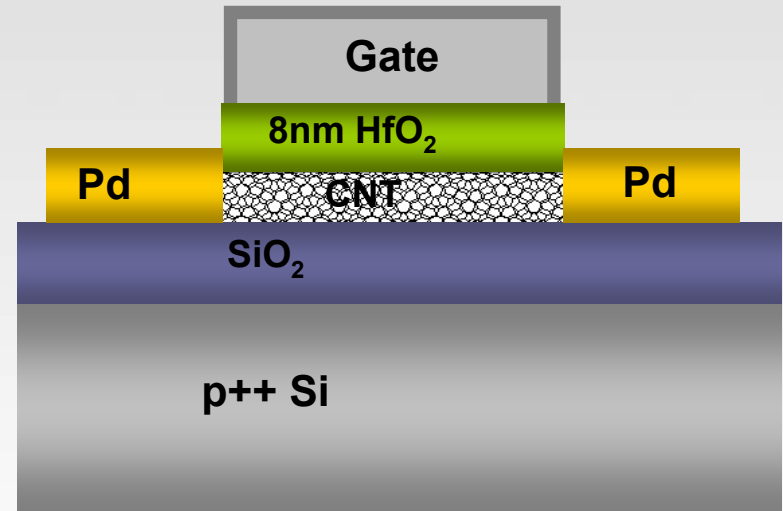
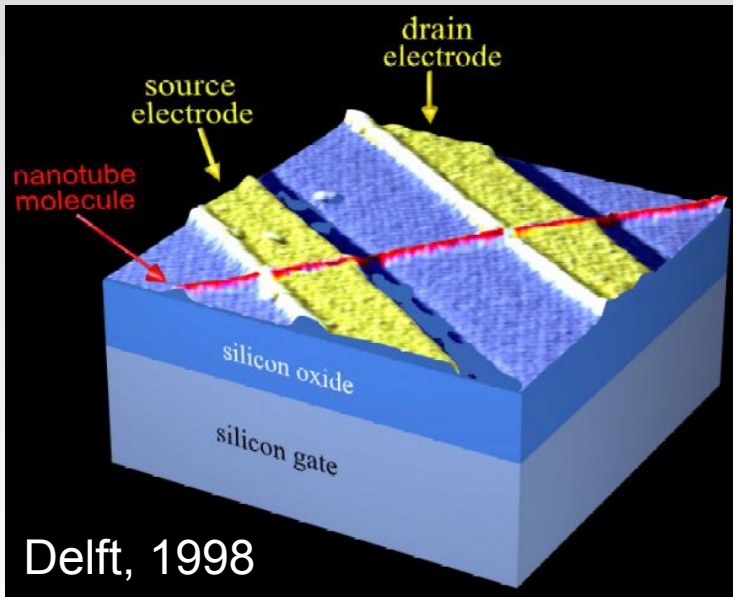


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# CNTFETs 1998 - 2005



Delft:  
Tans, et al., *Nature*, **393**, 49, 1998

IBM:  
Martel et al., *APL*, **73**, 2447, 1998

Javey, et al., *Nano Letters*, **4**,  
1319, 2004



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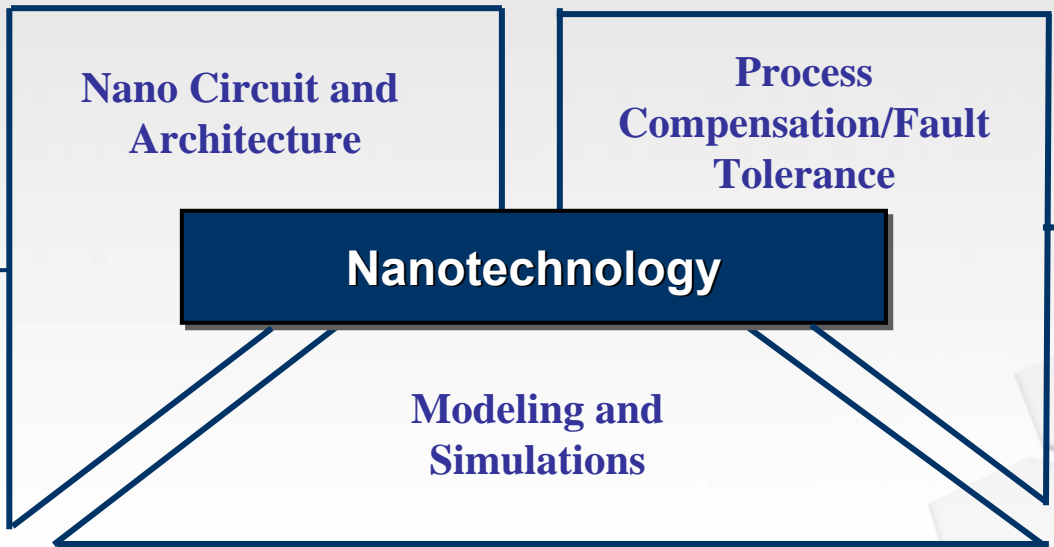
# Nanotechnology: Modeling & Circuit Architecture

## Circuit Simulations of Carbon Nanotube FETs

- *Ballistic FETs : Circuit Performance*
- *Schottky Barrier FETs : CMOS-like Applications*

**Nanometer Scaled Ckts & Interconnects**

- *Performance Estimation*
- *Power Est. & Low-Power Des.*



## Dynamically Reconfigurable Cache Design

- *Analysis*
- *Optimization*

## Ballistic Carbon Nanotube FETs

- *SPICE Compatible Modeling*
- *Schottky barrier FETs*



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# CNFETs for Circuit Simulations

- ***Development of a framework for simulation and performance/power estimation of non-silicon devices/circuits/systems is essential.***
- ***This will guide not only the device optimization but also facilitate development of novel circuit techniques for CNFETs.***



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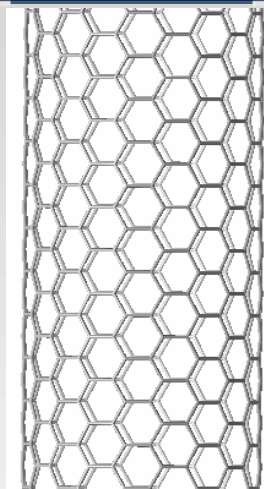
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# Circuit Simulation Strategies

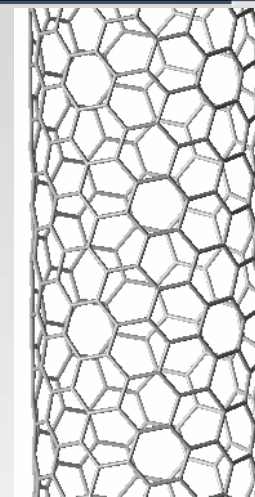
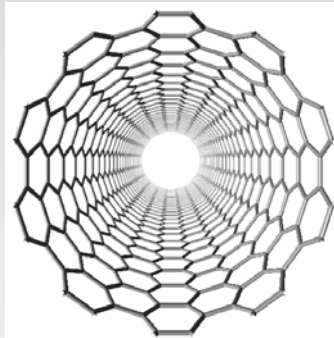
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1. A top-of-the-barrier circuit compatible model for MOS CNFETs (Purdue).
2. A mixed mode simulation environment consisting of an NEGF treatment of CNFETs (Purdue) and a circuit simulator, for both MOS CNFET and SB CNFET.

# Carbon Nanotubes: Structure & Synthesis

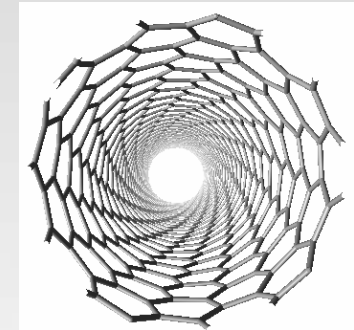


Metallic



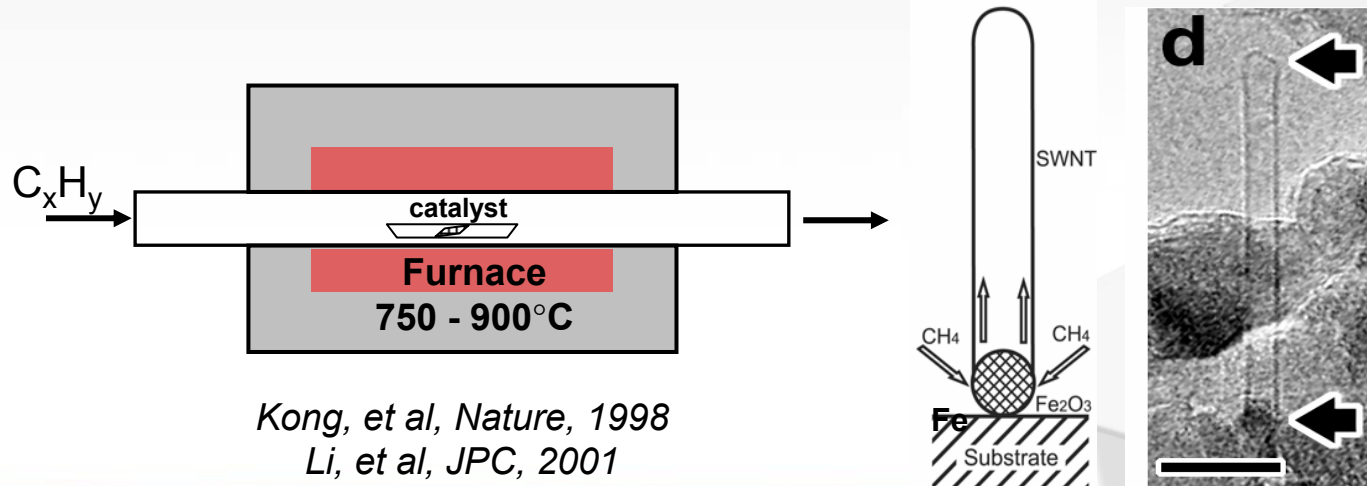
Semiconducting

$$E_G \approx 0.8eV/d(\text{nm})$$



Diameter (d): ~ 0.5-5 nm, Length: ~ 10 nm - 10 cm

## Growth: Chemical Vapor Deposition



# Three Types of CNFETs: (a) SBFET

SBFET

gate

source

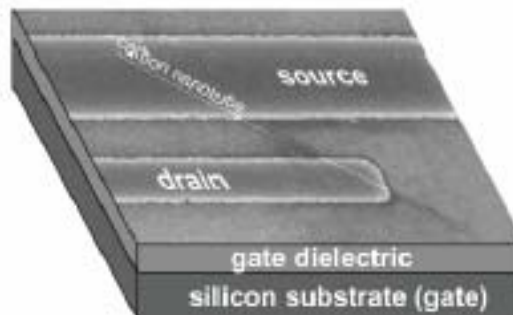
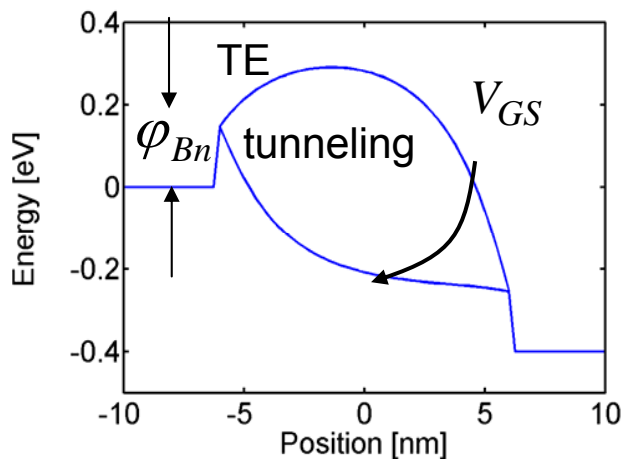
drain



metal

i or p<sup>-</sup>

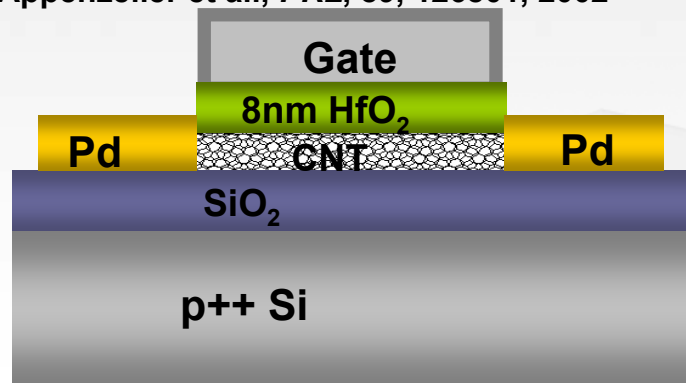
metal



“Carbon nanotubes as Schottky barrier transistors”

Heinze et al., *PRL*, 89, 106801, 2002

Appenzeller et al., *PRL*, 89, 126801, 2002

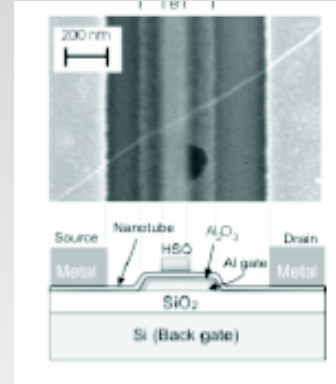
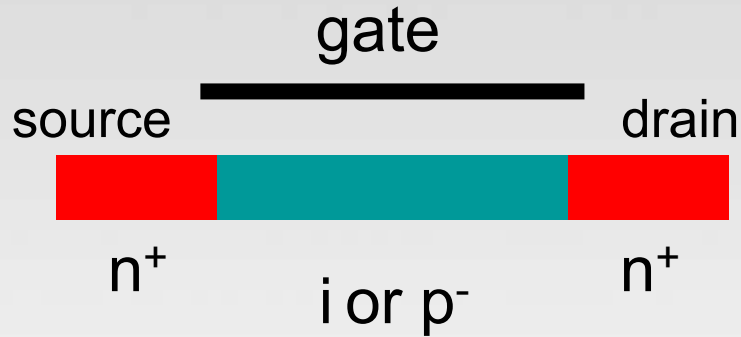


Javey, et al., *Nano Letters*, 4, 1319, 2004

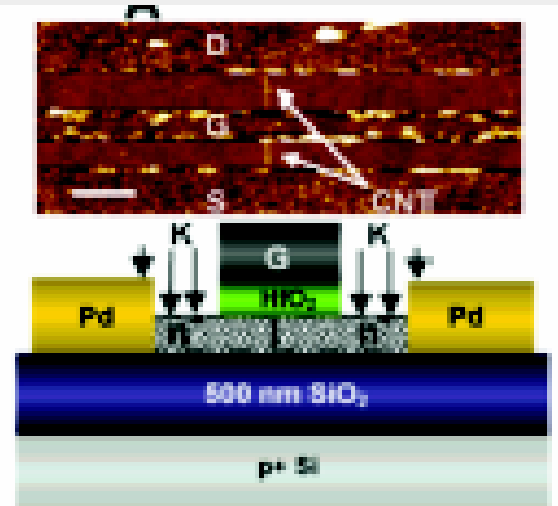
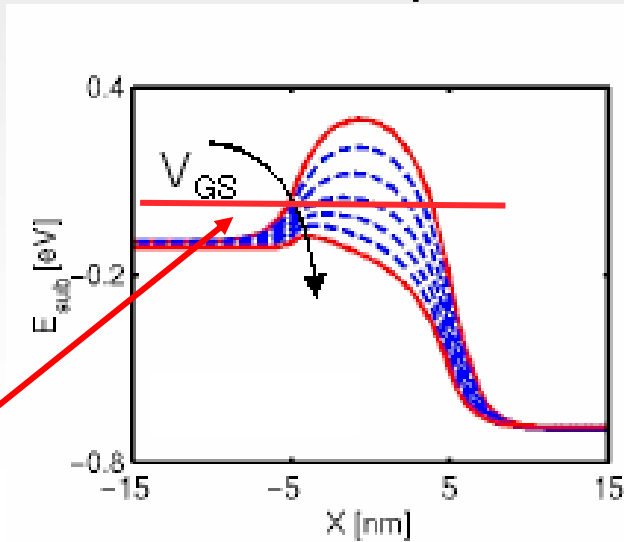
**Tunneling limited current. Gate electrostatics will control the tunneling barrier.**

# Three Types of CNFETs: (b) MOSFET

MOSFET



Appenzeller et al.,  
IEDM, 2004

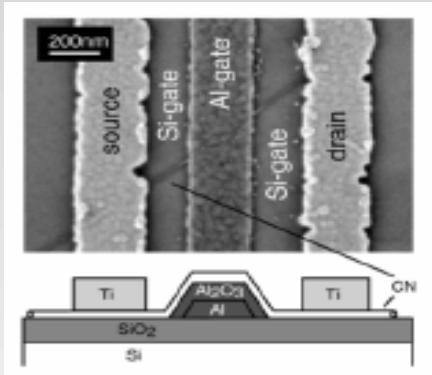
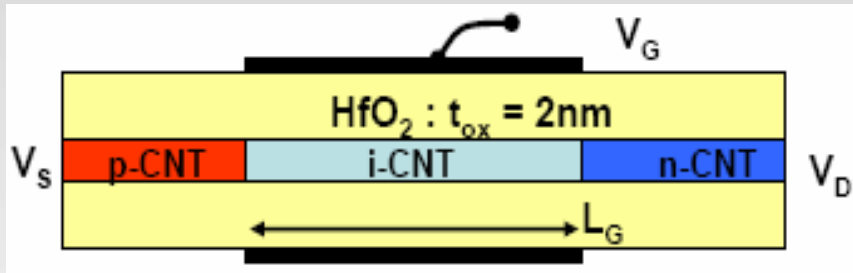


Javey et al., Nano  
Letters, 5,2, 2005

**Electrons do not see any tunneling barrier in the “on” state.  
Gate electrostatics control the top-of-the-barrier.**

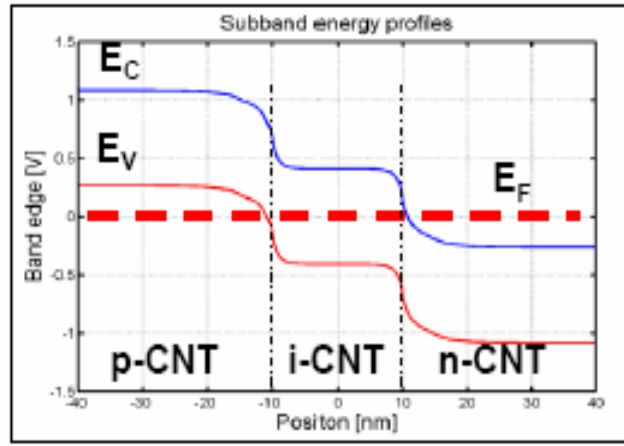
# Three Types of CNFETs: (c) BTBT FET

## BTBT FET

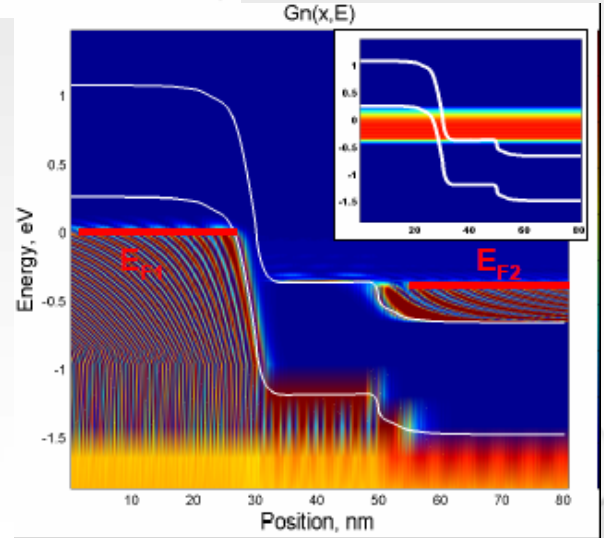


Appenzeller, PRL, vol 93, 19, 2005

Ineffective tunneling barriers.



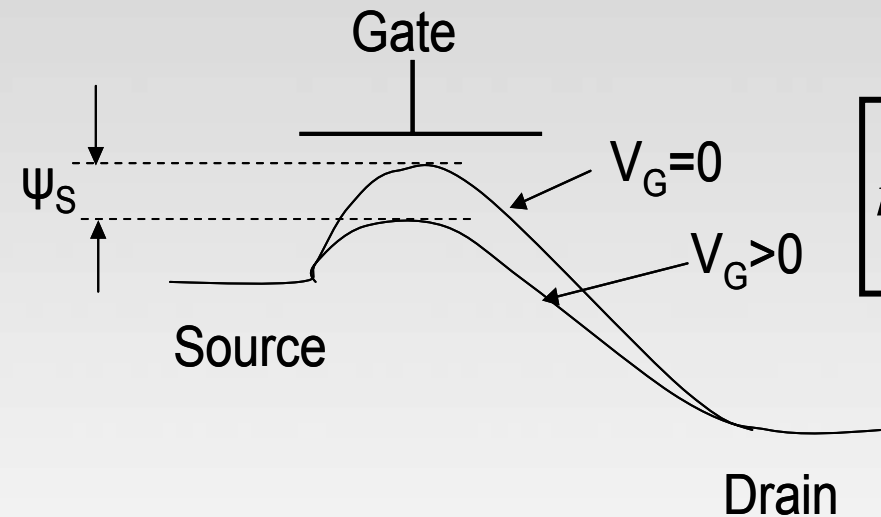
Simulation studies, Lundstrom, IEDM, 2005



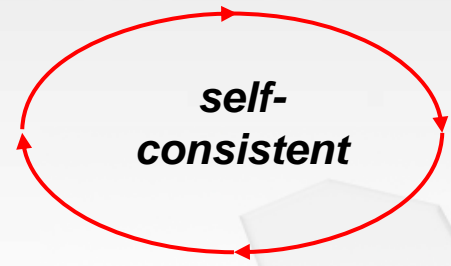
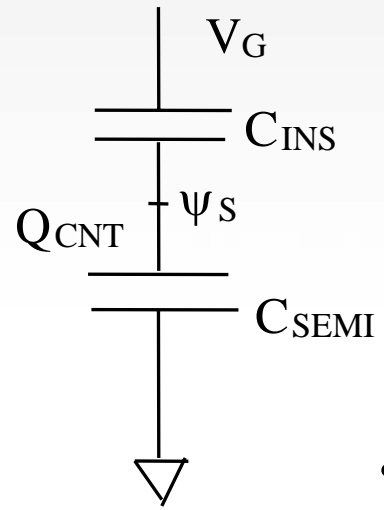
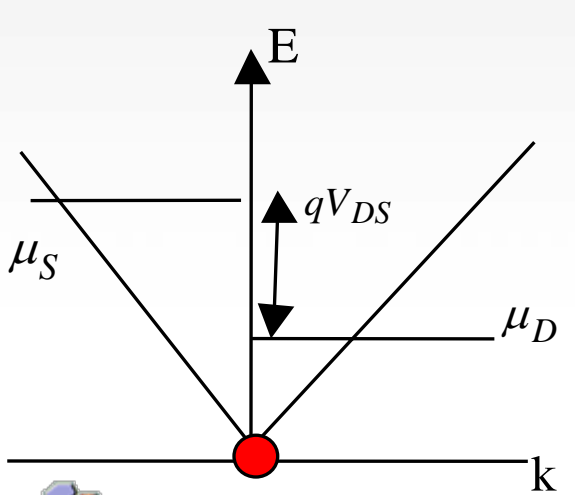
**Electrons tunnel from valance band to conduction band.  
Gate electrostatics control the bands in the intrinsic region.  
Not limited by thermionic emission.**



# Ballistic CNFETs with 1D Electrostatics



$$n_{CNT} = \int_{E_C}^{+\infty} \frac{D(E)}{2} [f(E - \mu_S) + f(E - \mu_D)] \cdot dE$$



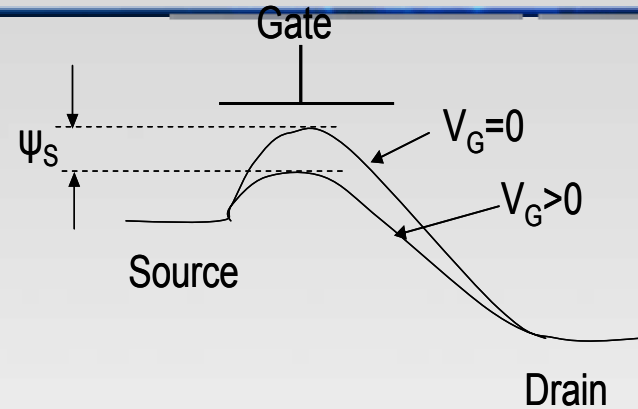
$$\psi_s = V_G - \frac{Q_{CNT}}{C_{INS}}$$

•  $I_{DS}$  is determined by  $\psi_s$

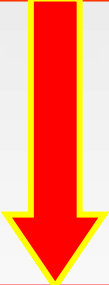


# A top of the barrier model: The SPICE Equivalent

Assumes 1D electrostatics and ballistic transport



Obtain  $\psi_S$  as analytical functions of  $V_{ds}$  and  $V_{gs}$ .

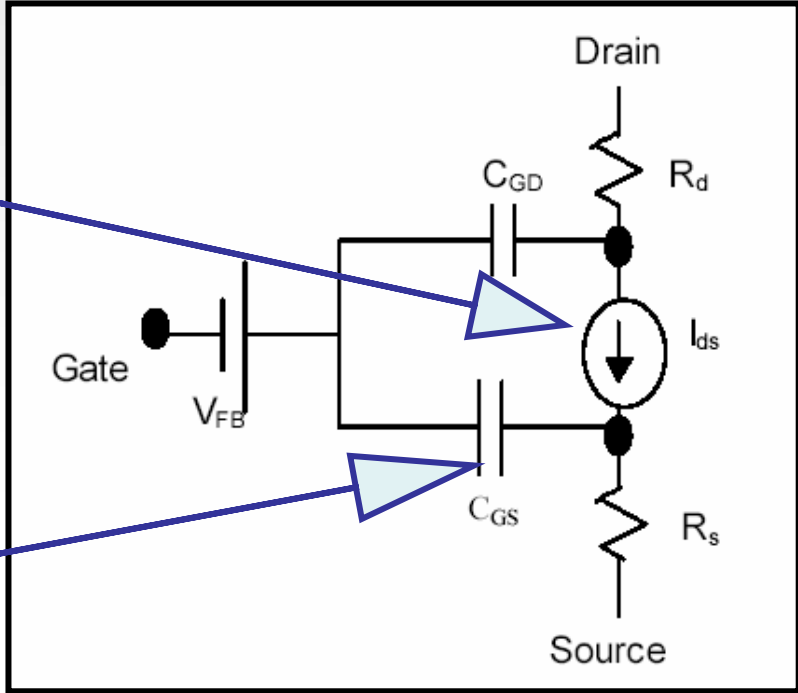


Compute 1D current from  $\psi_S$ .

Obtain the drain and source charges from  $V_{ds}$  and  $V_{gs}$ .



Differentiate charge w.r.t.  $V_g$  to obtain gate capacitors.



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# Designing with CNFETs

- Use of high K dielectric gives better gate control.
- High mobility gives higher *Ion*
- The intrinsic device shows several Tera Hertz of ring oscillator frequency.

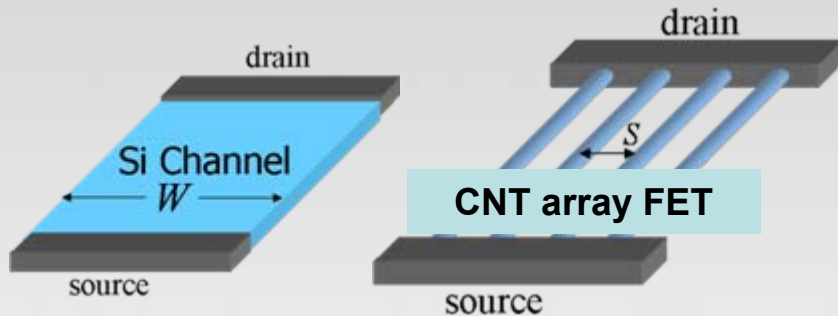


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# Back of the Envelope Calculations

## Current



$$I_{\text{per tube}} \sim V_{DD} / 6.5 \text{Kohms}$$

$$\sim 150 \mu\text{A} (@V_{DD} = 1\text{V})$$

$$\text{Take } d = S = 1\text{nm};$$

$$I_{\text{per gate width}} \sim 500 \times 150 \mu\text{A}/\mu\text{m}$$

$$\sim 75 \text{mA}/\mu\text{m} \text{ (+non-idealities)}$$

$$I_{\text{silicon}} \sim 1 \text{mA}/\mu\text{m}$$

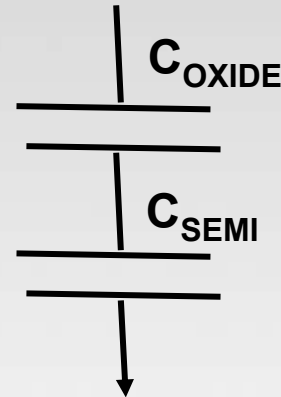
$$T_D = \frac{CV_{DD}}{I_{ON}}$$

$$C (/ \mu\text{m}) = 1\text{X}$$

$$I (/ \mu\text{m}) = 50\text{X}$$

$$T_{\text{DELAY}} \text{ (for same Tx widths)} = 0.02\text{X}$$

## Capacitance



**Physics:** Low DOS makes band pinning difficult.

**Intuitively:** Not enough electrons to screen the gate E-field.

**Circuits:**  $C_{\text{OXIDE}} > \sim C_{\text{SEMI}}$

$$C_{\text{per tube}} < \sim 1\text{-}5 \text{ aF} \text{ (@Length=50nm)}$$

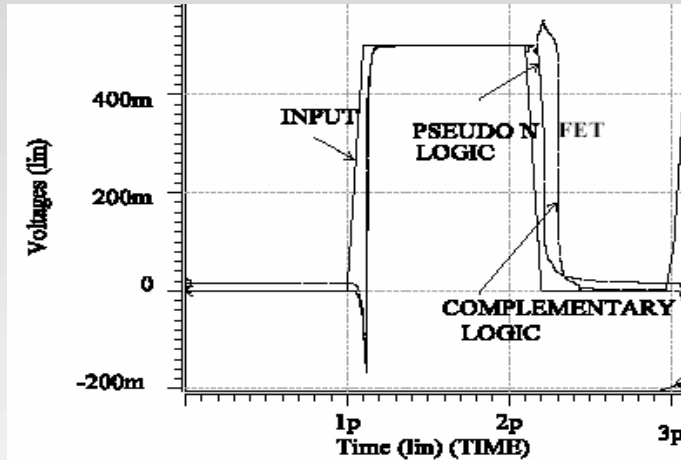
$$C_{\text{per gate width}} \sim 500 \times 2 \text{aF}/\mu\text{m} \sim 1 \text{fF}/\mu\text{m}$$

$$C_{\text{silicon}} \sim 1 \text{fF}/\mu\text{m}$$

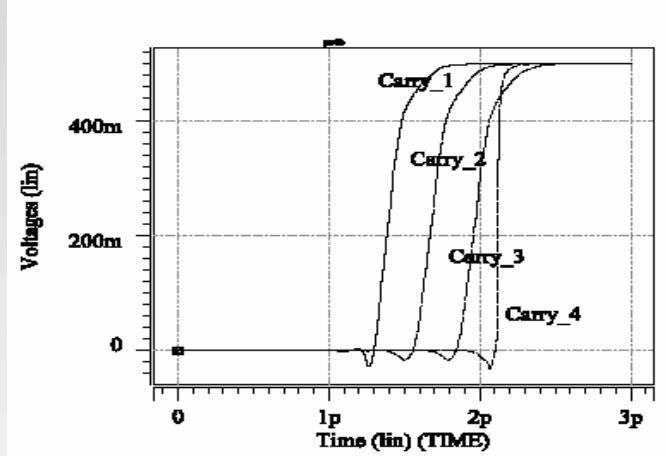
$$C_{\text{interconnect}} \sim 0.3 \text{fF}/\mu\text{m} \text{ (does not scale)}$$



# CNTFET Simulations : Intrinsic Device Performance



Wide I/P OR gate



Ripple carry adder

- Simulations of digital logic blocks have been done and performance of CNFETs has been evaluated ([tool will be available at the Purdue Nanohub](#))
- Parasitics will play an important role.
- Ultra high integration density providing more than 10X area reduction – power density can be high!



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# Issues in CNFET-based Digital Design

- High power and power density
- High defect density



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# Ultra-Low Power Techniques

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- Subthreshold operation
- Multi-valued operation
- Energy recovery

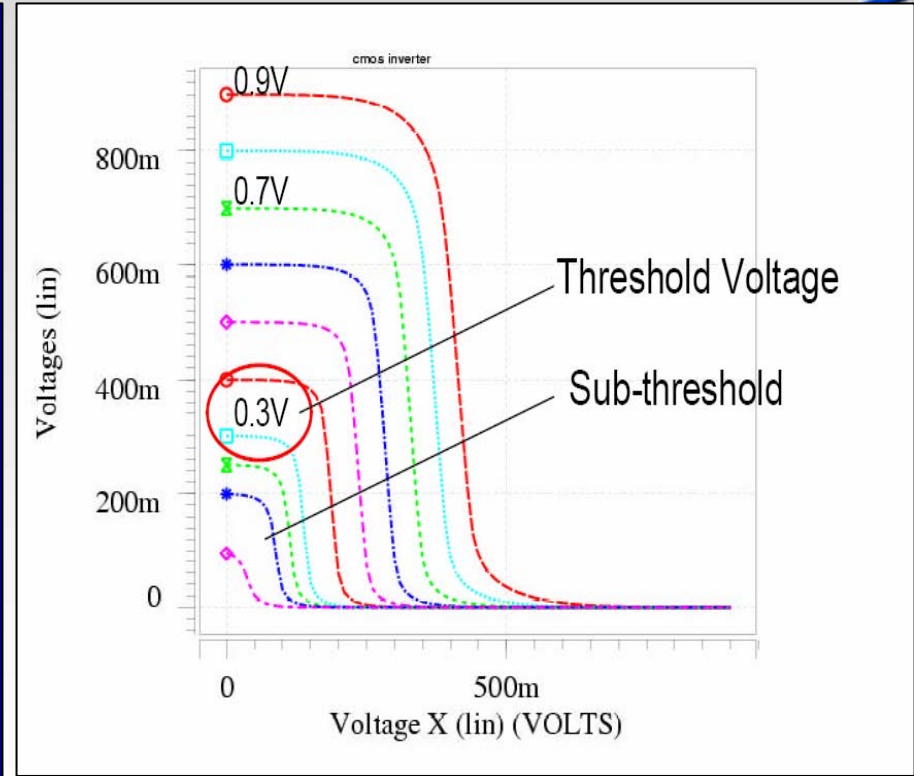
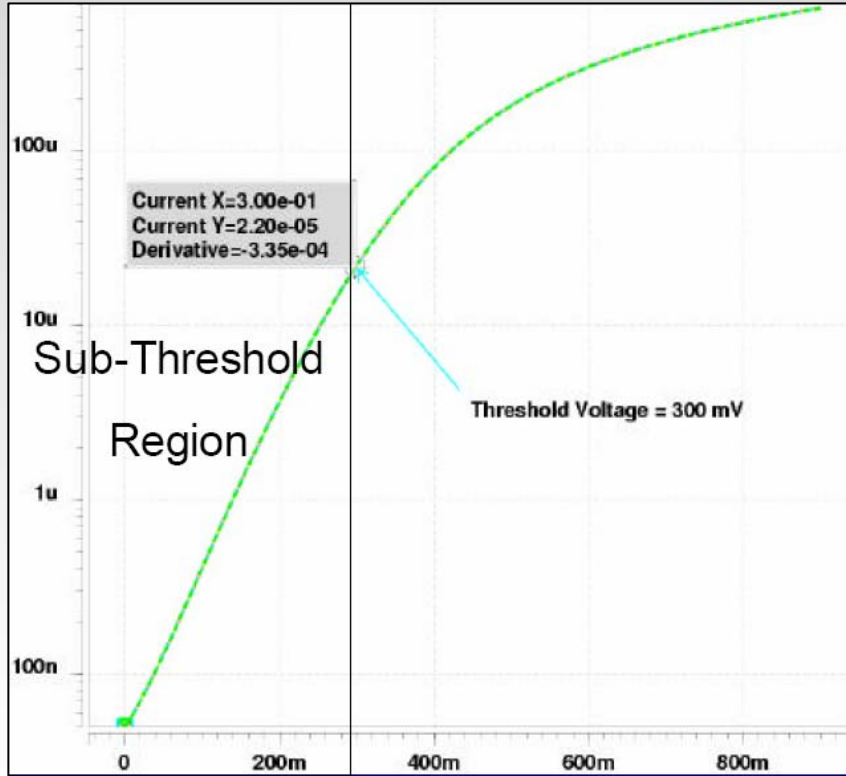


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# Digital Subthreshold Operation



- Lower currents and lower capacitance
- Transfer characteristics are sharper.



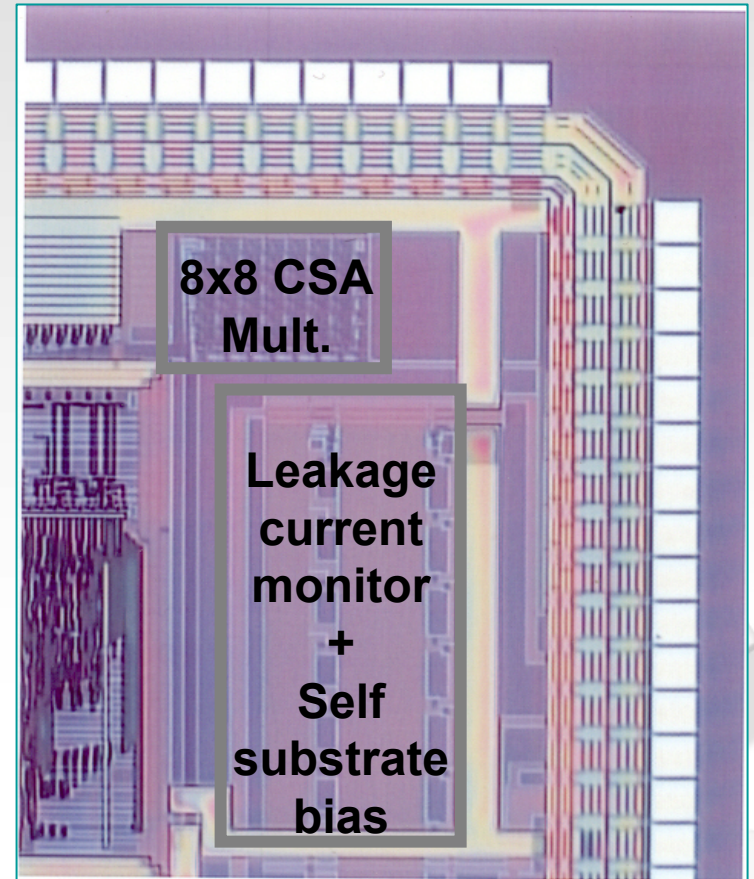
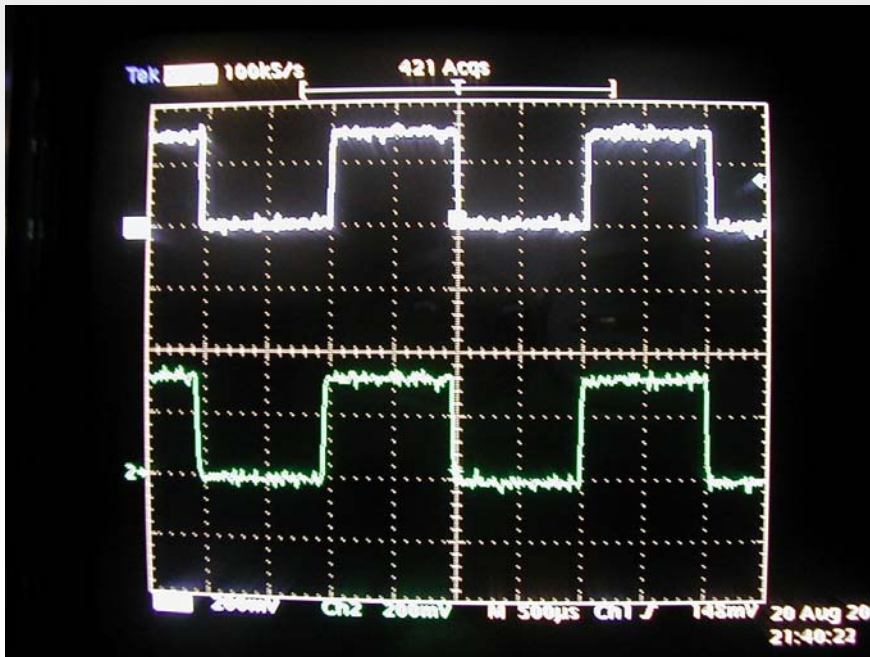
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# Si Subthreshold Operation Works!

- TSMC 0.35um
- 72 I/O pins, 84 PGA package
- Vdd=300mV
- Leakage current monitor
- Self-substrate bias

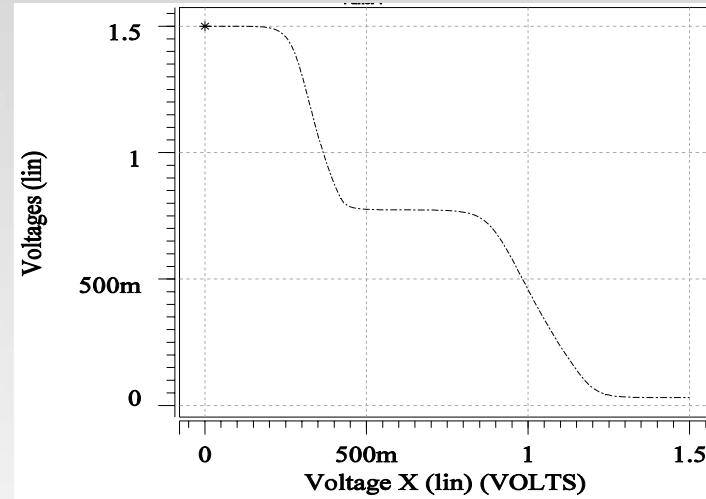
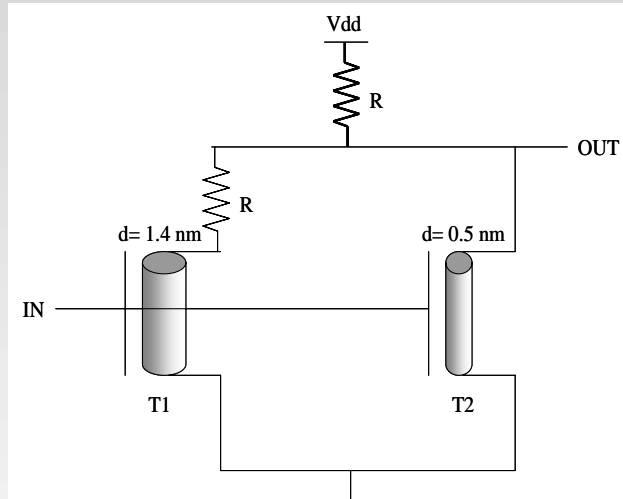


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# Multi-valued Logic for Lower Power



## A Ternary Inverter and its Voltage Transfer Characteristics

- The nanotube diameter determines the bandgap and hence the threshold voltage of the device.
- Dual diameter (and hence threshold voltage) can be used to design a novel multi-valued logic family

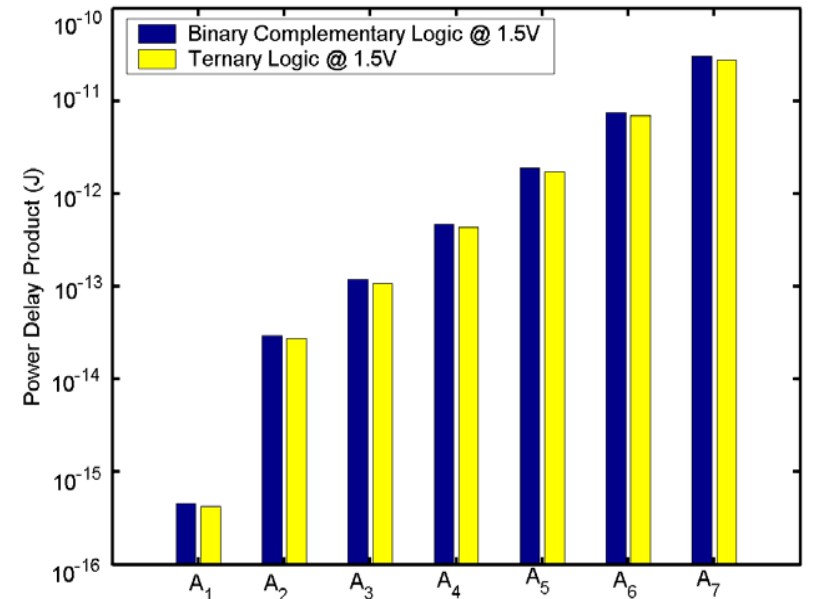
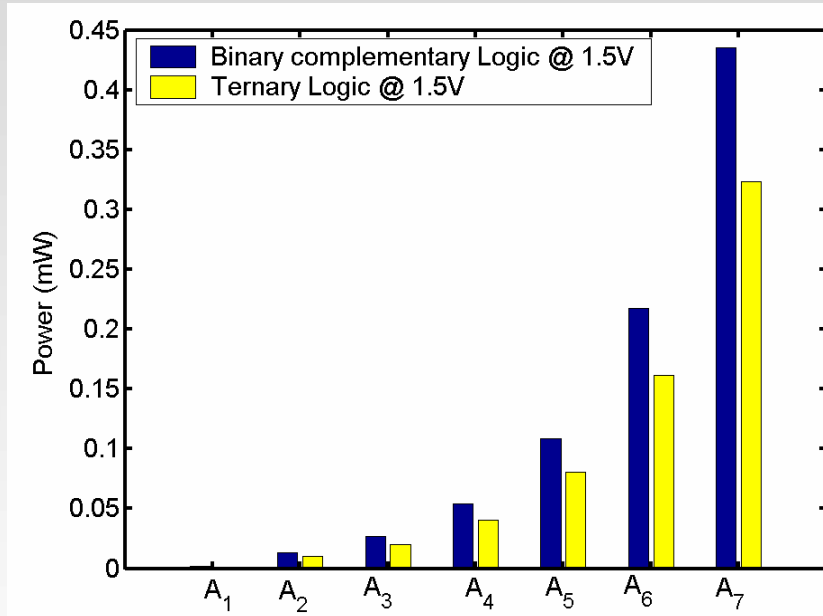


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# Multi-valued Logic



- Simulations show that the power consumption of the proposed logic family is lower than the binary logic family at iso-performance

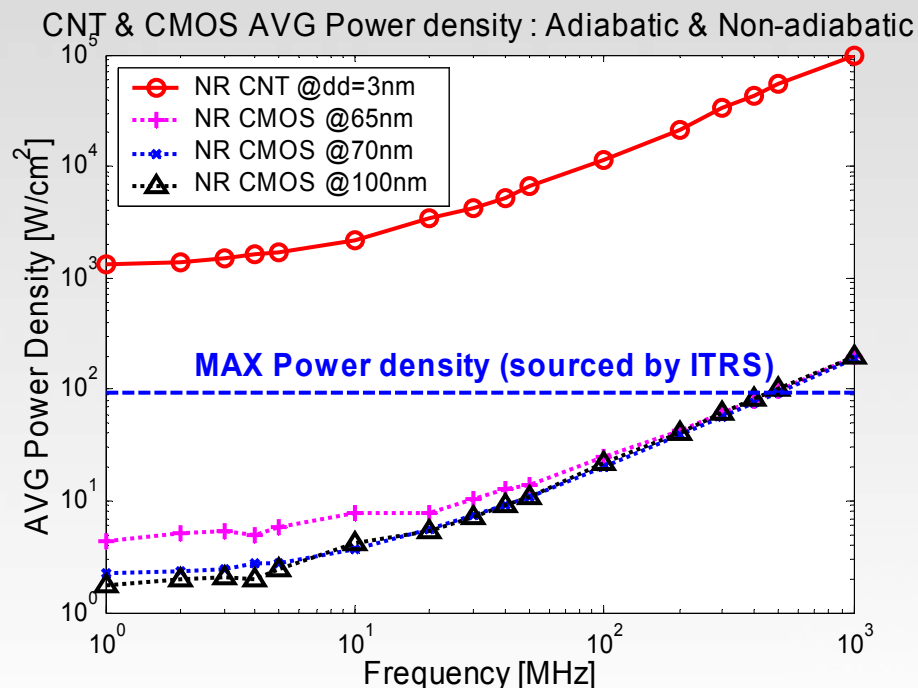


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# Energy Recovery for On-Chip Power Density Reduction



- High integration density and high current density would aggravate the problem of extreme on-chip power density in nano-scaled technologies

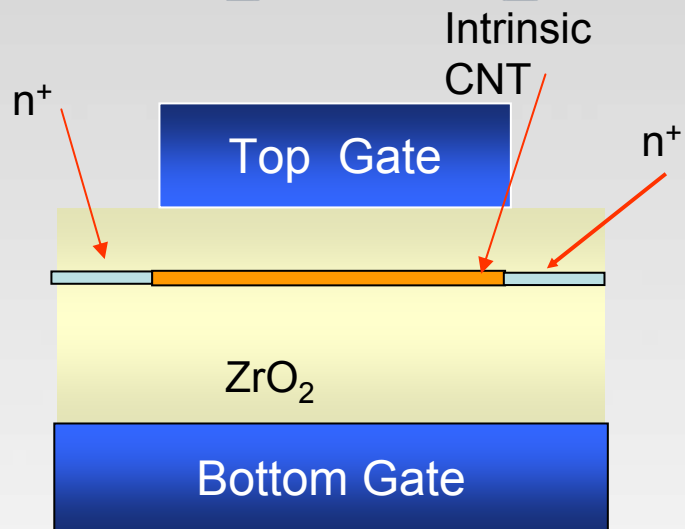


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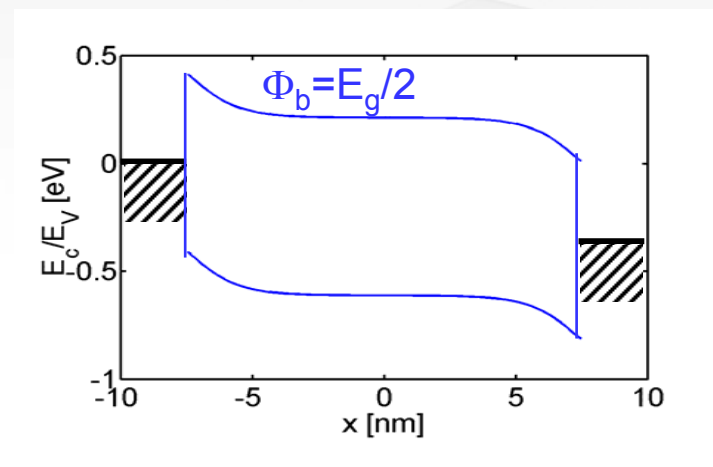
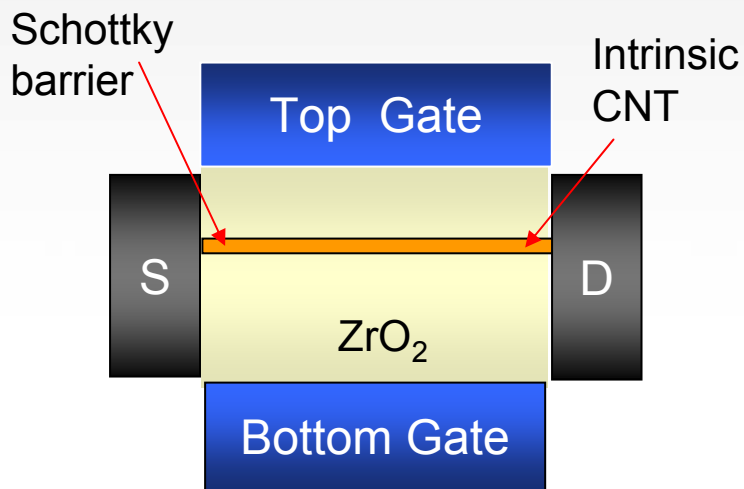
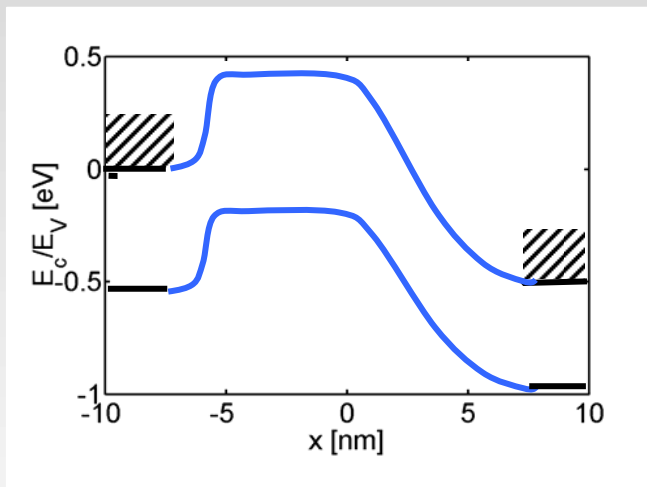
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# Carbon Nanotube FETs



### Band Diagram

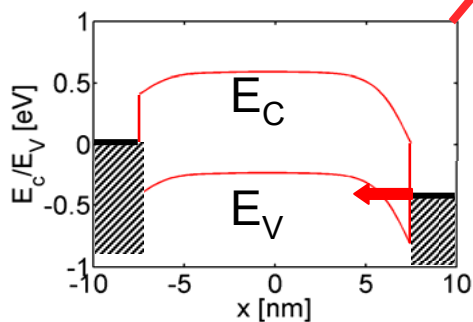
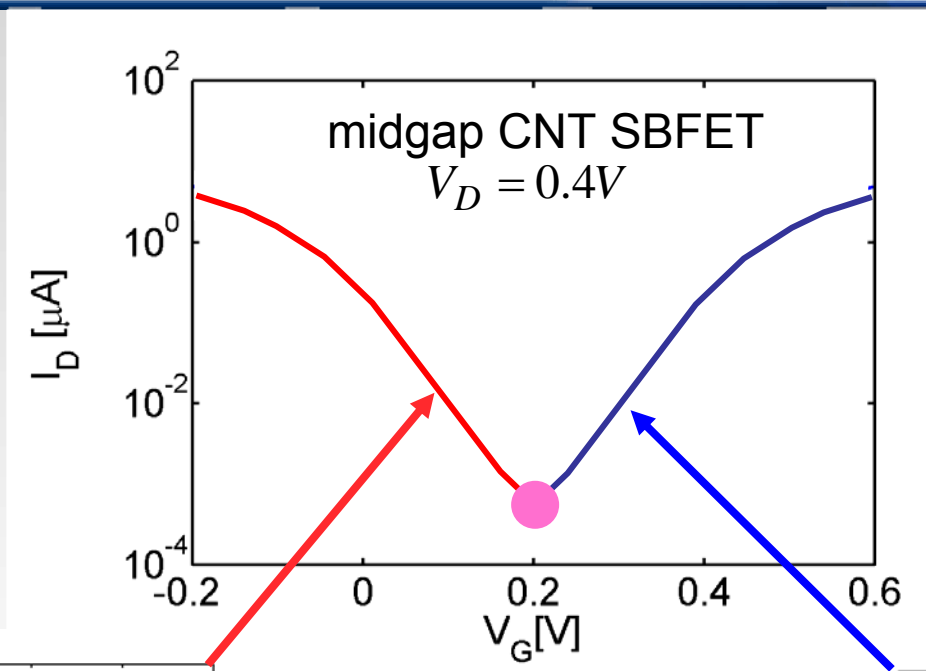


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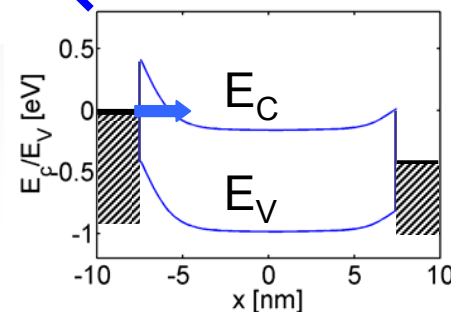


# CN SBFET: Ambipolar Conduction



$$V_G < V_D/2$$

**hole conduction**



$$V_G > V_D/2$$

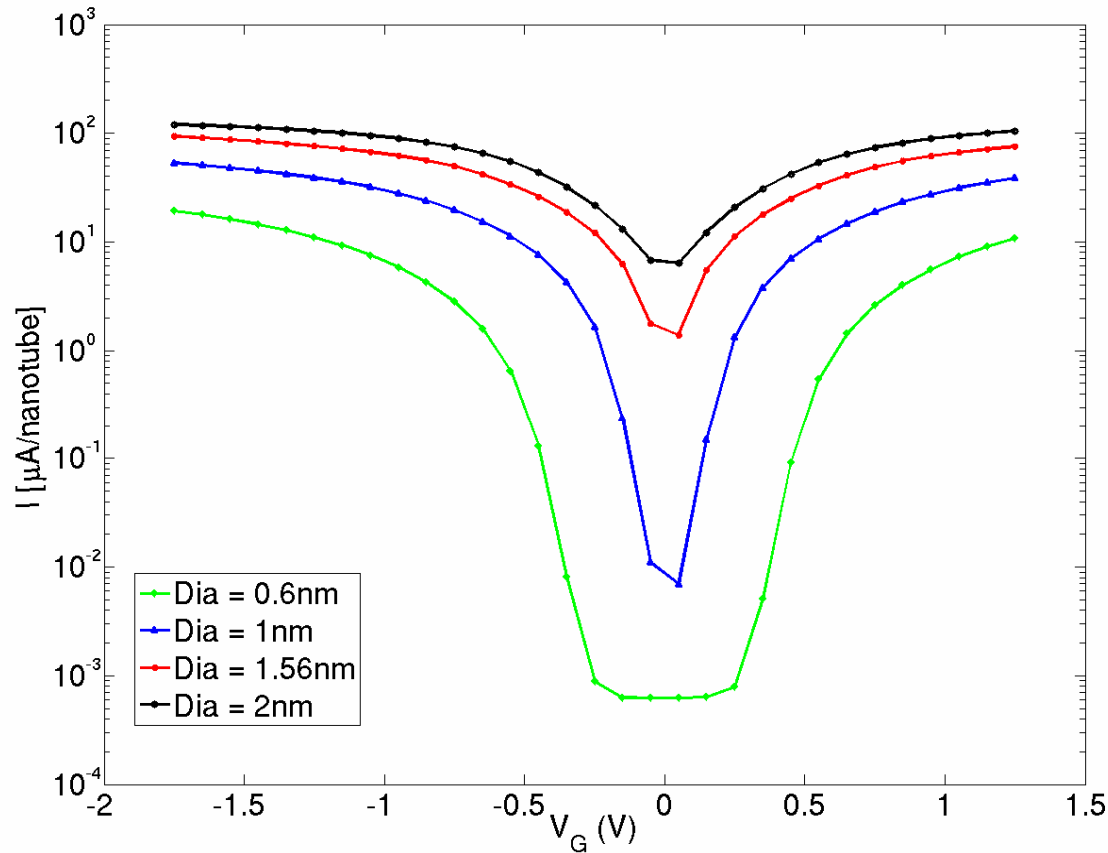
**electron conduction**



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# $I_{DS}-V_{GS}$ as a function of diameter



Top-gated structure

CNT Dia = 1.0 nm

$T_{\text{OX}} = 2$  nm

Oxide:  $\text{HfO}_2$

S/D material: Mid-gap SB

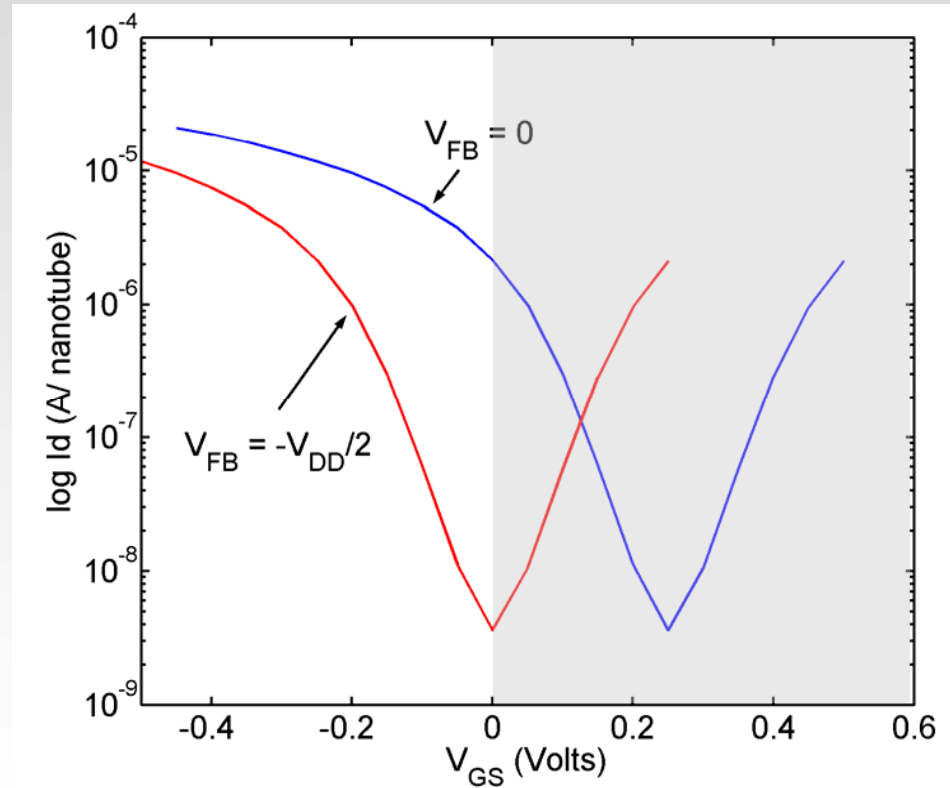
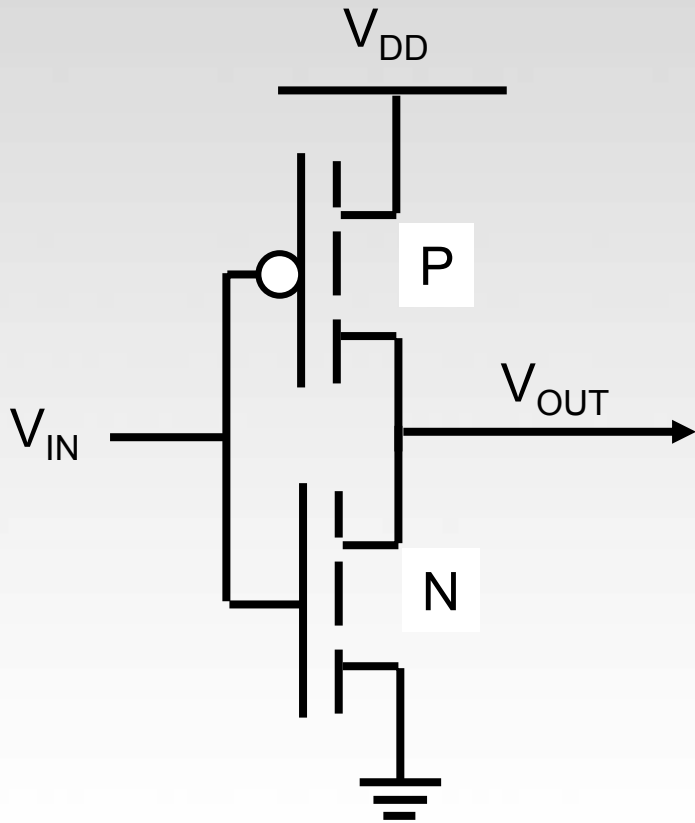
Smaller Diameter  $\rightarrow$  Larger Schottky Barrier

$I_{\text{ON}}$  increases linearly with diameter.

$I_{\text{OFF}}$  increases exponentially with diameter.



# CMOS Inverter with Ambipolar FETs



By shifting  $V_{FB}$  by  $V_{DD}/2$ , we get a useable FET (joint work with Professor Lundstrom)

NOTE: the p-FET and the n-FET are the same device!

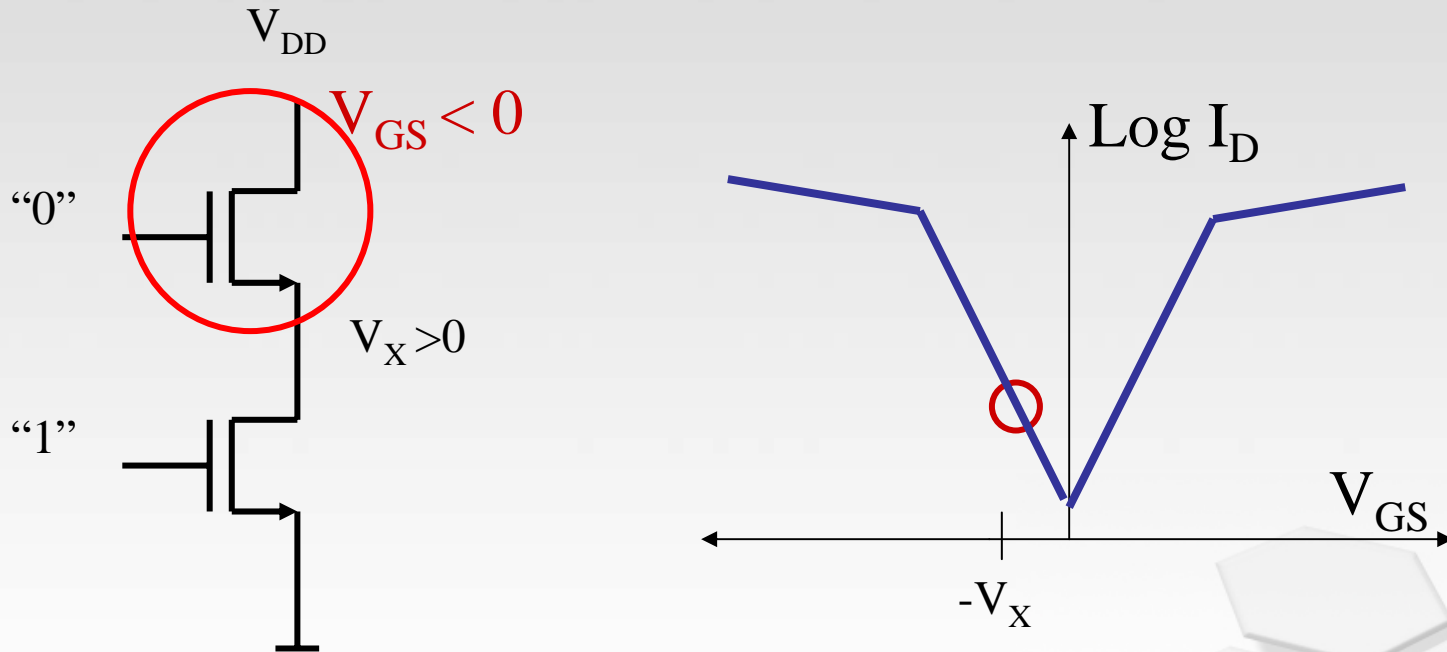


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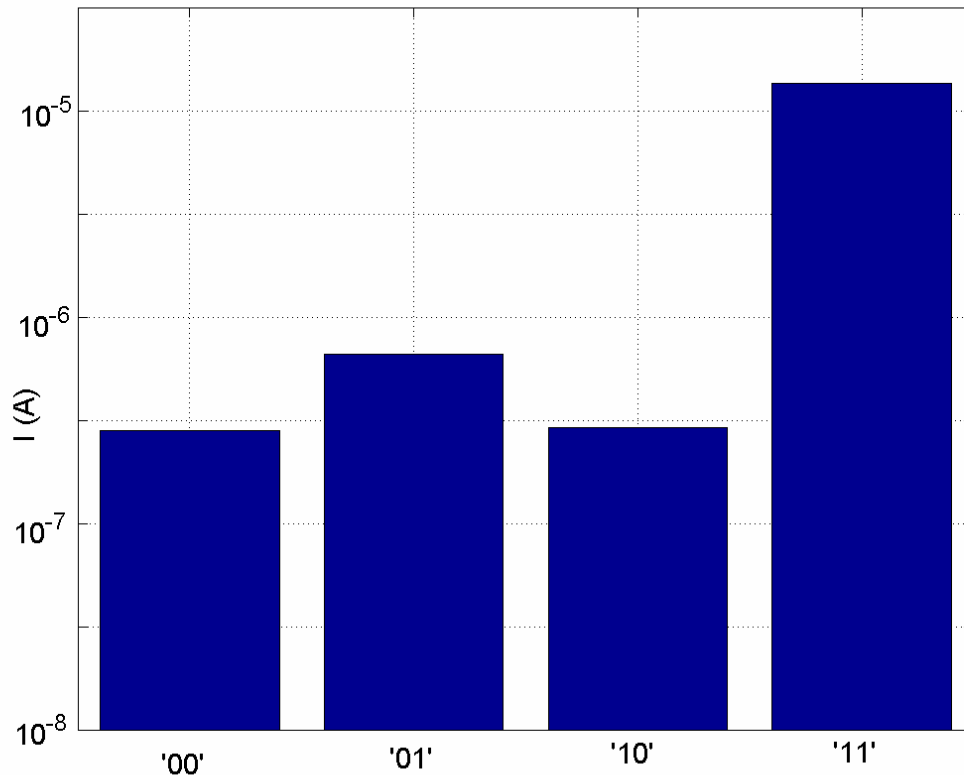
# CMOS logic with stacked transistors



For transistor stacks in the “off” state, we can have  $V_{GS} < 0$ .  
Are these useable in CMOS logic?



# Current vs. input vector



- '01' is the maximum leakage condition
- A stack is functionally operational when  $V_{FB}$  is fixed at  $V_{DD}/2$

**CMOS type logic is possible using ambipolar CNT SBFETs with proper  $V_{FB}$  design**

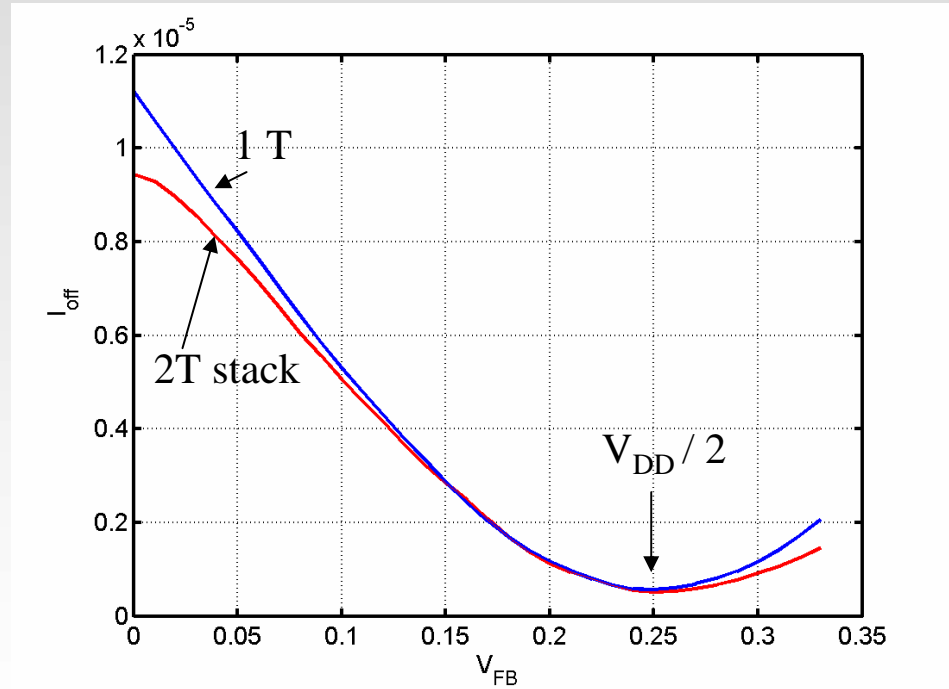
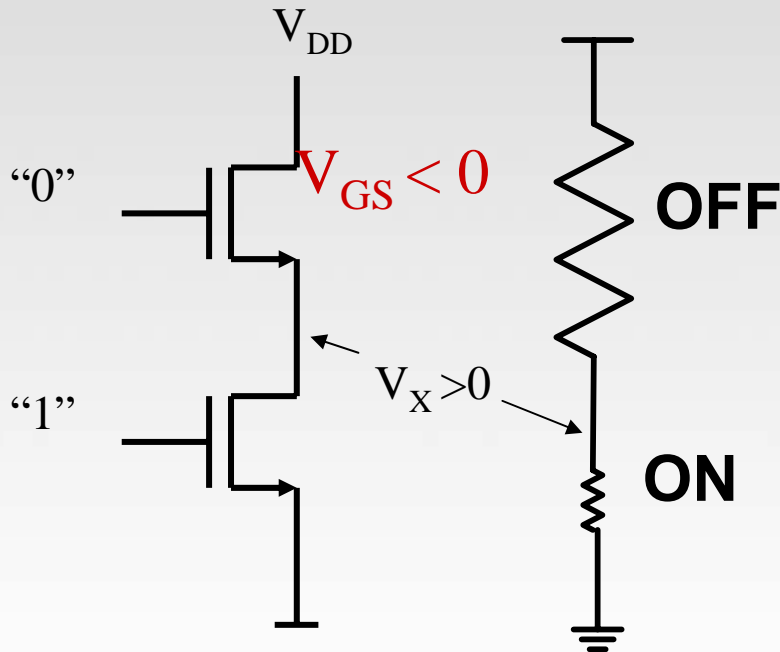


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# CMOS logic with stacked transistors



Ratio of  $I_{ON}$  to  $I_{OFF}$  determines  $V_X$

For  $I_{ON} / I_{OFF} \sim 1000$ ,  $V_X \sim 10\text{mV}$ .

Hence,  $V_{FB} = V_{DD}/2$  is sufficient for a 2T stack

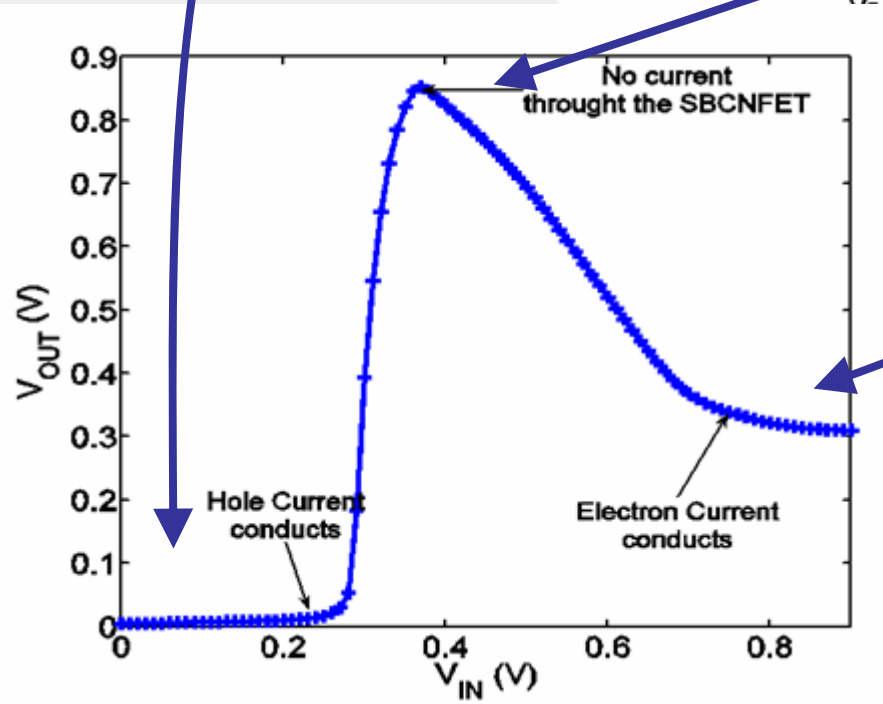
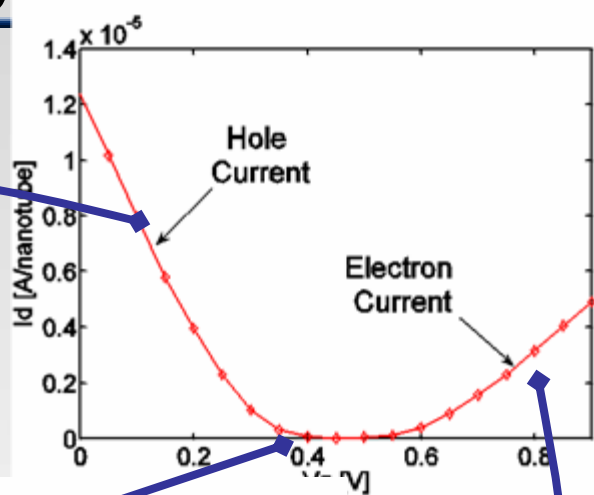
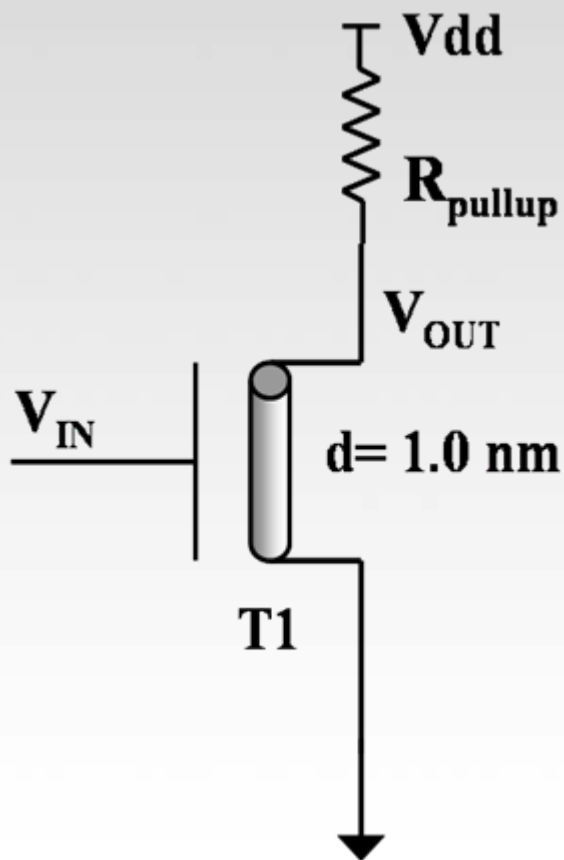


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# A three valued memory cell for higher memory density

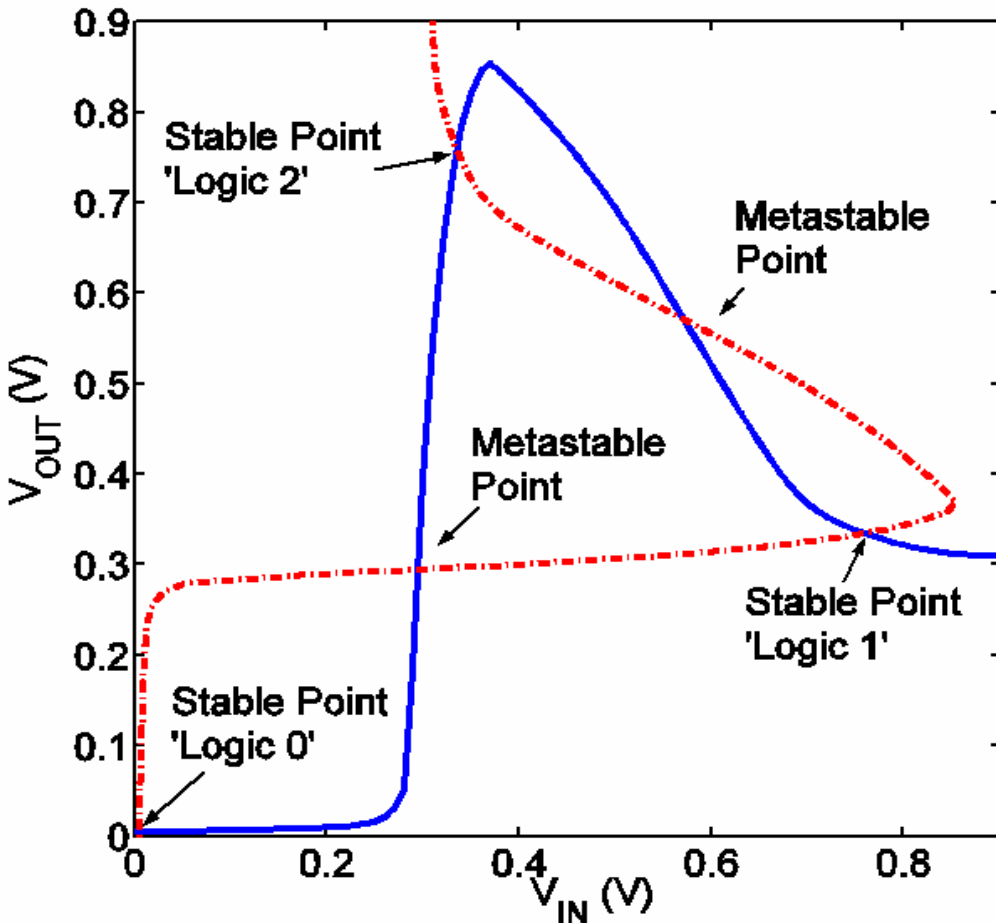


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# The Transfer Characteristics



- o The transfer characteristic shows that the two curves meet at three points.
- o Two of these are metastable points.
- o Three of them are stable operating points located at  $(0,0)$ ,  $(V_{dd}/2, V_{dd})$  and  $(V_{dd}, V_{dd}/2)$

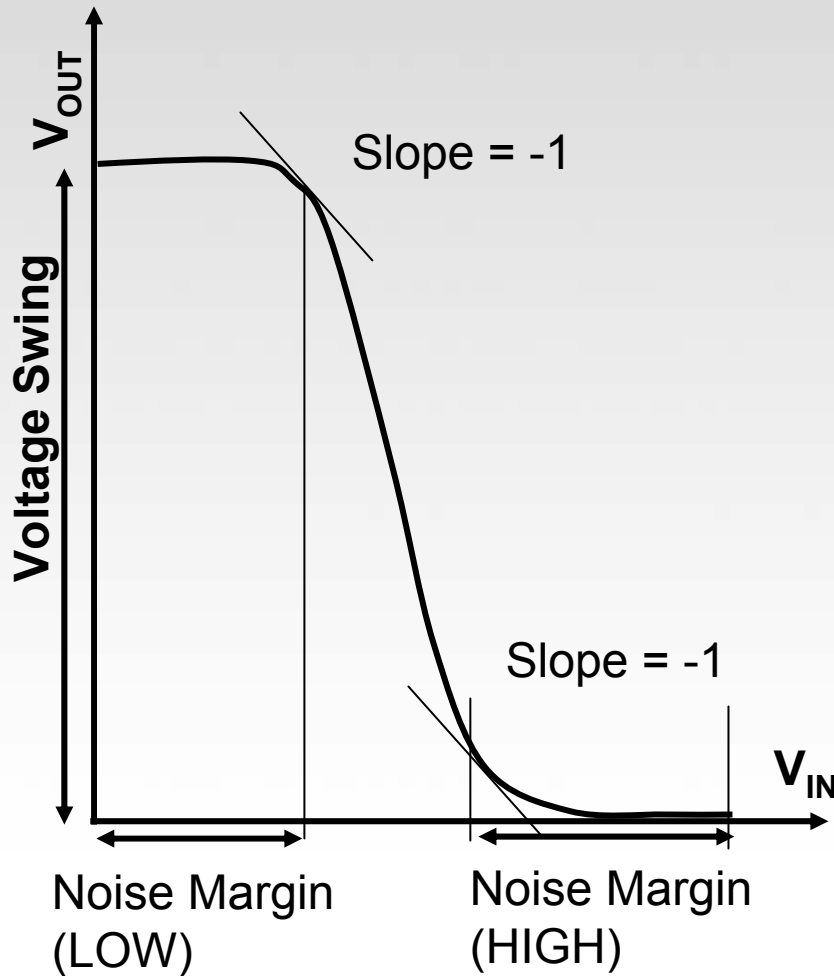
**A three valued memory element is possible.**



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# Voltage Swing and Noise Margin

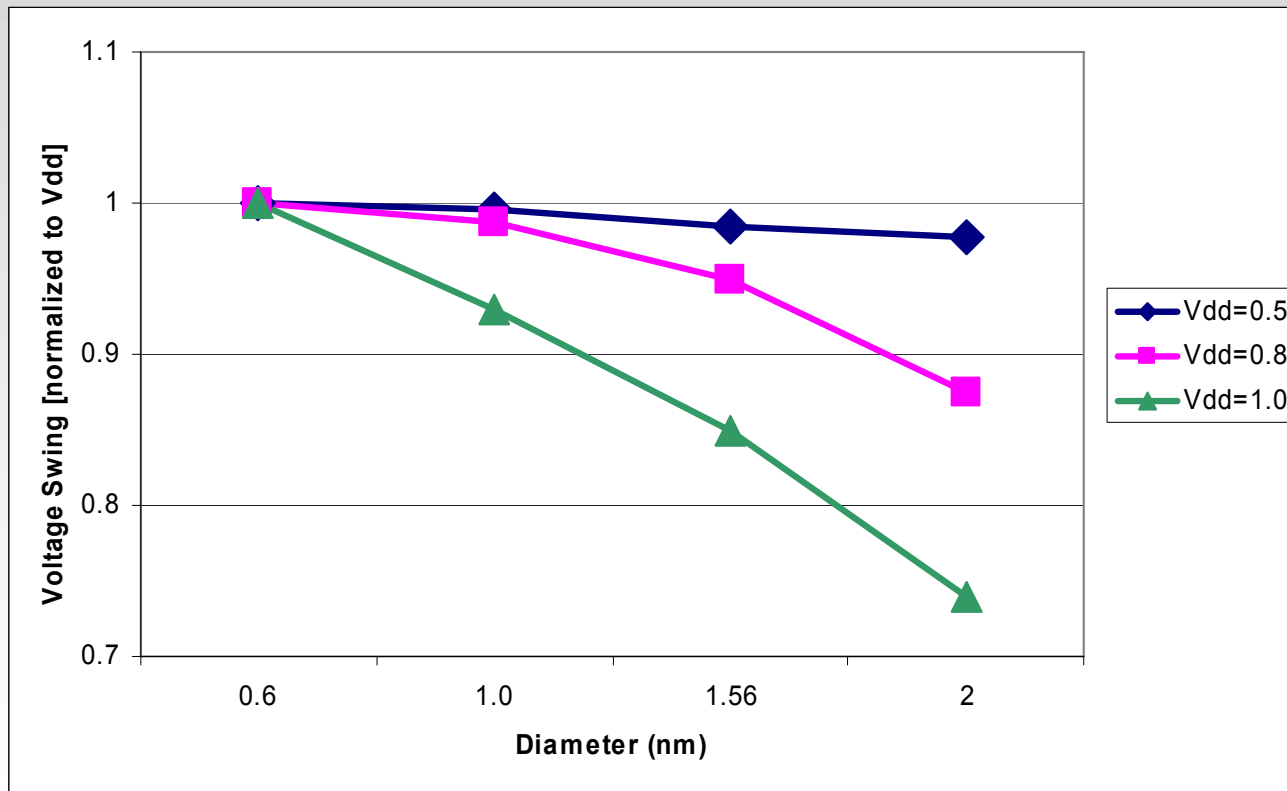


The ideal values should be:

- Voltage Swing (0 to  $V_{DD}$ )
- Noise margin ( $V_{DD}/2$  for both LOW and HIGH states)



# Role of CNT Diameter on Voltage Swing



Top-gated structure

$T_{OX} = 2\text{nm}$

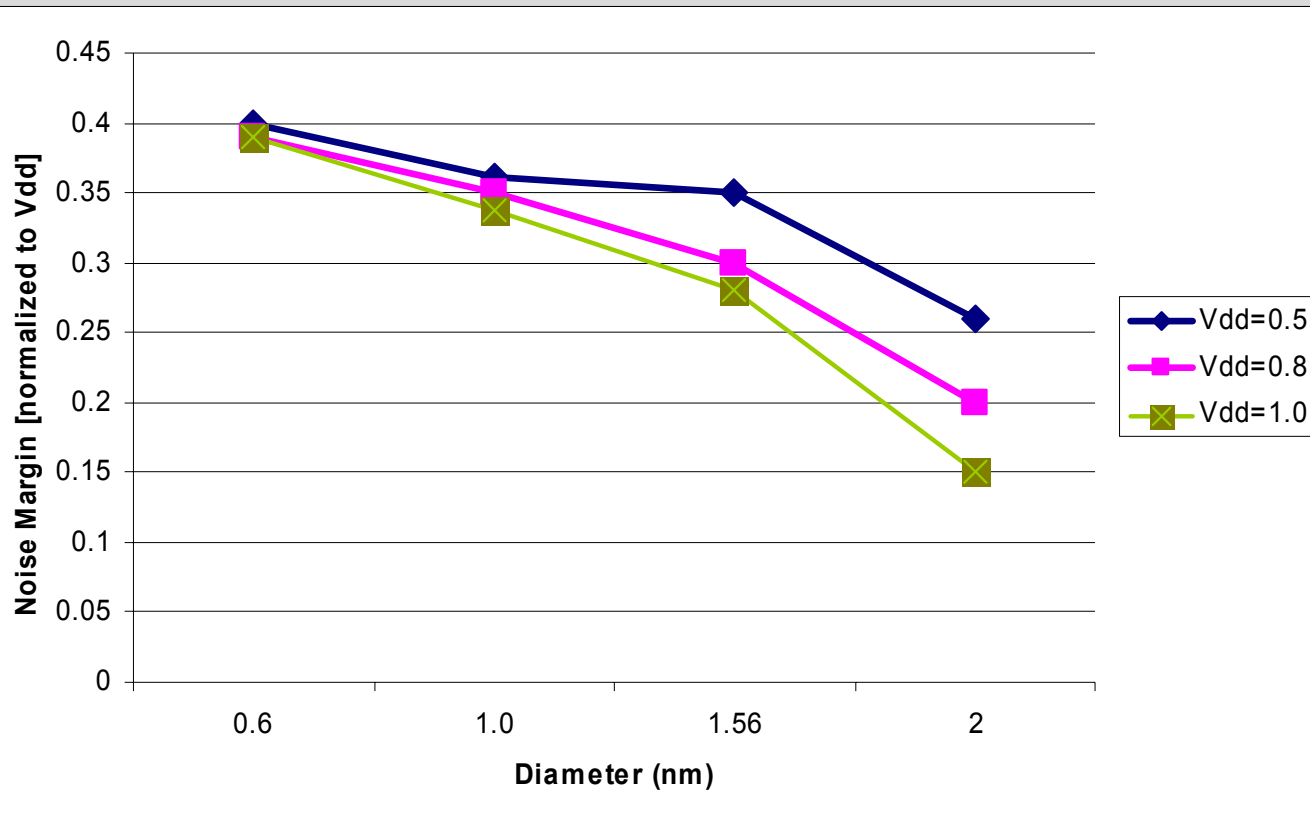
Oxide:  $\text{HfO}_2$

S/D material: Mid-gap SB

NO PARASITICS ASSUMED

**Large CNT diameter and high  $V_{DD}$  are not desired**

# Role of CNT Diameter on Noise Margin



Top-gated structure

$T_{OX} = 2\text{nm}$

Oxide:  $\text{HfO}_2$

S/D material: Mid-gap  
SB

NO PARASITICS  
ASSUMED

**Large CNT diameter and high  $V_{DD}$  reduce the noise margin considerably**



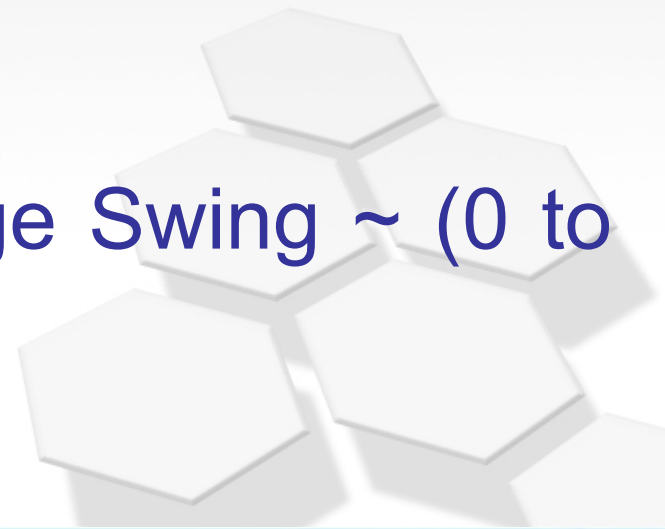
# Towards an Optimum CNFET: Learning

Large Dia ( $d > \sim 1.6\text{nm}$ ) and High  $V_{DD}$  ( $V_{DD} > \sim 0.6\text{V}$ ) – Not Usable in SB CNFETs

## Reason:

- $I_{OFF} \sim \exp(V_{dd} - E_G)$  unlike thermionic transport (MOS CNFETs)

MOS CNFETs have full Voltage Swing  $\sim (0 \text{ to } V_{dd})$ .



# Performance – Power Studies

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Design of a single tube CNFET

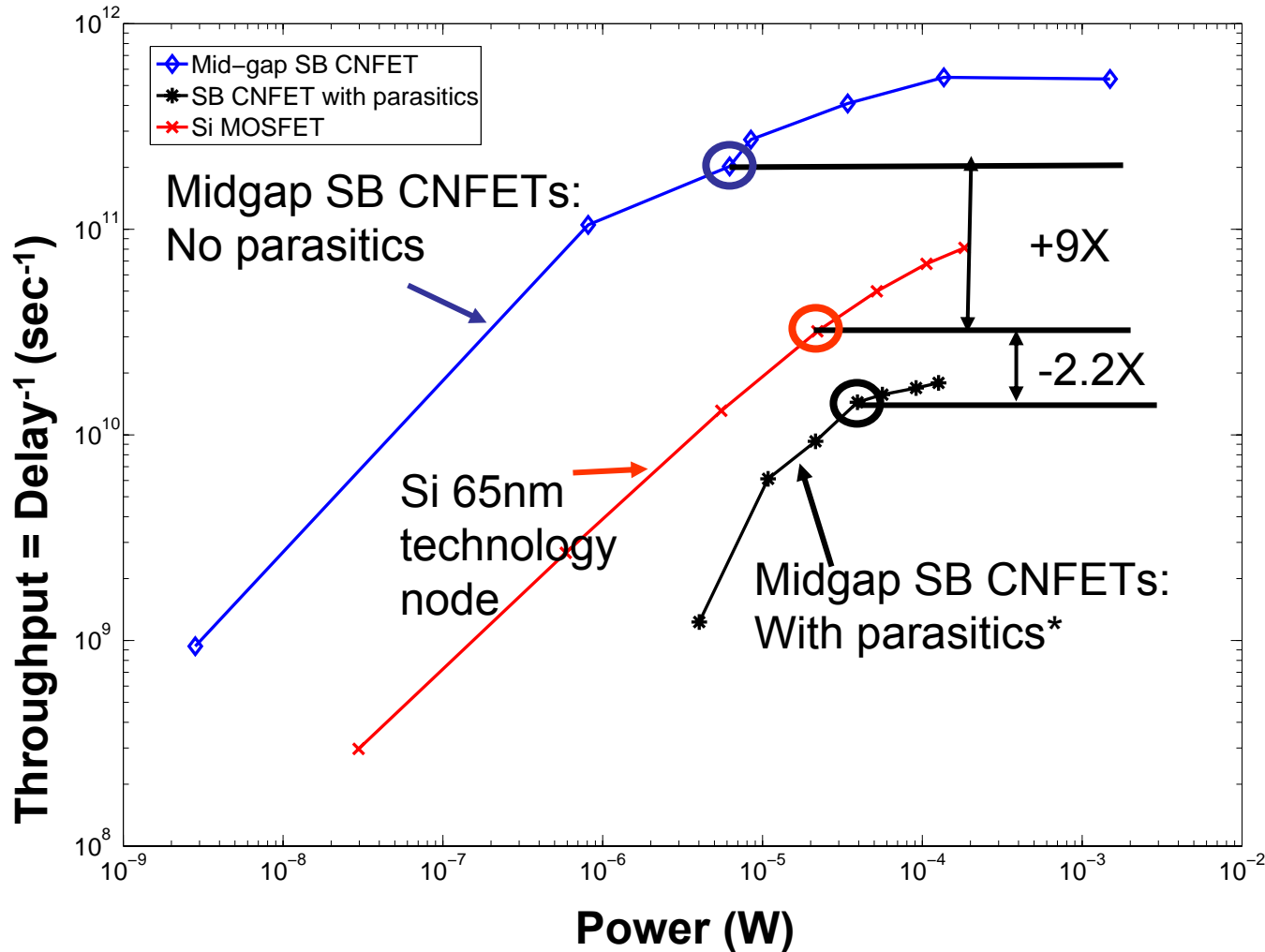
Transient simulations to determine:

- **Role of Parasitics:**

$R_{S/D}$ ,  $C_{gs}/C_{gd}$ ,  $R_{gate}$ .

- **Choice of Packing Density on circuit performance.**
- 

# Benchmarking CNFET circuits



ISO- $V_{DD}$  (0.5V)

Top-gated structure

CNT Dia (d): 1nm

$T_{ox}$  = 2nm

Oxide: HfO<sub>2</sub>

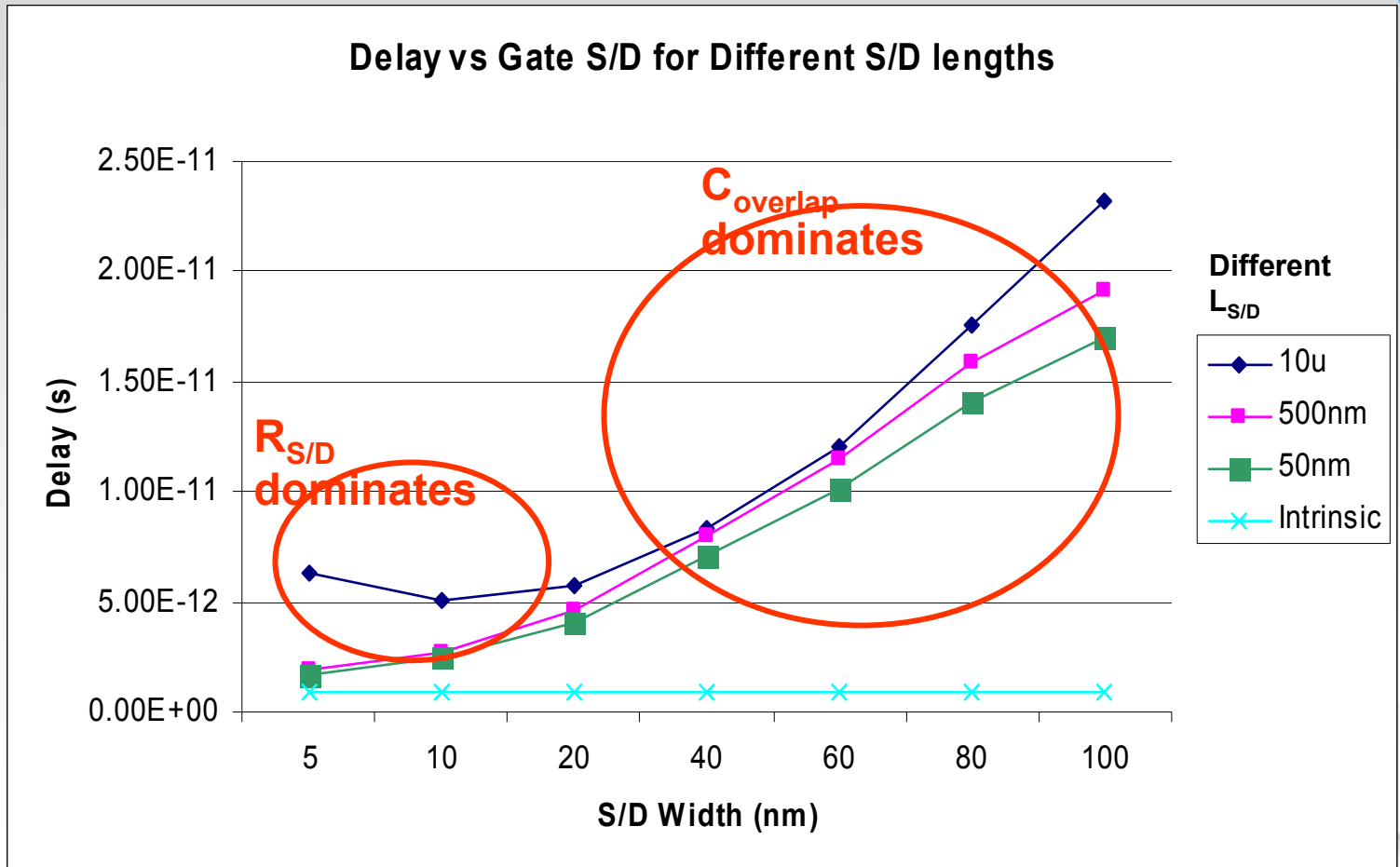
S/D material: Mid-gap SB

Parasitics are neglected.

Silicon Tx: 1264 (65nm) process

\*Parasitics extracted from Stanford device and  $T_{ox}$  scaled to 2nm

# Delay as a function of S/D Width

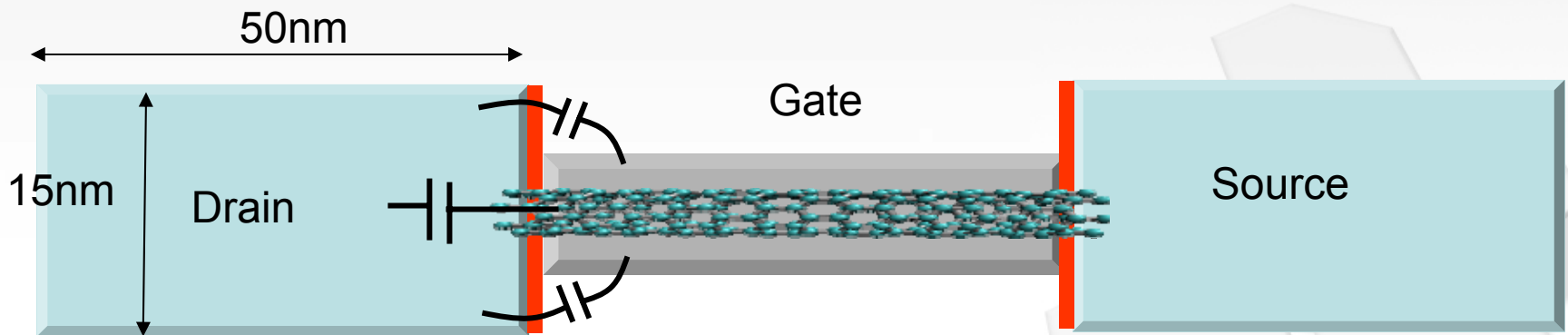


We need nano contacts to nanotubes

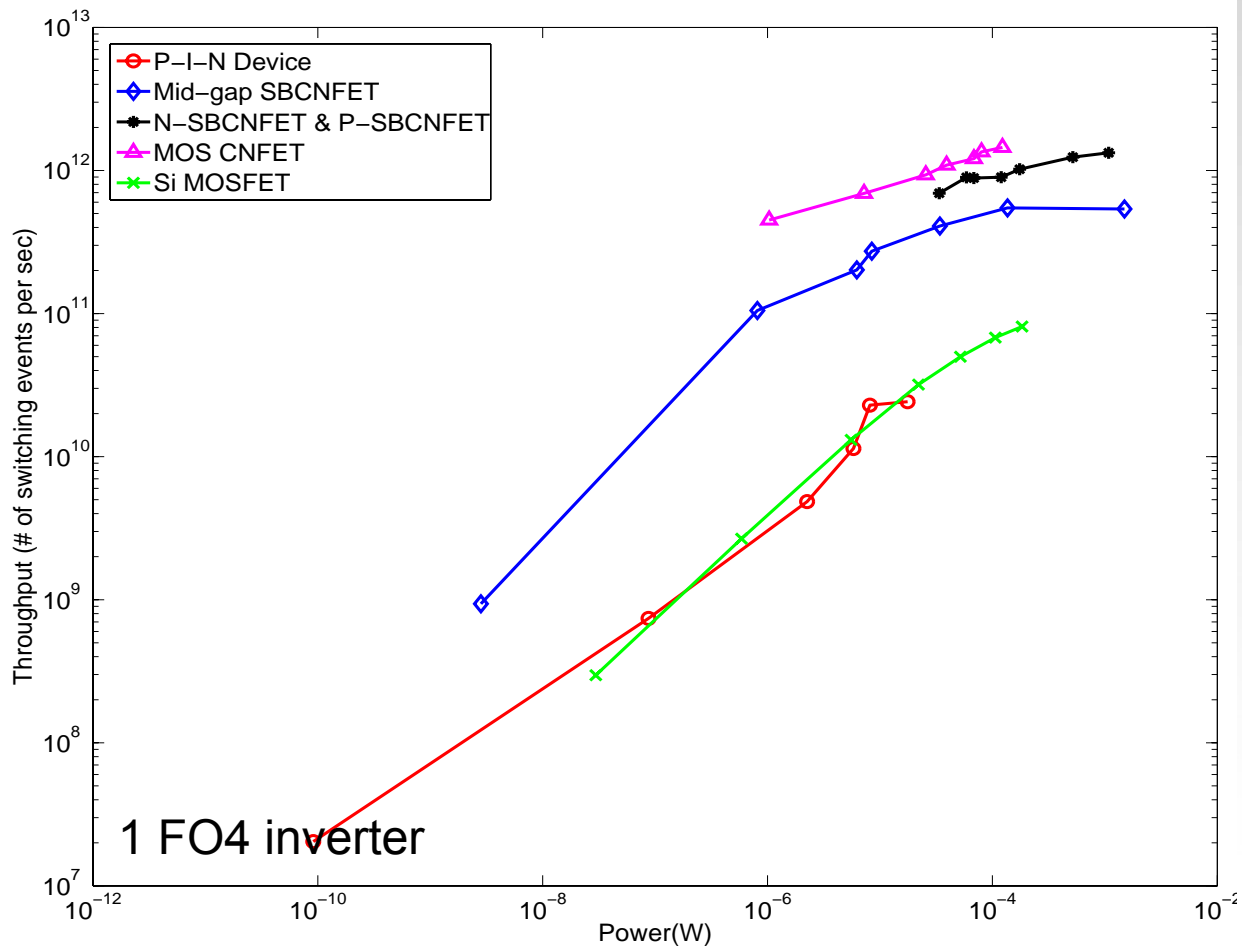
# Possible Solution

## Narrow Gate Electrode and wide S/D:

- The Gate needs to be patterned exactly on the top of the channel to reduce capacitance. (Gate electrode thickness can be large so that  $R_{\text{gate}}$  is small).
- Wider Source/Drain reduces  $R_{\text{S/D}}$ . Typical dimensions are 15nm X15nm for a length of 50nm.



# Benchmarking Performance of Different CNT Technologies



**Top-gated structure**

**$T_{ox} = 2\text{nm}$**

**Oxide:  $\text{HfO}_2$**

**S/D material: Mid-gap SB**

Simulations performed for  $V_{DD}$  values of 0.2 to 0.8V in steps of 0.1V

- MOS CNFETs have the best performance
- P-I-N tunneling devices can be used for ultra low power/ low leakage circuits



# CNT as Interconnects

- An **all CNT design**
- Parasitics will play an important role as the intrinsic gate capacitance is extremely small
- Ultra-small and high reliability
- Cu can handle a max. current density of  $\sim 10^6 \text{ A/cm}^2$  whereas CNTs can handle more than  $10^8 \text{ A/cm}^2$
- Mechanically strong and no electro-migration effects

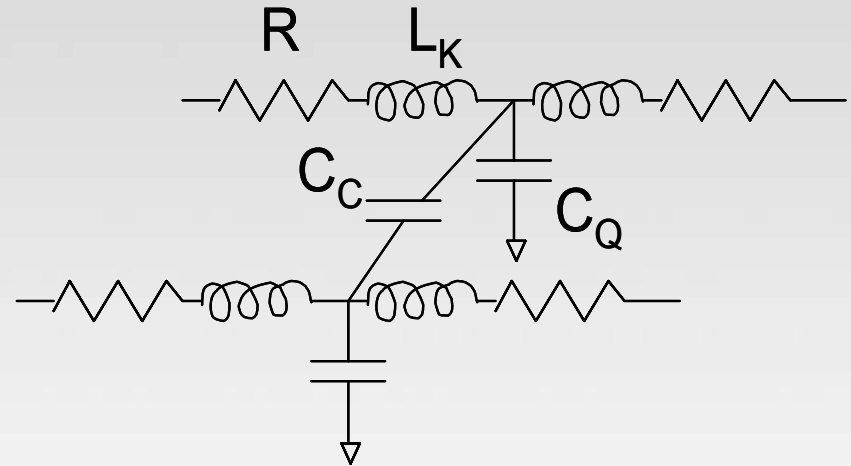
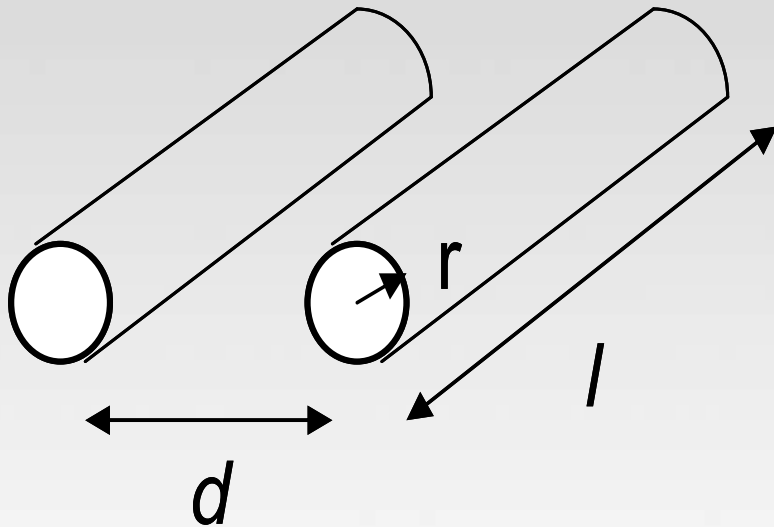


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# Modeling CNT Interconnects\*



Developed an **RLC Model for CNT Interconnects**:

- Incorporates quantum as well as electrostatic capacitances
- Models the kinetic (or self) inductance

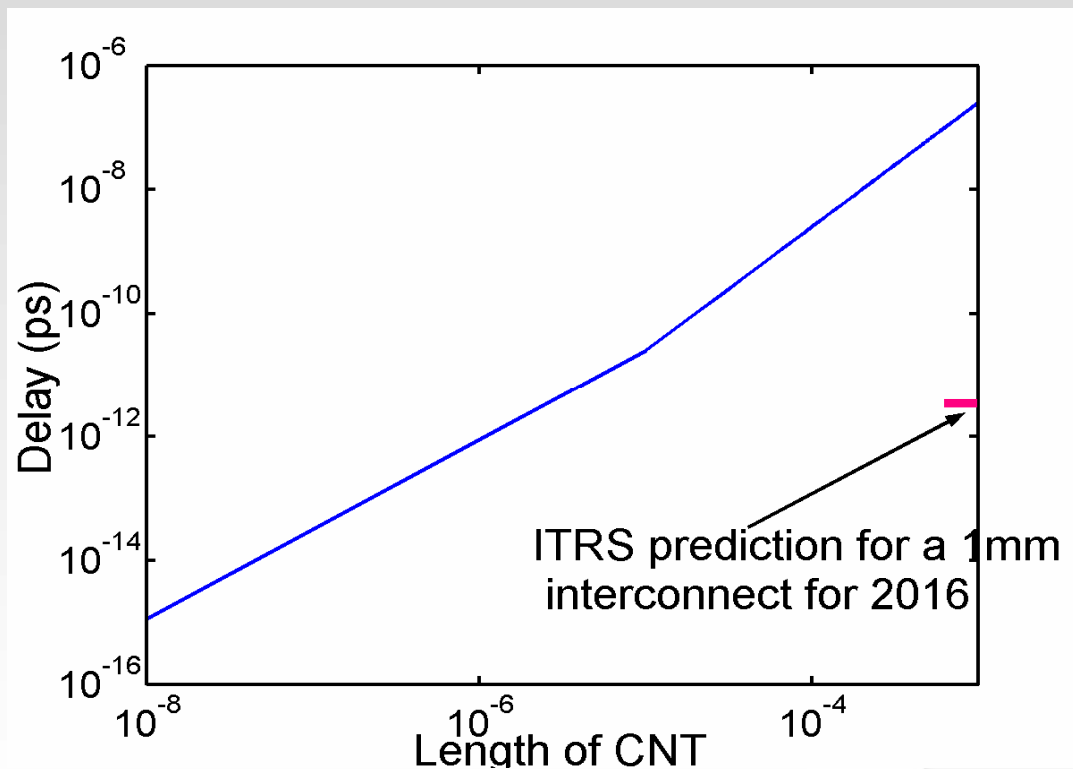


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# Performance of a single CNT



**Delay vs length of a single CNT interconnect. The ITRS prediction has been marked.**

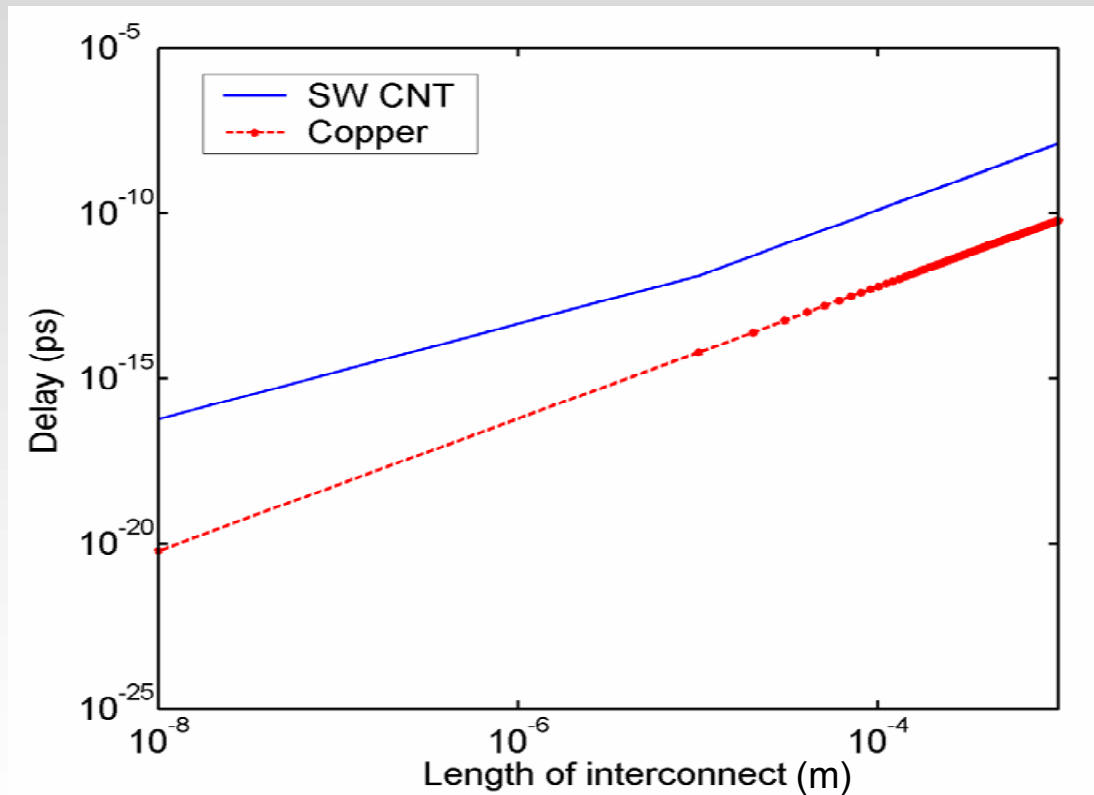


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# Parallel CNTs: Performance estimation



**Comparison of delay of 20 parallel CNT interconnects with copper interconnect having the same equivalent width (w=80nm)**



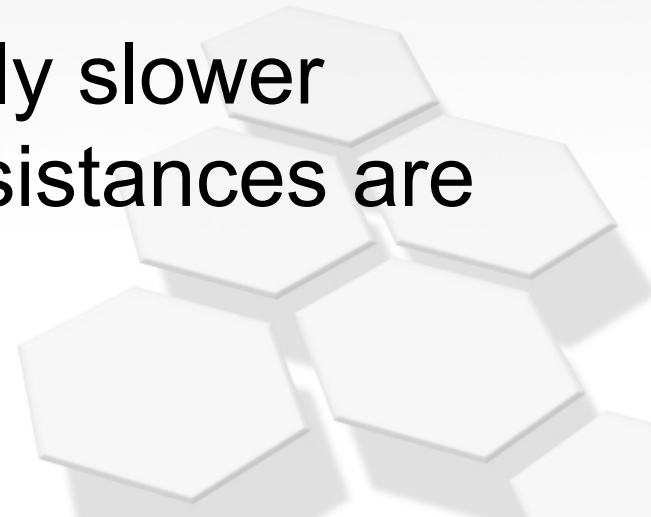
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# Limitations of CNT Interconnects

- CNT interconnects are severely limited by the contact resistances and kinetic inductance.
- High current densities do not result in high performance.
- Can only be used in relatively slower circuits where the device resistances are high.



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# Nanotube as a 1-D Nanoconductor

- The wave propagation is slowed down by the kinetic inductance
- Below 100 GHz, the propagation is RC-limited anyway: the series R ( $\sim 10$  kOhm/ $\mu$ m) overwhelms the inductance
- The series resistance is much larger than that of conventional macroscopic interconnect

→ “A **single** nanotube will be **SLOW** as an interconnect in general”  
(Ref: [Sayeef05])

Note: a single CNT could still be used as a local interconnect if the load is another nanoscale CNT-based structure  $\rightarrow RC \sim 25$  fs (Ref: [Burke04]).

DC power distribution might be another option



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# Conclusions & future work

- A simulation framework for evaluating CNFET based circuits and systems has been developed. More work is required to develop mixed mode device/circuit simulators for different types of devices
- Novel circuit ideas for low power/high-density are being developed considering special features of the CNFETs
- Device optimization strategies needed and are being developed for optimized performance – device/circuit co-design
- Fault tolerant architecture and circuit design under process variation need to be considered

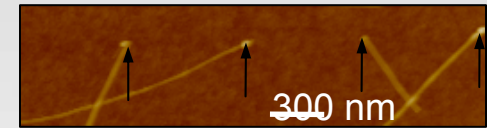
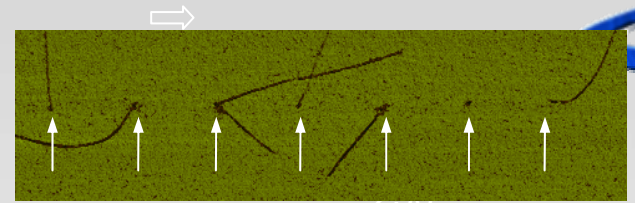


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# Major Technological Challenges

1. Control of chirality (yield ~90% with PECVD).
2. Direction of growth has to be controlled and gate material deposited on the CNT only.
3. Arrange CNTs in parallel in arrays to make effective transistors.
4. Nano-contacts with low parasitics need to be made.
5. Air stable chemical doping of CNTs necessary for making MOS CNFETs.
6. Make better metal-nanotube contacts free from tunneling barriers.



CNTs grow in random direction (Javey, 2004)



Control of directionality is important