A Non-Contact Interconnect Technology for Reducing Semiconductor Chip Cost

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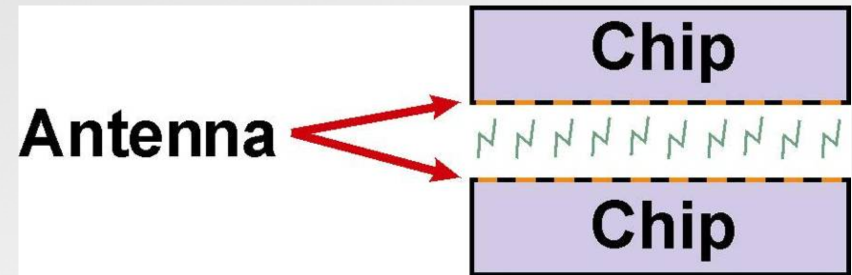
Outline

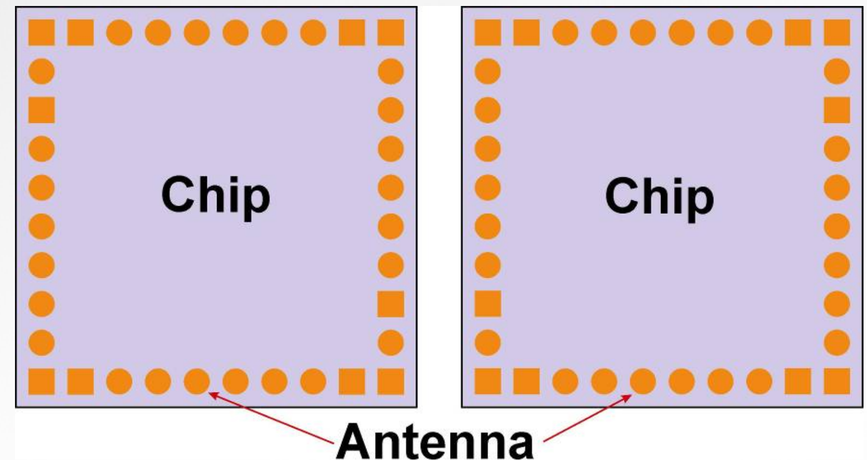
1. Technology overview
2. Application summary
3. Results of development
4. Conclusion

SCANIMETRICS

The Technology

- Disruptive technology which enables new testing techniques and capabilities
- Wireless chip-scale communications
- Distances <100 µm





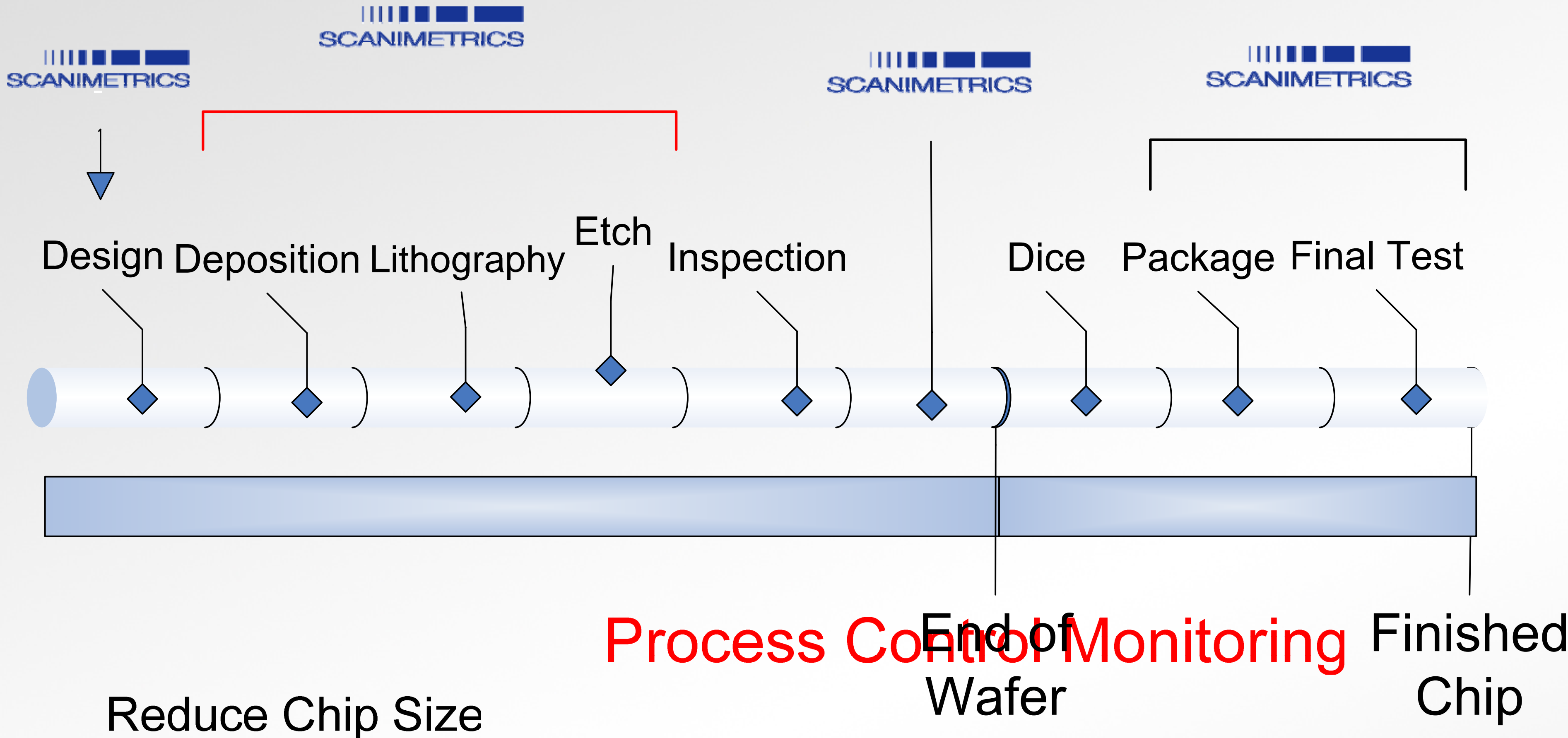
Benefits

- Technology is “non-contact”
  - Chips can be smaller
  - Manufacturing process can be monitored
  - More chips can be tested at once
  - No damage during testing

- Chips are less expensive and production is more efficient

SCANIMETRICS

Technology adds value at several points in the value chain.



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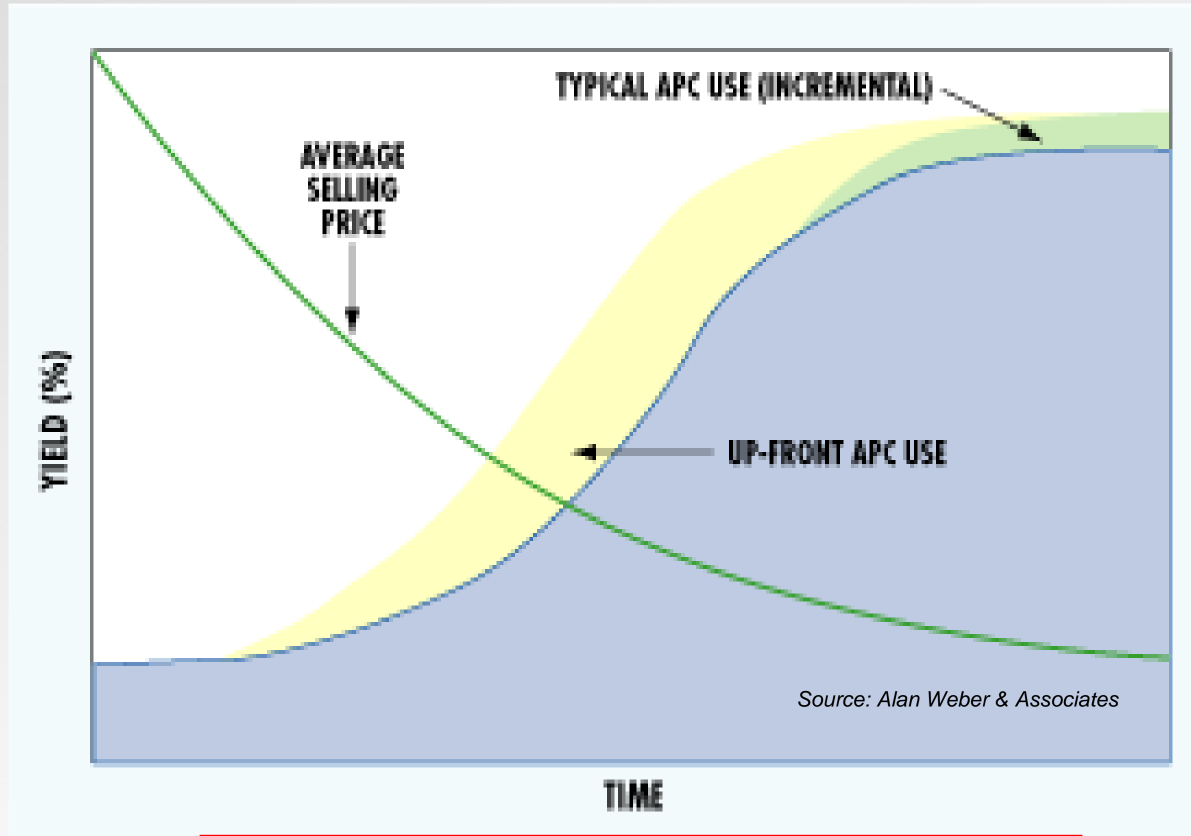
Process Control Monitoring

- Circuits can be tested after 1st metal layer
- Full wafer, multi-site testing capability
- Most PCM tests can be duplicated wirelessly
- Certain wireless tests may be done earlier or later in the process
- DC parametric tests
- AC parametric tests

Process Control Monitoring

Applying Automatic Process Control early in a fab's life cycle can yield significant returns



Enables the earliest possible in-situ process monitoring, shortening a fab's "time to money".

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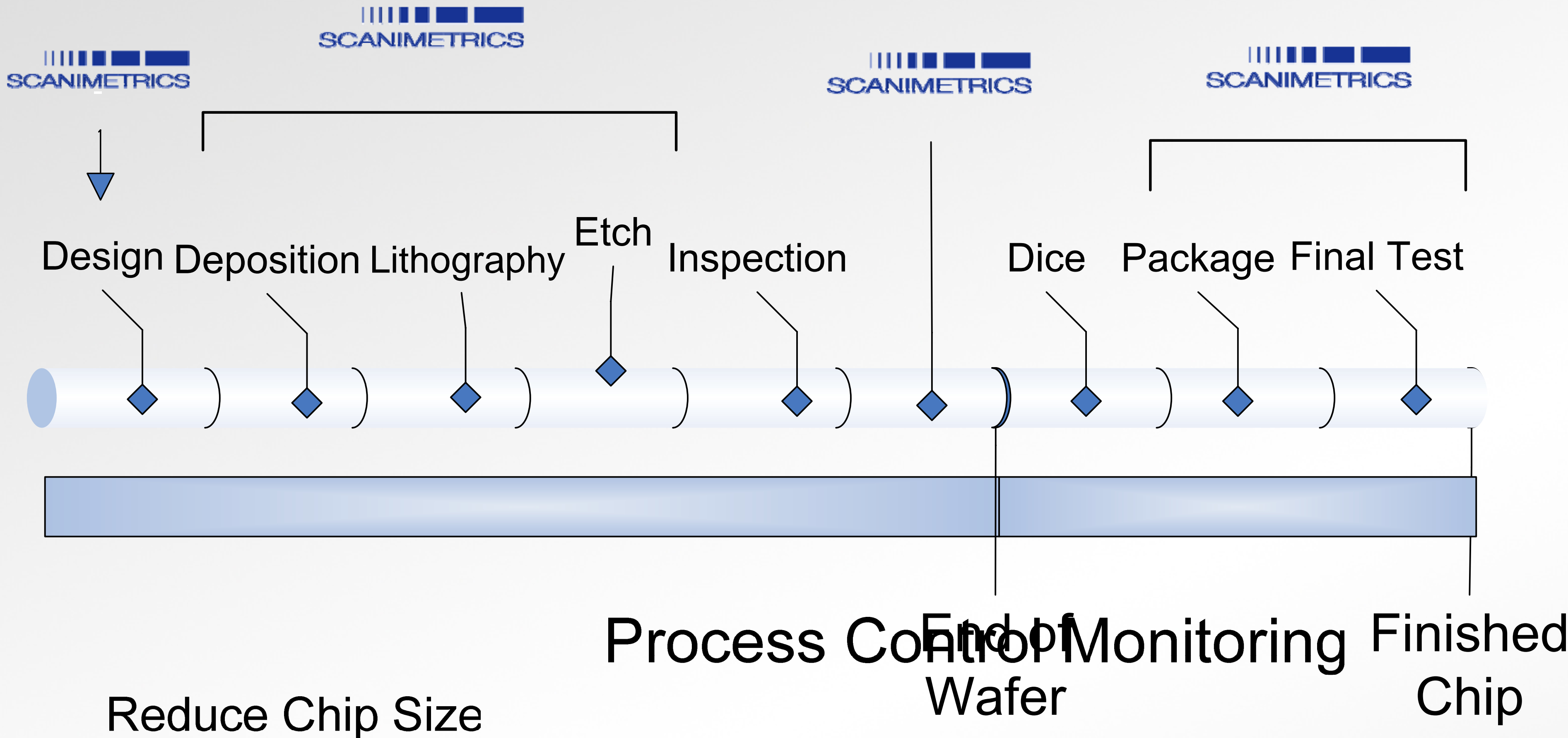
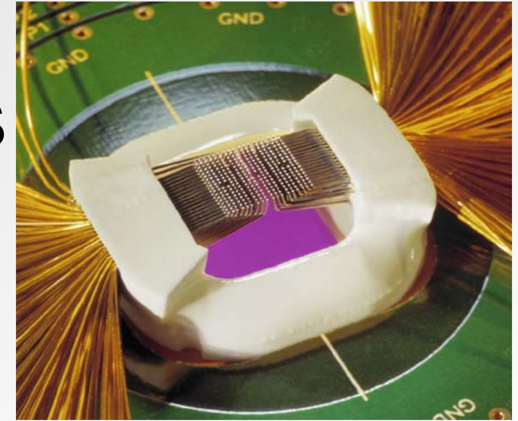
Value Chain

Scanimetrics adds value at several points in the value chain.



Current Technology

- Increases chip costs
- Limits technological advances
- Limits throughput
- Damages chips
- Current industry participants:



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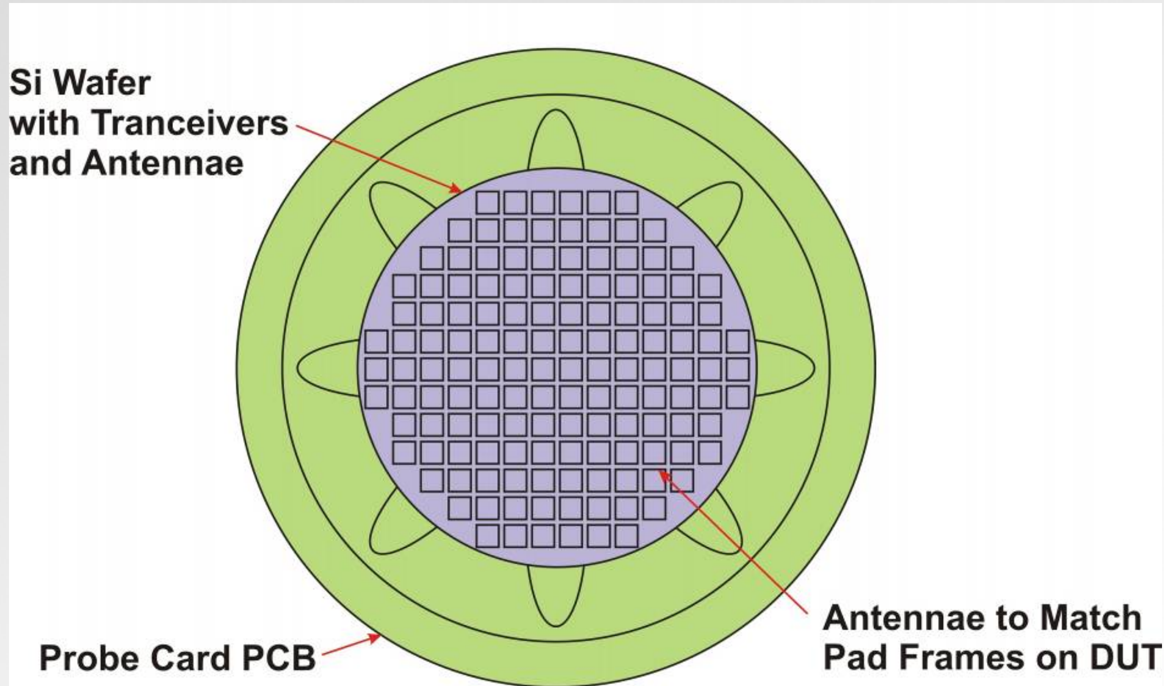
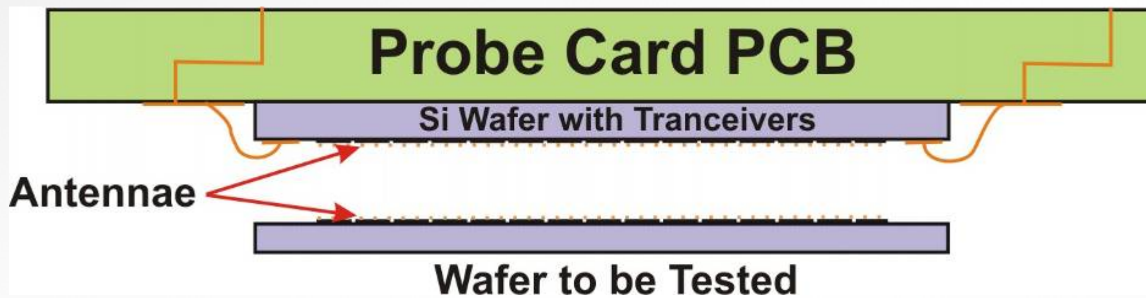
Wafer Probe





Wafer Probe

- Probe separation proportional to pitch
- Wireless power transfer >100mW
- Separate antennae/probes for power transfer
- Hi-rel signal i/o, eliminates contact force and scrubbing issues
- Lower alignment accuracy requirements than mechanical probes
- Scaling
  - Gbps test speeds
  - Highly parallel testing
  - Probe pitch
- Processes
  - Compatible with existing equipment and processes
  - Capability to work with new materials (low-k dielectrics)

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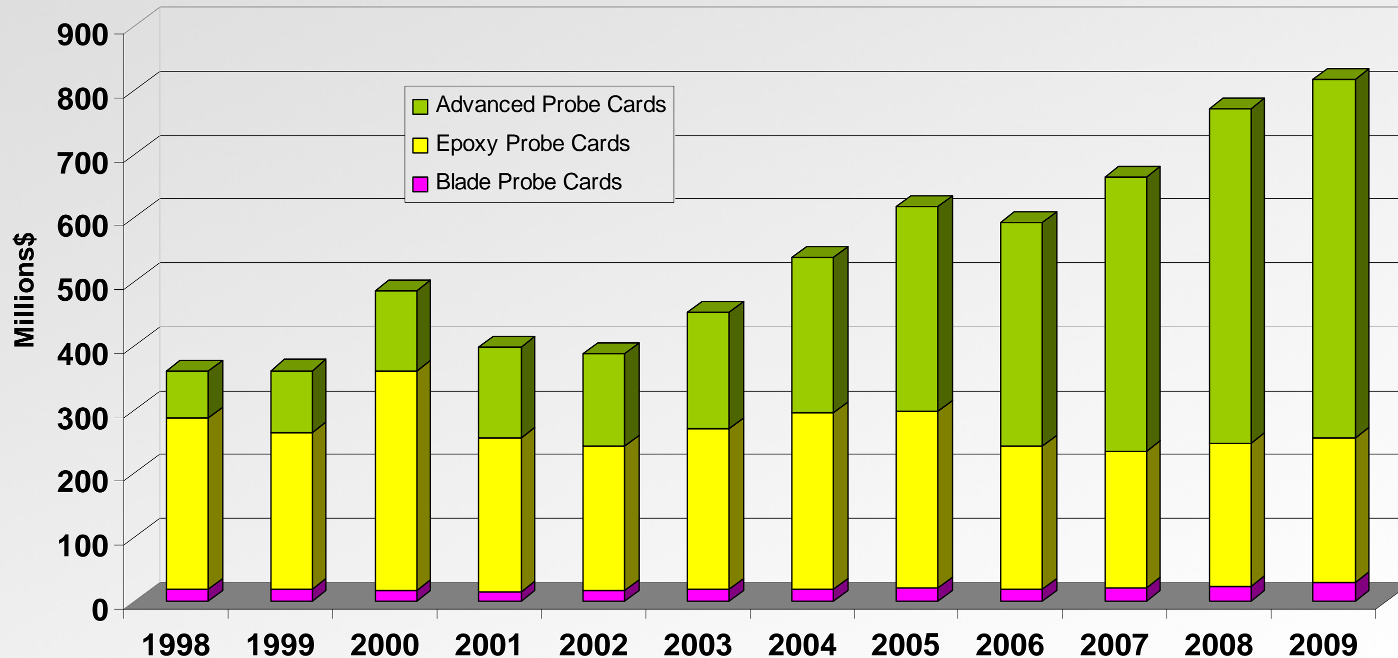
Wafer Probe Card Market



Source: VLSI Research 05/04

- The real 2006 figures are already exceeding the 2008 predictions
  - It is expected to grow 19.1%, following 19.5% growth to $838 million in 2005

    - VLSI Research Inc (06/06)

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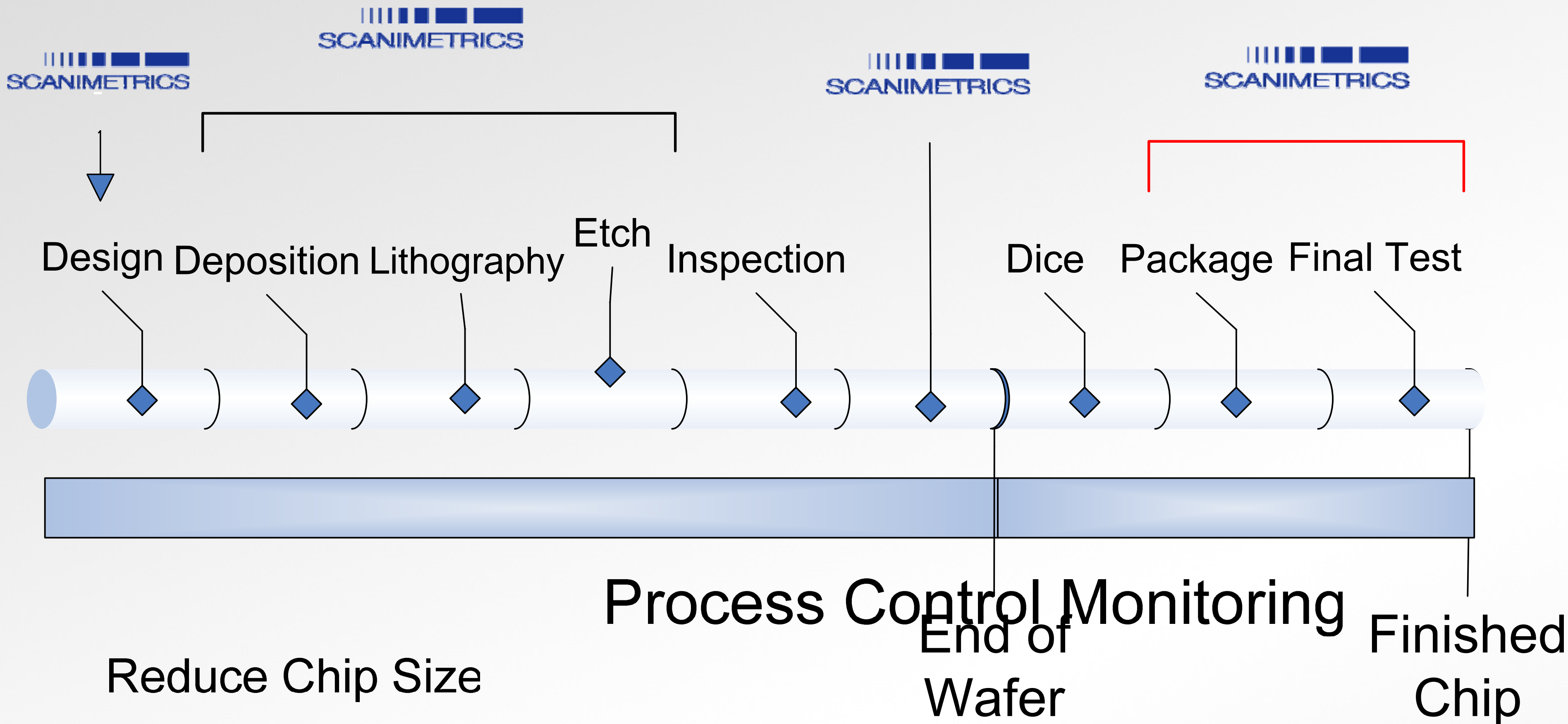

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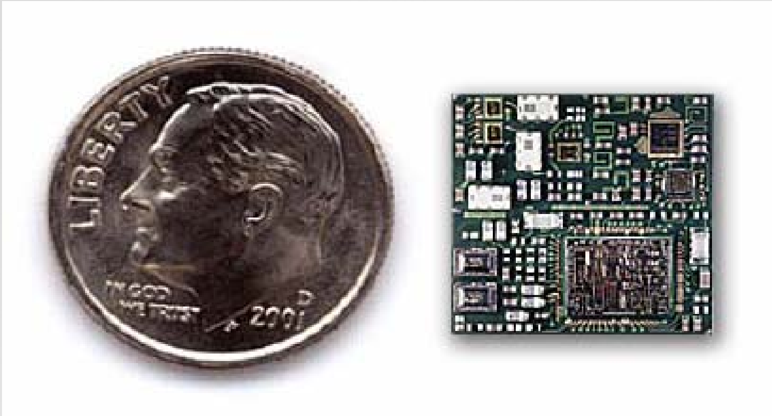
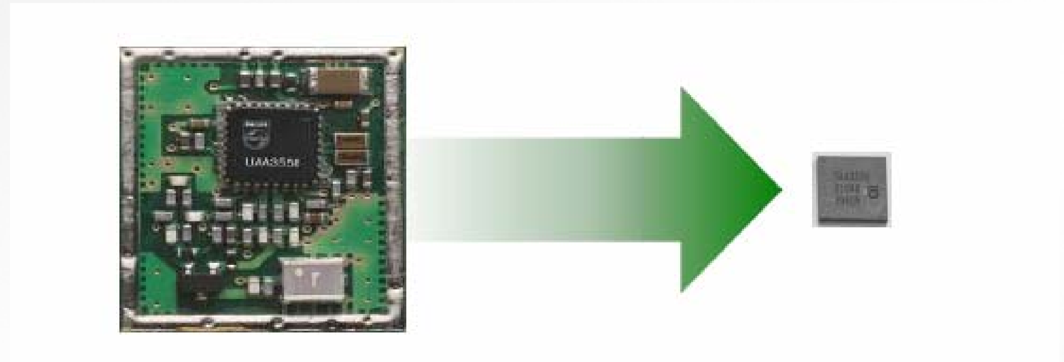
A little more on SiP testing



SiP "*System in Package*"

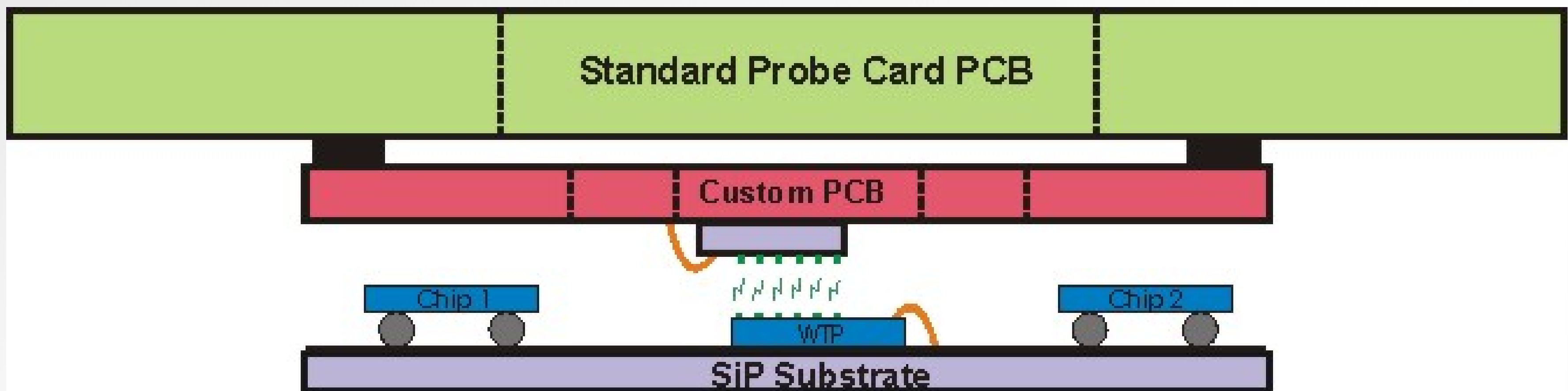
SiP is an rapidly advancing technology for dramatically reducing chip size by combining smaller chips on a host chip thereby eliminating much of the packaging

Scanimetrics is an enabling technology for SiP by allowing testing of each chip component as they populate the host chip



SiP Testing

- Wireless Test Port (WTP)
  - Allows testing during the assembly process so bad "KGD" and assembly errors are detected early
- Increases yield of SiP device
- Reduce discard of good die



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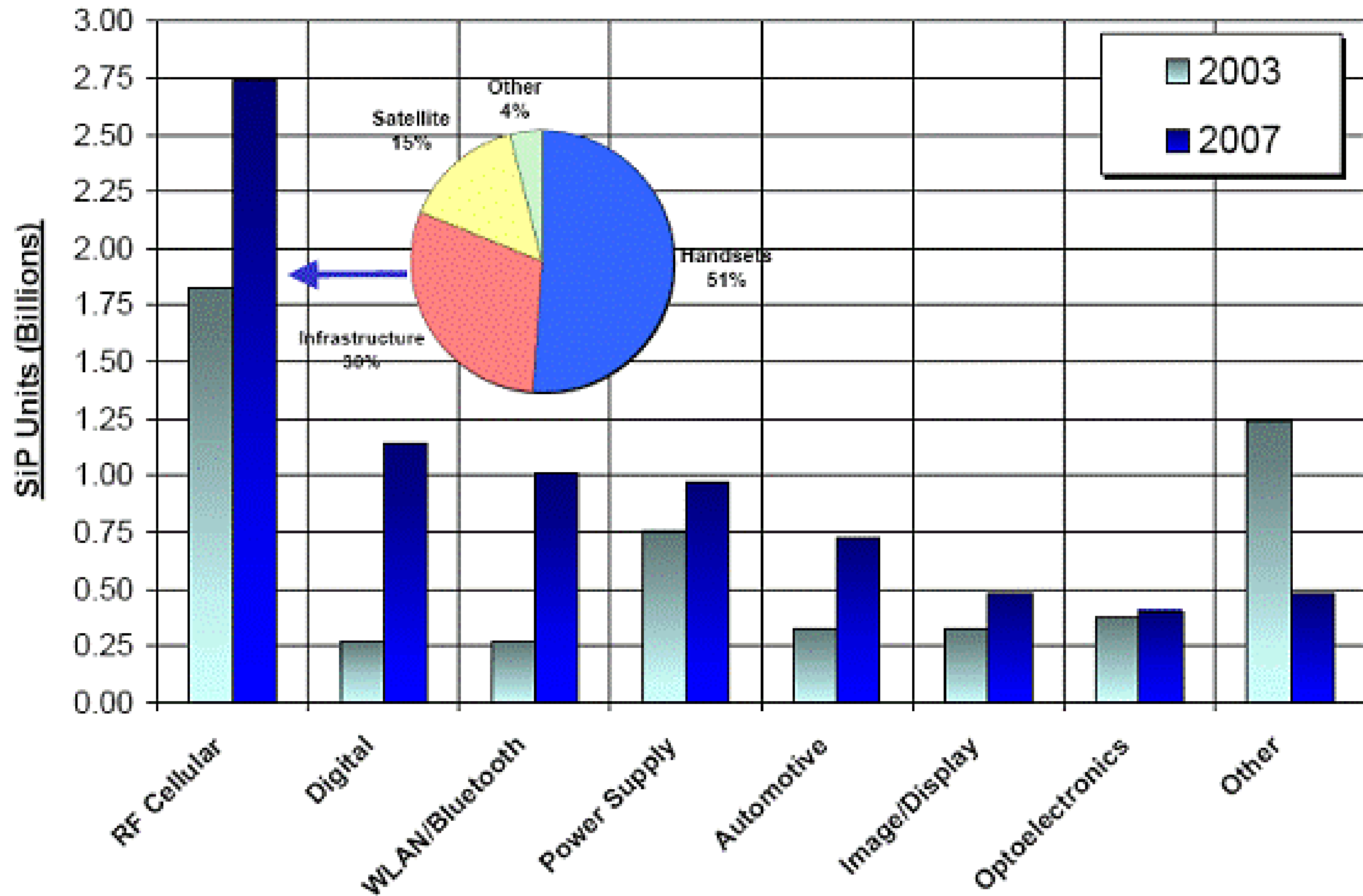
SiP Testing



Sources: Prismark .

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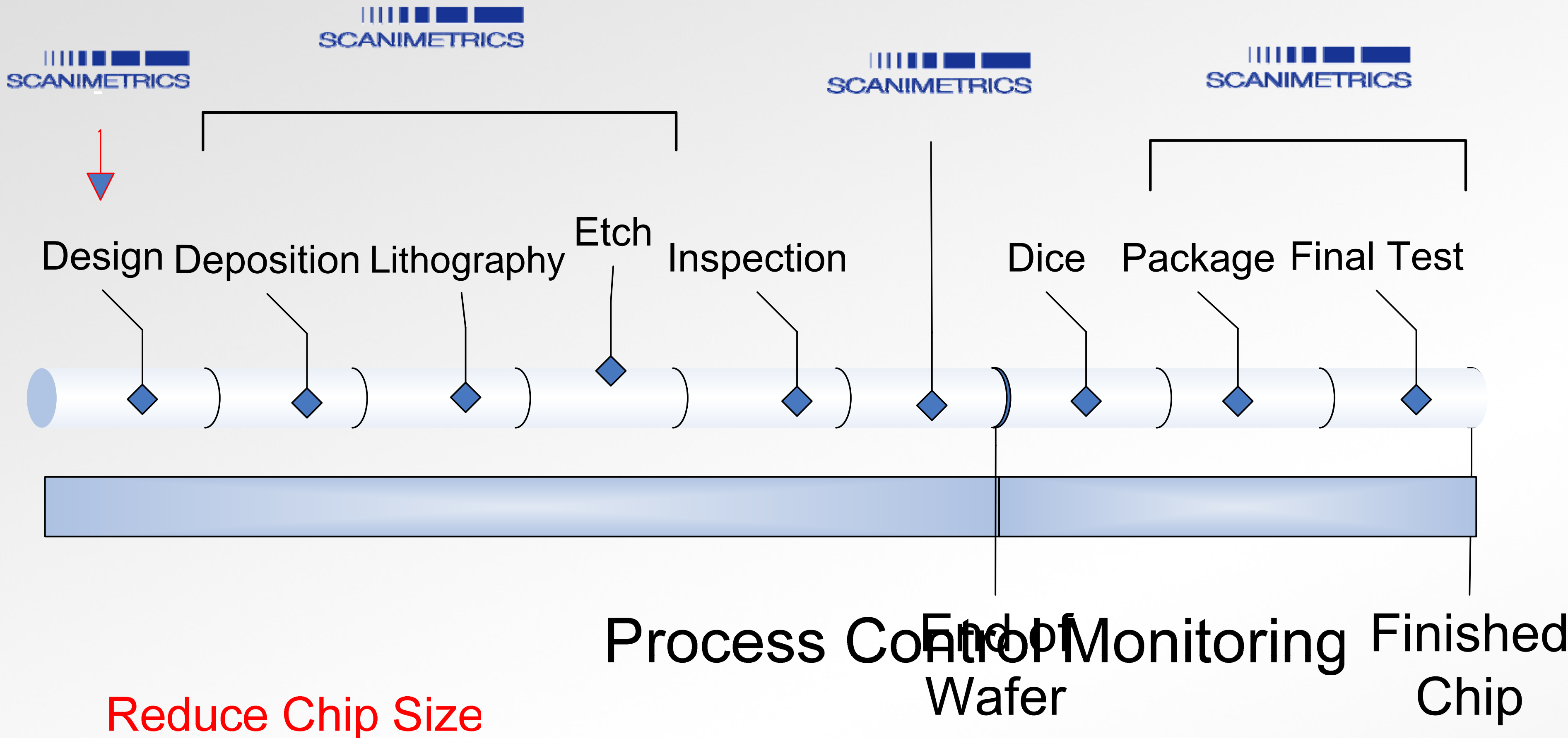


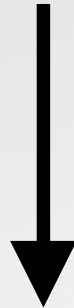
SCANIMETRICS

Impact on DUT – without CUP

SCANIMETRICS

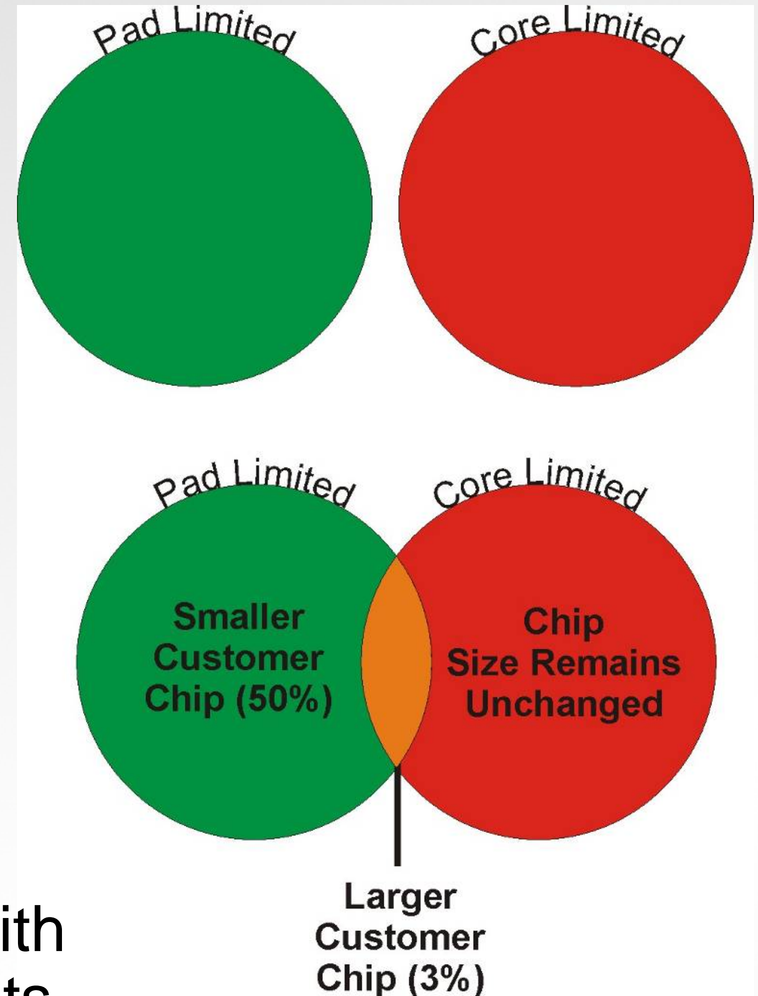
Impact on DUT – With CUP

Chip size w/o Scanimetrics

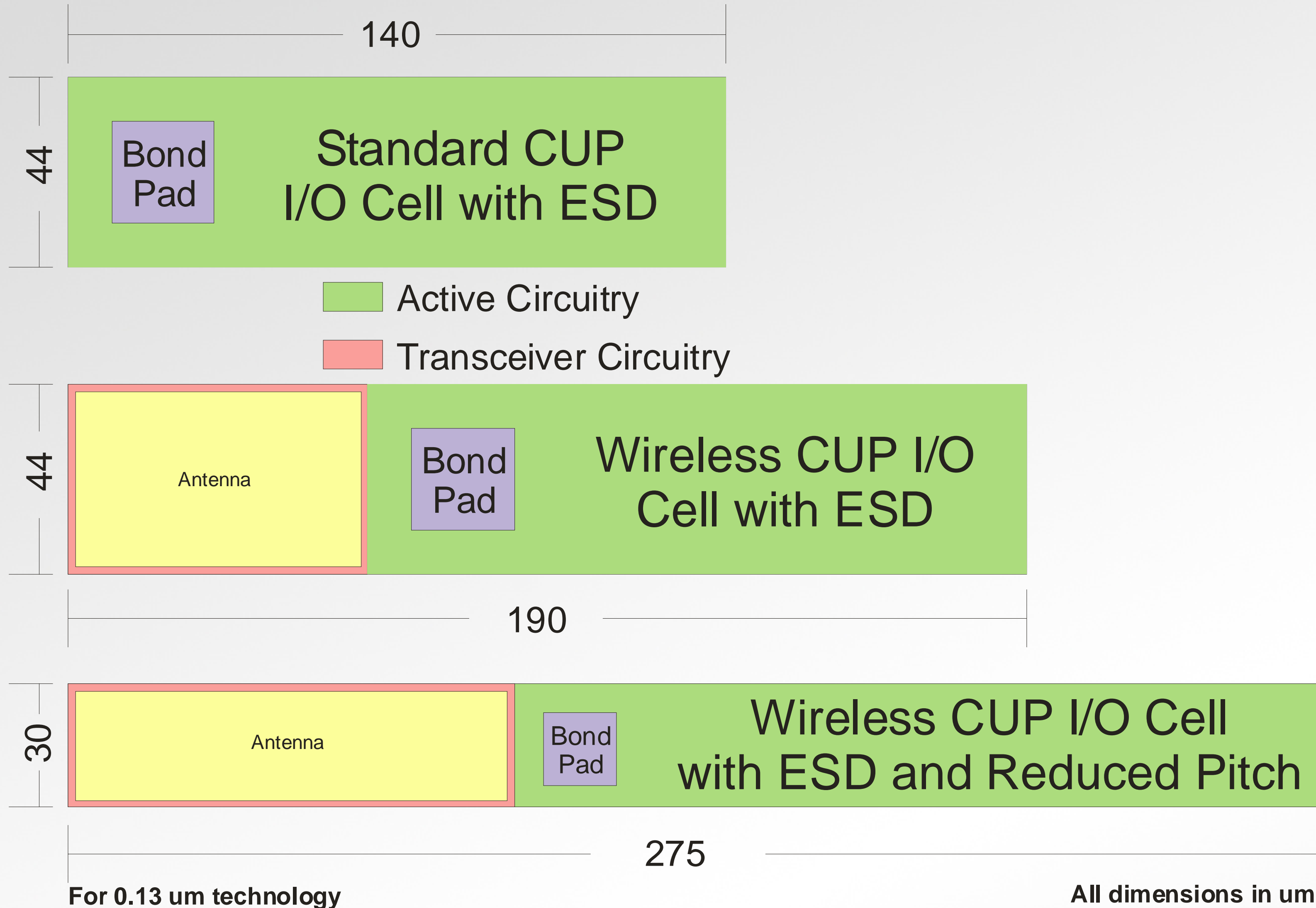


Chip size with Scanimetrics

Supports internal test points with no ESD protection requirements



Impact on DUT – Pad Limited Designs



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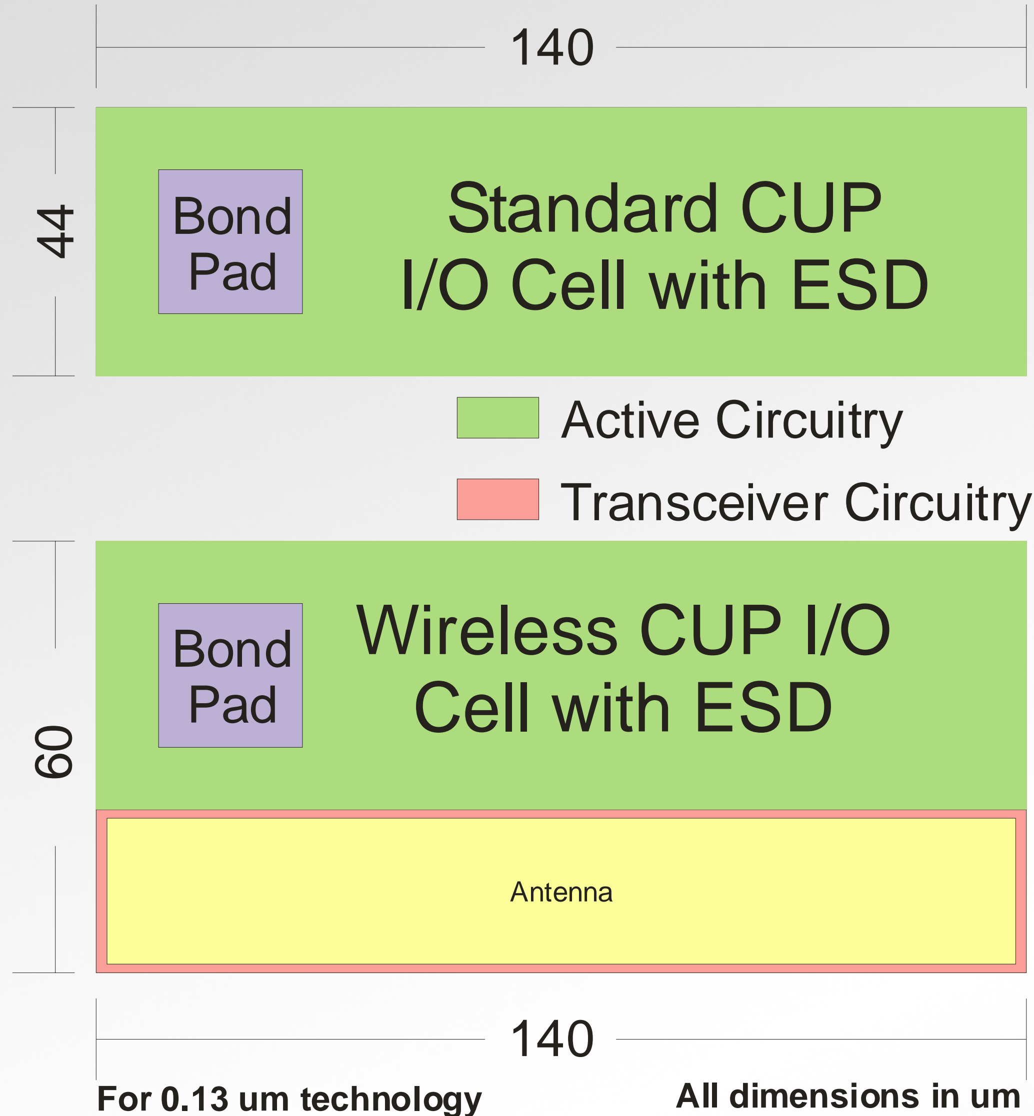
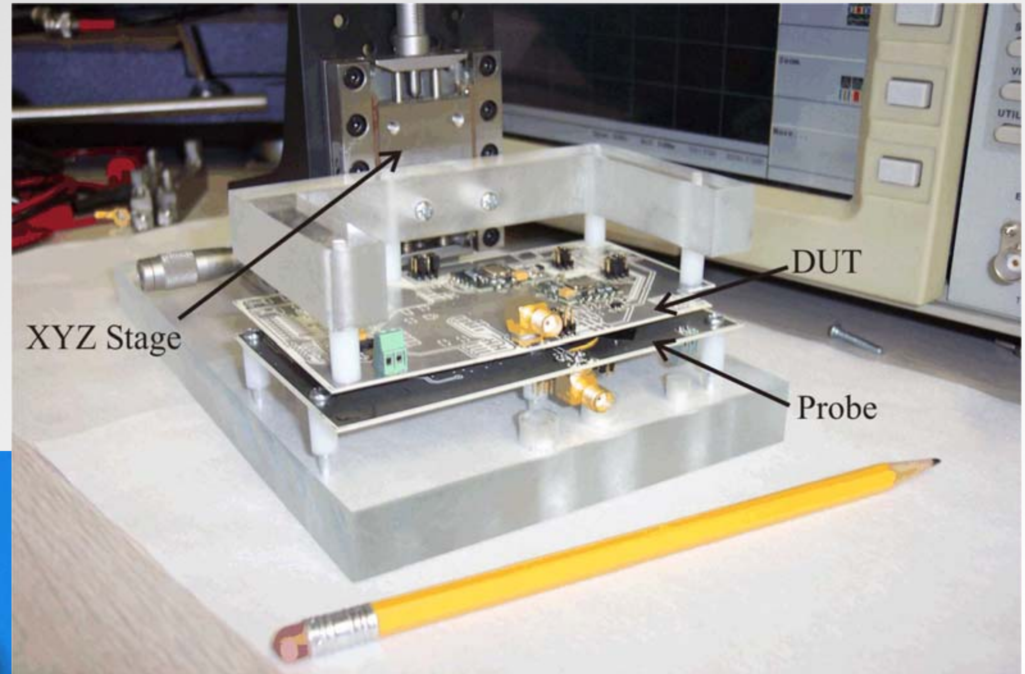
Impact on DUT – Core Limited Designs

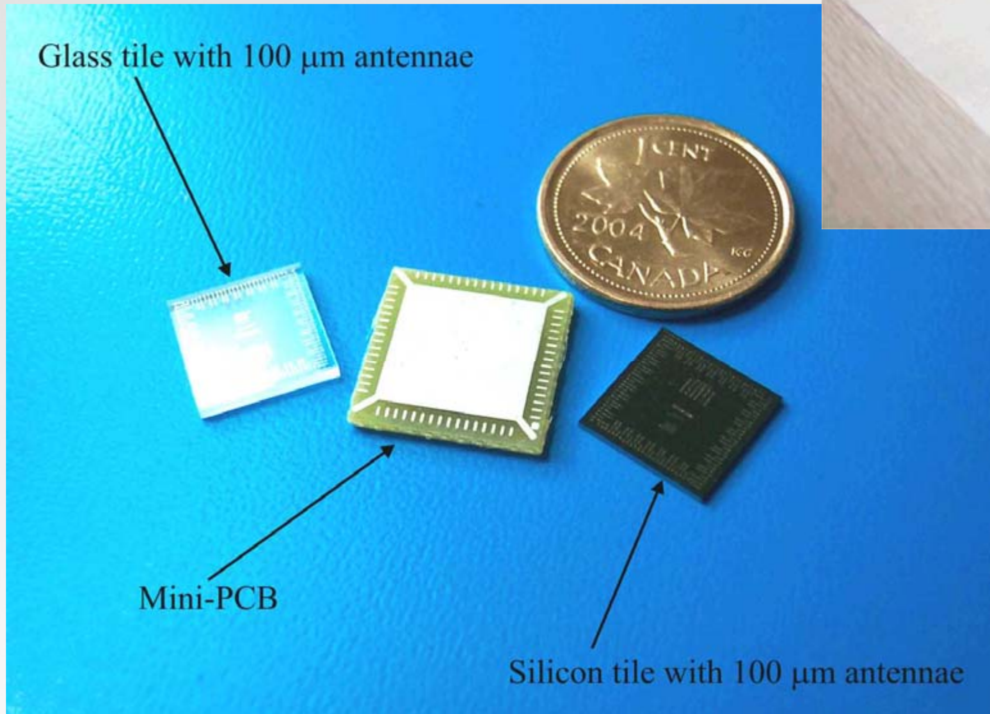


For 0.13 um technology

All dimensions in um

Prototype





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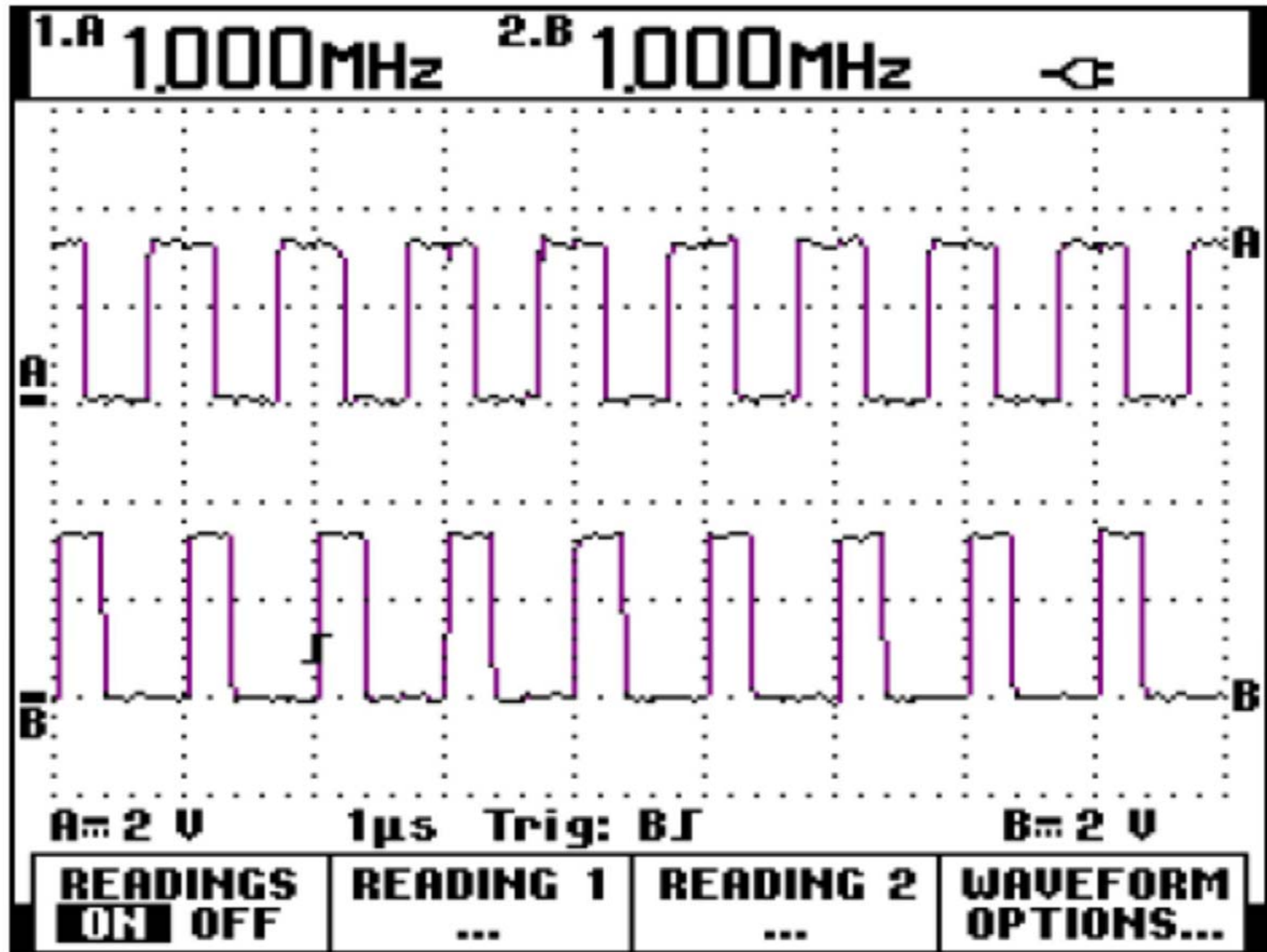
Data signaling



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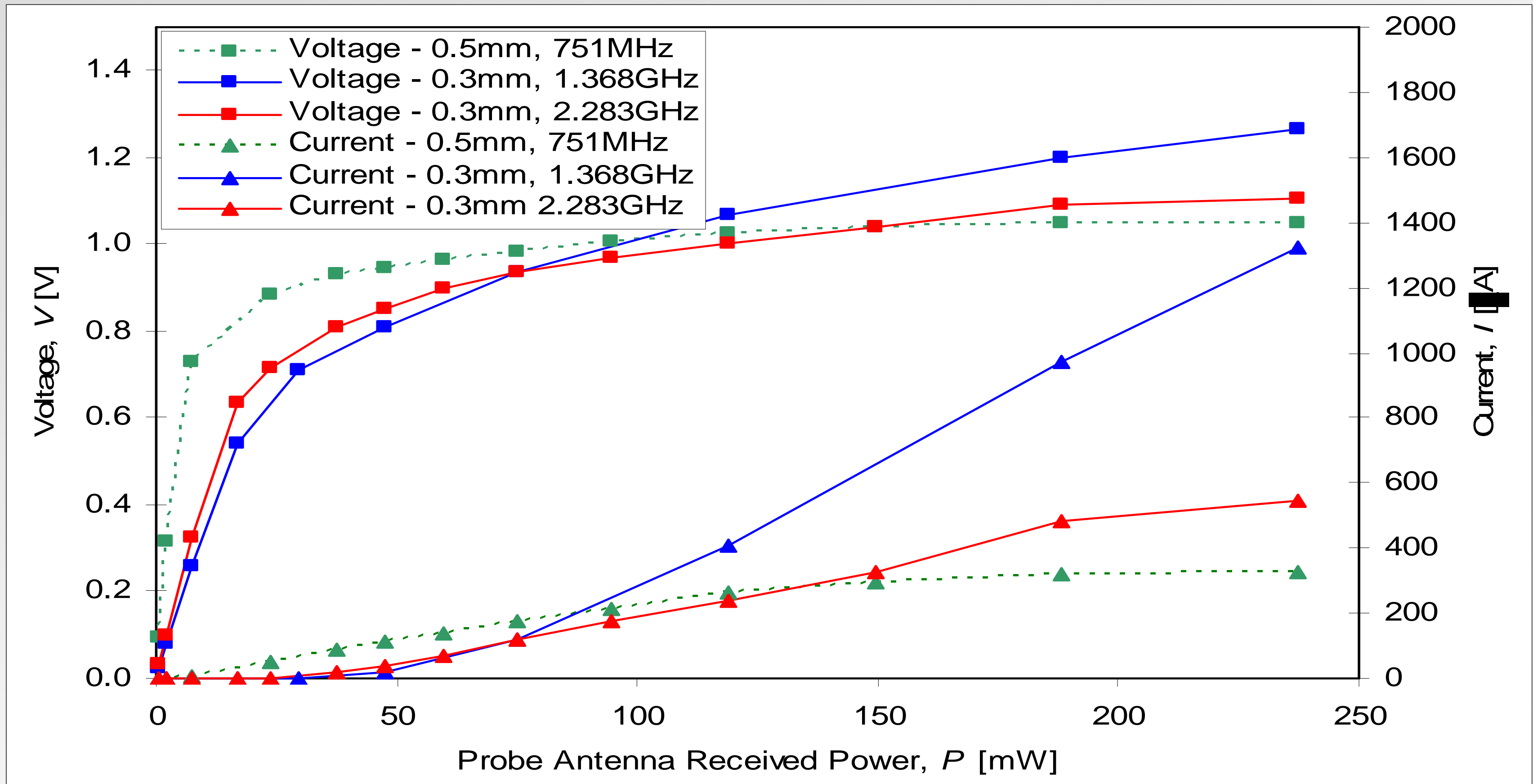
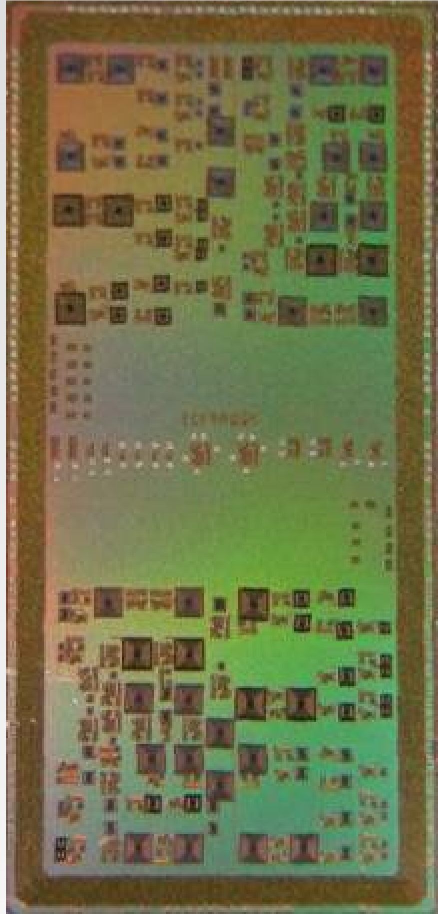
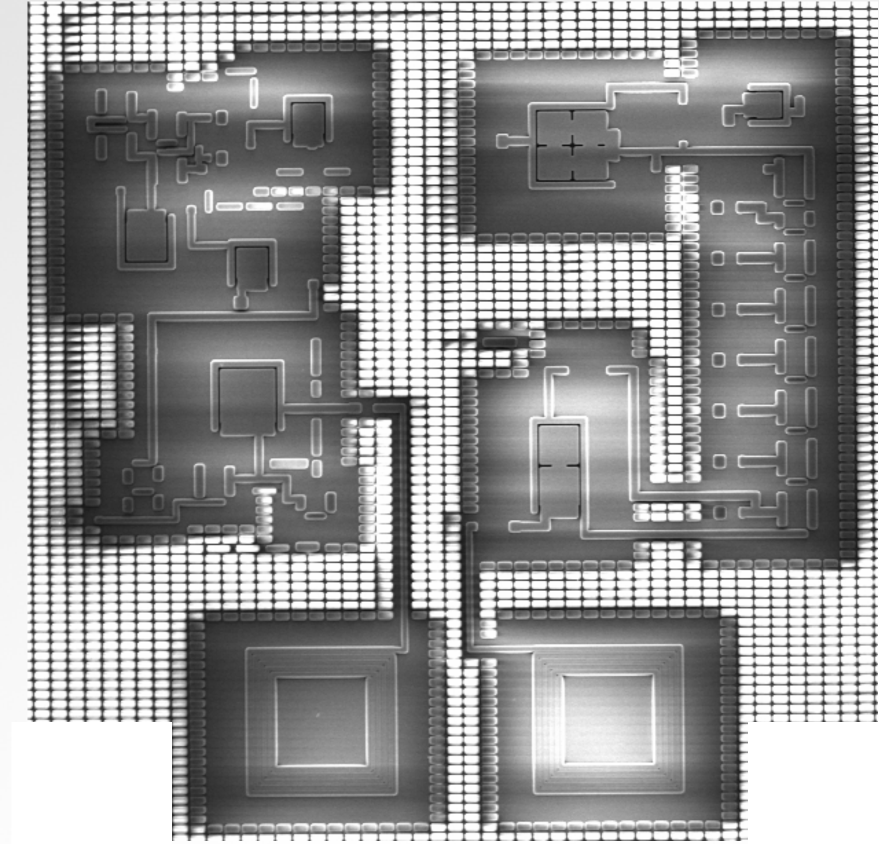
Power coupling



First generation silicon





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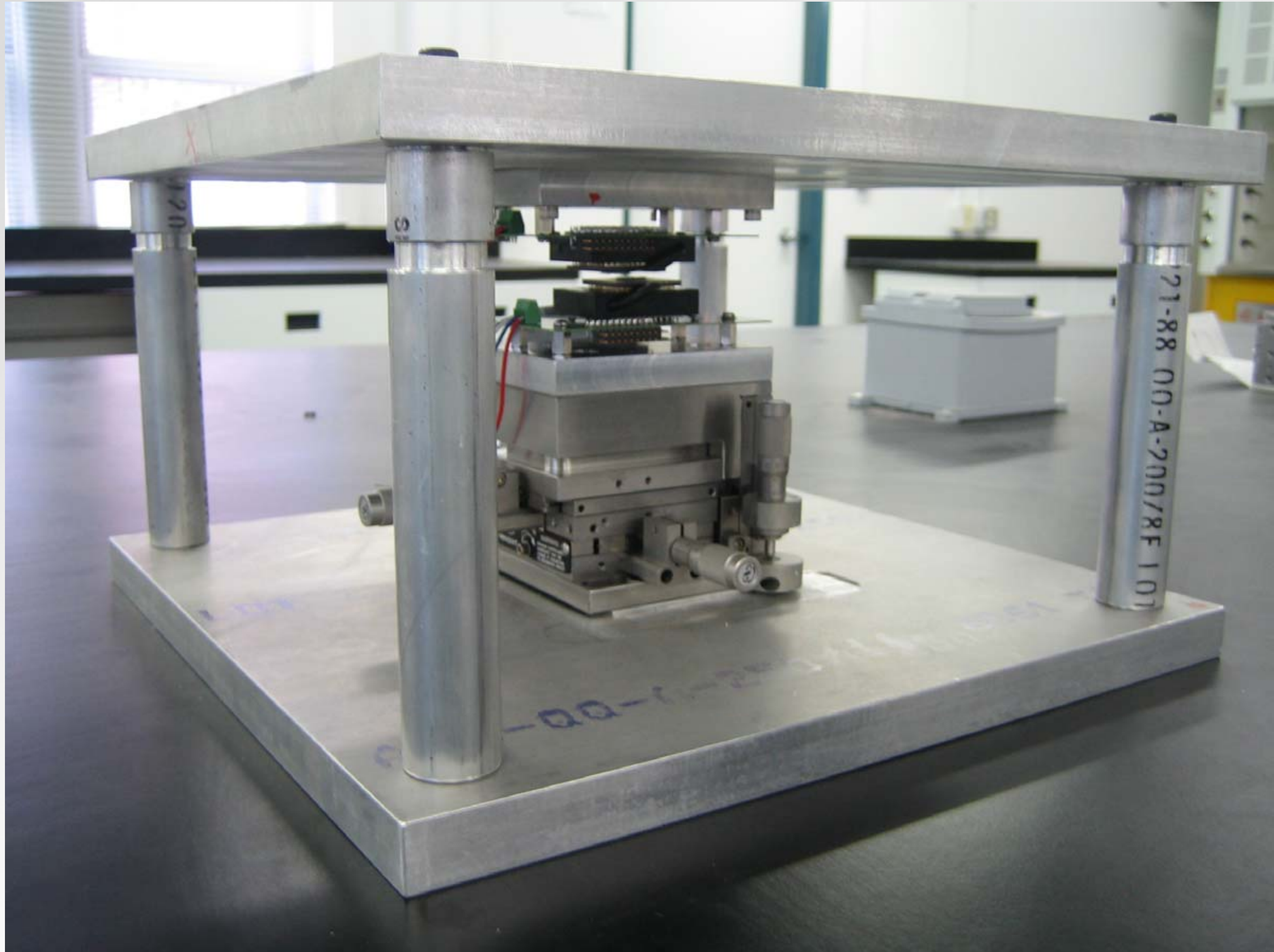
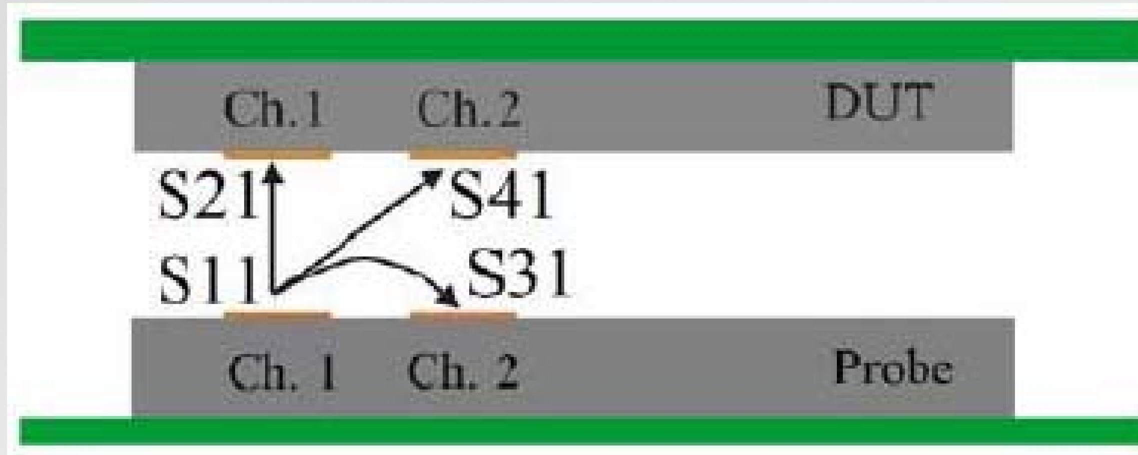
Test platform



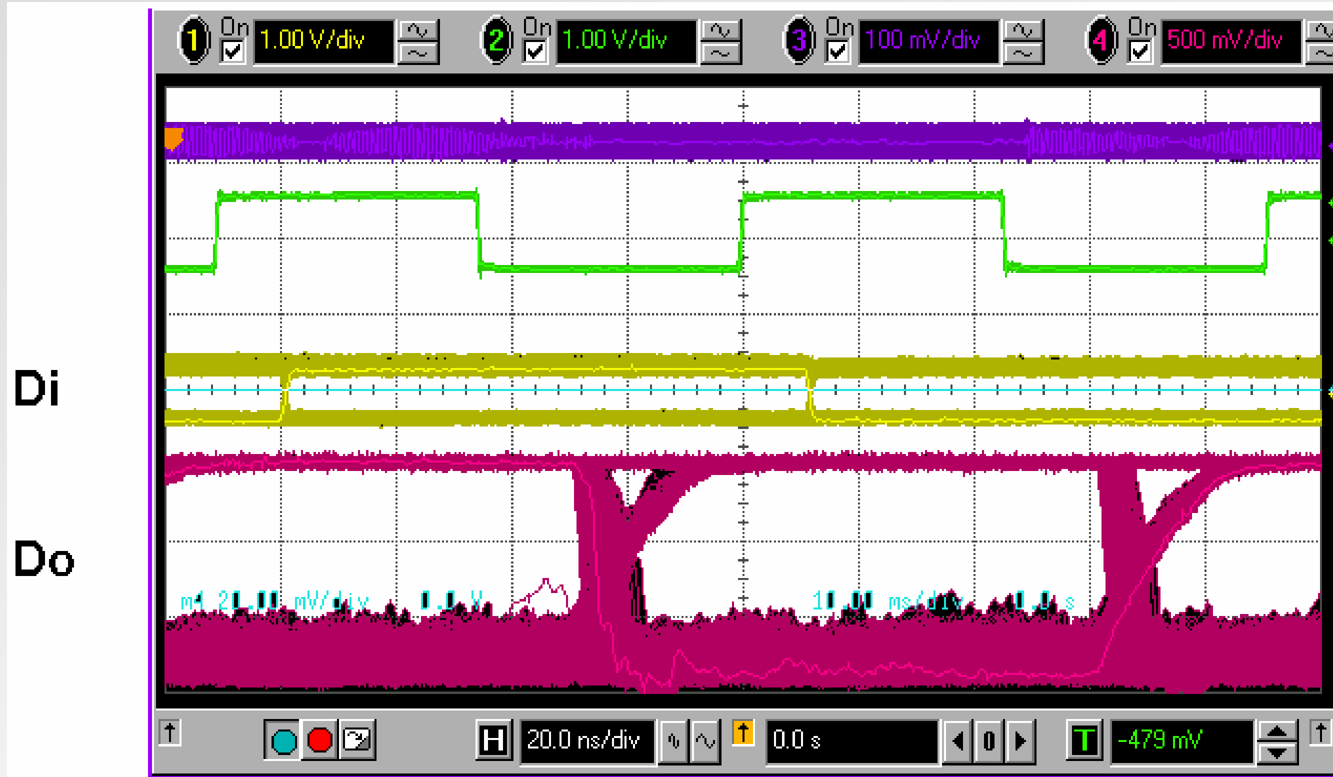
Coupling



Parameter	Size=60µm, f = 5GHz, z = 60µm	
	x = 30µm	x = 60µm
S21	-32dB	-32dB
S31	-44dB	-50dB
S41	-56dB	-55dB

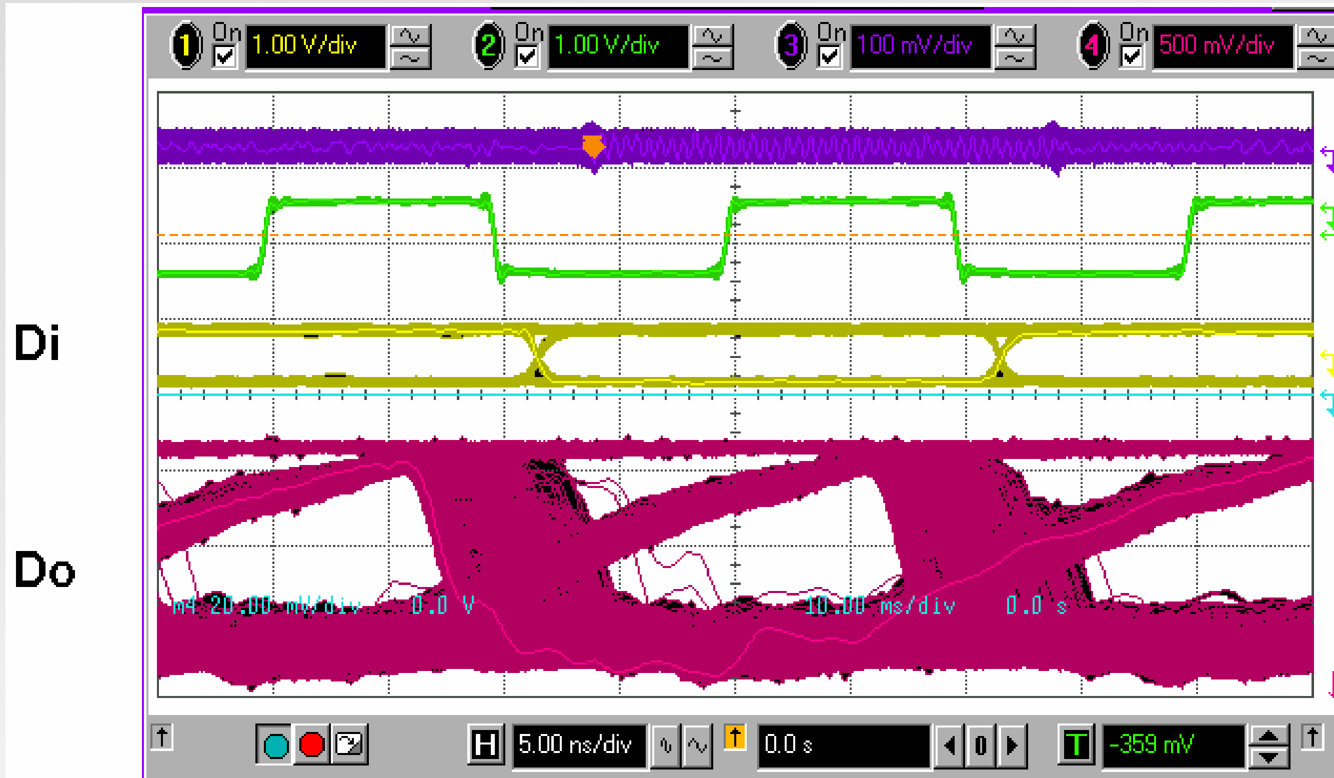
Sellathamby, et al, 2005 ITC

Data signaling



Eye Diagram of 20 MBPS data signal

Data signaling



Eye Diagram of 100 MBPS data signal

SCANIMETRICS

First generation silicon

- Bit error rate better than 10^{-12}
- 180nm process
  - Technology scales well
  - Two designs validated at two foundries
  - 130nm in fabrication
- Coupling devices 60um
  - Second generation 18um, 10x perf/size
  - Third generation, 10x perf/size

Conclusion

- Dramatically reduces chip manufacturing cost
- Enables new System in Package (SiP) technologies
- Vastly improves:
  - Chip size
  - Manufacturing control
  - Testing

"(Scanimetrics) technology is seminal in nature and the impact will be profound."

(Denny Sabo, former CEO, Arithmos)

Thank you!