A Multi-Mode Continuous-Time ΣΔ Modulator for a LTE/WCDMA/GSM Radio Receiver

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ABSTRACT

A multi-mode continuous-time ΣΔ modulator that achieves 70dB dynamic range while dissipating 16mW in an LTE 9MHz bandwidth mode, and also achieves 70dB/80dB dynamic range while dissipating 8mW in WCDMA/GSM 2MHz/200kHz modes respectively is presented. The modulator uses a 3rd order feed-forward architecture for the wide bandwidth LTE modes and is reconfigured as a 2nd order feed-back architecture for the WCDMA/GSM bandwidth modes. A 17-level quantizer is used for all modes. The modulator has been fabricated in a 90nm CMOS process and occupies 0.6mm2. The supply voltage is 1.5V.

INTRODUCTION

Because of their potential for wide bandwidth, high dynamic range and low power consumption as well as their inherent anti-alias filtering and improved immunity to substrate noise, continuous-time ΣΔ analog-to-digital converters (ADC) are increasingly becoming the architecture of choice for use in today's integrated portable multi-band radio receivers. Despite the aforementioned potential advantages, there are several challenges that arise when a continuous-time ΣΔ modulator is used in a portable multi-band radio receiver for which the receive bandwidths vary over a wide range and for which the power consumption must be minimized as much as possible over all bandwidths. Several recently published continuous-time ΣΔ modulators [1]-[3] present designs for which the performance has been optimized for a particular bandwidth. This paper presents a ΣΔ modulator that provides the required dynamic range for LTE, WCDMA, and GSM bandwidths with near optimal power consumption through the use of a re-configurable architecture that uses a 3rd order feed-forward architecture clocked at 208MHz for the wide bandwidth LTE modes and a 2nd order feed-back architecture clocked at 104 MHz for the WCDMA/GSM bandwidth modes.

A description of the multi-mode radio receiver requirements and the resulting ΣΔ modulator system design and the related challenges are provided in section 2. A brief description of the circuits that comprise the modulator is included in section 3. Section 4 presents measured results and section 5 presents some conclusions.

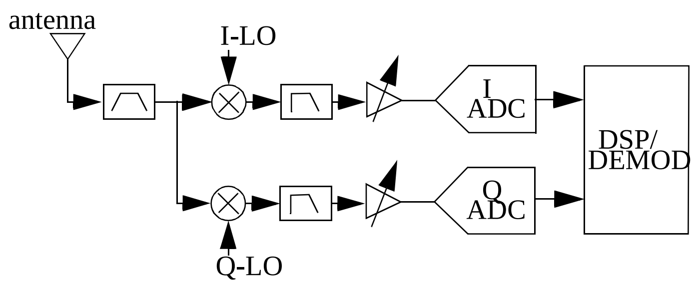

Figure 1 - Simplified block diagram of a direct-conversion baseband sampling radio receiver

SYSTEM OVERVIEW

A simplified block diagram of a commonly used receiver architecture is shown in figure 1 [4]. It is a direct-conversion/baseband sampling receiver and includes a pre-select filter, at least one mixer with the final mixer being quadrature and placing the final intermediate frequency (IF) at or near DC, a low pass filter, automatic gain control (AGC) and an ADC followed by additional digital selectivity and demodulation. In order to reduce the cost and performance requirements of the blocks preceding the ADC, the ADC is required to process wide bandwidth, large dynamic range signals, with minimal distortion and sampling energy (which might de-sense the receiver) and with minimal power consumption. For the LTE/WCDMA/GSM multi-mode radio receiver for which the presented continuous-time ΣΔ modulator is intended, the minimum ADC bandwidth, dynamic range and power requirements are 9MHz/2MHz/200kHz and 70dB/70dB/80dB with 20mW/10mW/10mW respectively.

In order to meet the LTE 9MHz dynamic range and power requirements, the 3rd-order fully-differential continuous-time ΣΔ modulator shown in figure 2.a) was chosen. The modulator uses a 17-level quantizer and is clocked at 208MHz giving an oversampling ratio of 11.6. The feed-back DACs use a non-return-to-zero (NRZ) pulse to improve immunity to clock jitter and an auxiliary local feedback DAC was used to mitigate the effects of excess-loop delay [5].

As explained in [6], during normal operation, an LTE receiver may encounter large blocking signals which can cause a 3rd-order feed-back modulator to become unstable and loose information until the loop

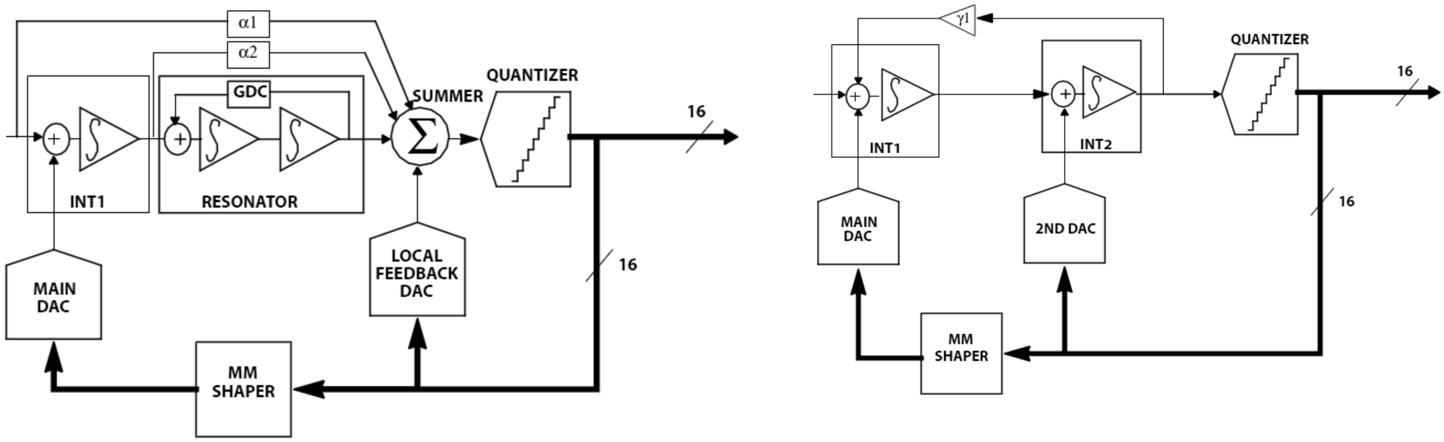

Figure 2. (a) modulator in LTE wide bandwidth mode (b) modulator in WCDMA/GSM mode

filter is reset. Consequently, a feed-forward architecture with only one feedback DAC to the loop filter was chosen. This architecture allows the modulator performance to gracefully degrade by limiting the outputs of the second and third integrators [3] so that order of the loop filter is reduced when a large input is applied to the modulator thereby allowing a quick recovery without the need for resetting loop filter.

Since the bandwidth requirements for the WCDMA and GSM modes are significantly lower, the 2nd-order feed-back modulator shown in figure 2.b) was sufficient. In WCDMA/GSM modes, the modulator is clocked at 104MHz giving an oversampling ratio of 26/260 respectively. The modulator uses a 17-level quantizer in this mode as well. The feedback DACs use RZ pulses in the narrower bandwidths in order to avoid the effects of excess-loop delay and the associated local-feedback DAC. Because a 2nd-order, feed-back modulator is inherently stable, the input overload behavior is acceptable without integrator limiting. Switching to a 2nd-order feedback modulator that does not require a high-speed summer also saves significant (nearly half) power.

The modulator switches between modes based on the power requirements of the receiver. The mode switches to the 3rd-order feed-forward architecture for required ADC bandwidths of 2.5MHz or greater and to the 2nd-order feed-back architecture otherwise.

CIRCUIT DESCRIPTION

Integrators

Because of the high speed and high gain requirements for the amplifier that is used in first integrator of the modulator, a Miller-compensated two-stage amplifier with active common-mode feedback was used [7]. The amplifier consumes 1.3mA including biasing and achieves a typical DC gain of 68dB, a unity gain bandwidth of 1.2GHz, and an output signal swing of more than 1V peak-to peak. The same amplifier was also employed in the second integrator which had similar gain and bandwidth requirements except that in WCMDA/GSM mode, the amplifier's current was scaled down by 30% because the gain and bandwidth requirements are reduced in that mode. The resistors and capacitors of the active-RC integrators are implemented as tunable arrays giving an overall post-tuning accuracy of 6%.

Summer

The primary summer design objective was to have sufficient DC gain for summing accuracy and sufficient bandwidth to process the high frequency content of the local feedback DAC which outputs current signals at the sampling frequency. System level

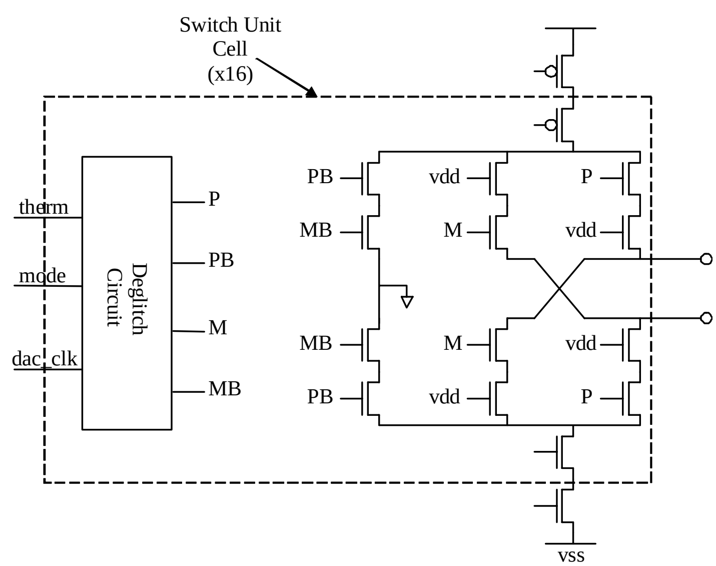

Figure. 3. DAC basic architecture.

simulations of the ADC were used to determine the actual gain and bandwidth requirements. Further design considerations were the relatively large capacitive load presented by the quantizer inputs; output swing; and sufficiently small differential offsets to minimize quantization errors.

In order to meet all of the above criteria, a fully differential two stage Miller compensated [8] OTA was chosen. The OTA has a telescopic pmos input first stage and common source nmos second stage with cascoded outputs. The OTA achieved closed loop bandwidths in excess of 500 MHz, DC voltage gains greater than 60 dB, and an output swing greater than +/- 500 mV single-ended.

The miller compensation capacitor in the OTA is calibrated to reduce variations in unity-gain bandwidth which in turn reduced variations in phase margin [8]. This allowed a reduced bias current in the second stage (which was a significant portion of the overall ADC supply current) relative to the case without calibration.

DAC

The DAC consists of an NMOS and a PMOS current mirror array and an array of 16 differential switches. To reduce the noise contributed to the signal path during the RZ phases used for the 2nd-order feed-back mode, a path is added to the conventional DAC switch architecture to shunt current (and noise) away from the signal path to the output common-mode voltage. The basic architecture is shown in Figure 3. Each switch unit cell consists of a deglitch circuit, switches, and cascode devices. The cascodes are placed in the switch unit cell to ensure that the parasitic capacitance on the critical nodes between the cascodes and the switches is minimized. This is particularly important when a mismatch shaper is used because switching activity is substantially higher. The deglitch circuit is designed to ensure that the signals P, M, PB, and MB cross above mid-rail so that a make-before-break transition occurs and that glitching of the output signals Ioutp and Ioutm are minimized. Additionally, these signals are controlled to implement RZ or NRZ operation based on the mode input bit. The mismatch shaper was implemented based on the work of Dr. Ian Galton [9].

Quantizer

The quantizer comprises 16 level-shifting preamplifiers and sixteen dynamic comparators to provide a 17-level thermometer code output with the center level corresponding to a differential input within +/- 31.25 mV or +/- 1/2 LSB of zero volts. A resistive ladder provides differential voltages in 1 LSB increments, so that each preamp output crosses zero at an input voltage corresponding to a specific threshold voltage, and all comparators operate to detect zero crossing for their respective level. Quiescent current consumption is 80uA per preamp. The resistor ladder draws about 300 uA of current from the 1.5 V supply, and the comparator array consumes roughly 350 uA during clocking at 208 MHz, so that the total operating current of the quantizer is under 2 mA in LTE mode.

EXPERIMENTAL RESULTS

A multi-mode continuous-time ΣΔ modulator has been fabricated in a 90nm CMOS process and occupies 0.6mm2. The supply voltage is 1.5V. All digital portions of the modulator were also integrated on chip. Fully-differential circuitry was used throughout the modulator for improved power supply rejection and increased dynamic range. Power consumption is 16mW in LTE 9MHz mode and 8mW in WCDMA/GSM 2MHz/200kHz modes. The required reference voltages were generated off chip. An FFT of the modulator output in LTE 9MHz mode is shown in figure 4. The measured input level versus SNR/SNDR is shown in figure 5 and is greater than 70dB for LTE/WCDMA modes and greater than 80dB for GSM mode. The input frequency versus SNR/SNDR for LTE 9MHz mode is shown in figure 6 and is also greater than 70dB for LTE/WCDMA modes and greater than 80dB for GSM mode. The measured performance is summarized in table 1.

Table 1: Summary of Measured Results

LTE 9MHz mode:	
peak SNR/SNDR)	70.5dB/64.5dB
clock rate	208MHz
power	16mW
WCDMA 2MHz mode	
peak SNR/SNDR	71.5dB/62dB
clock rate	104MHz
power	8mW
GSM 200kHz mode	
peak SNR/SNDR	80dB/64.5dB
clock rate	104MHz
power	8mW
supply voltage (all modes)	1.5V
chip area	0.6mm2

CONCLUSIONS AND ACKNOWLEDGMENTS

A multi-mode continuous-time ΣΔ modulator that is configured with a 3rd-order feed-forward loop filter with an NRZ pulse feedback DAC for wide bandwidths, and with a 2nd order feed-back loop filter with an RZ pulse feedback DAC for narrower bandwidths to achieve near-optimal power consumption over LTE/WCDMA/GSM bandwidths has been presented. The modulator has also been designed to exhibit graceful input overload behavior in all modes. An overview of the required circuits has also been presented.

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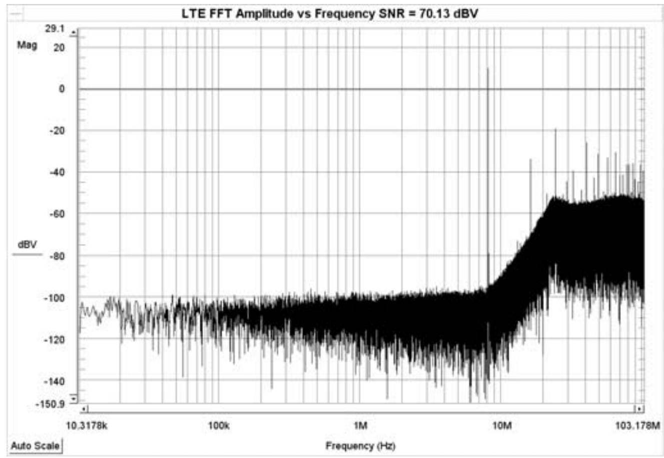

Figure 4. FFT of modulator output for LTE 9MHz mode

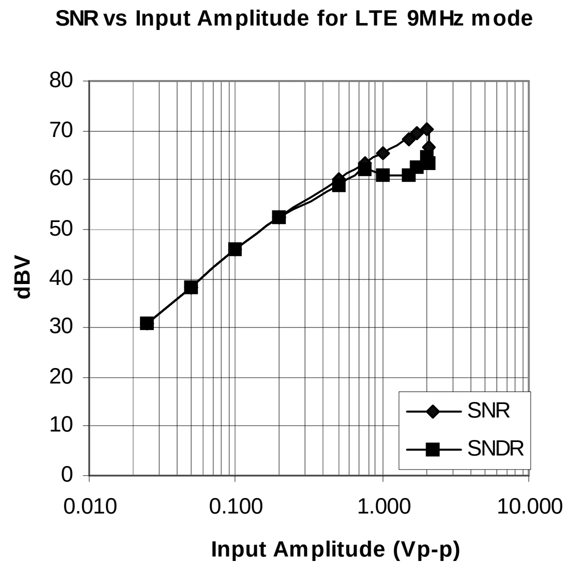

Figure 5. Input amplitude vs. SNR, SNDR for LTE 9MHz mode

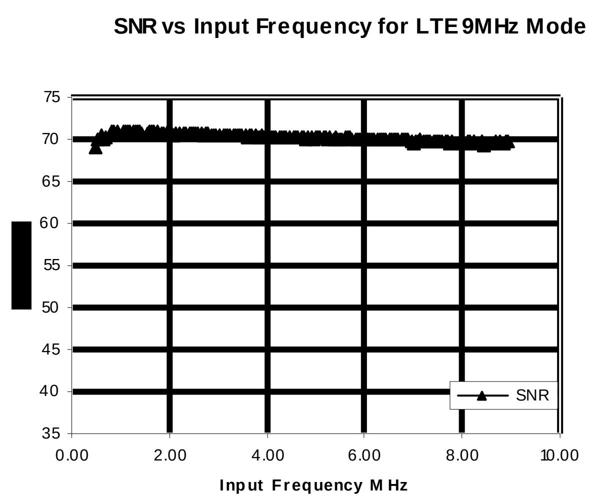

Figure 6. Input Amplitude vs. SNR for LTE 9MHz mode