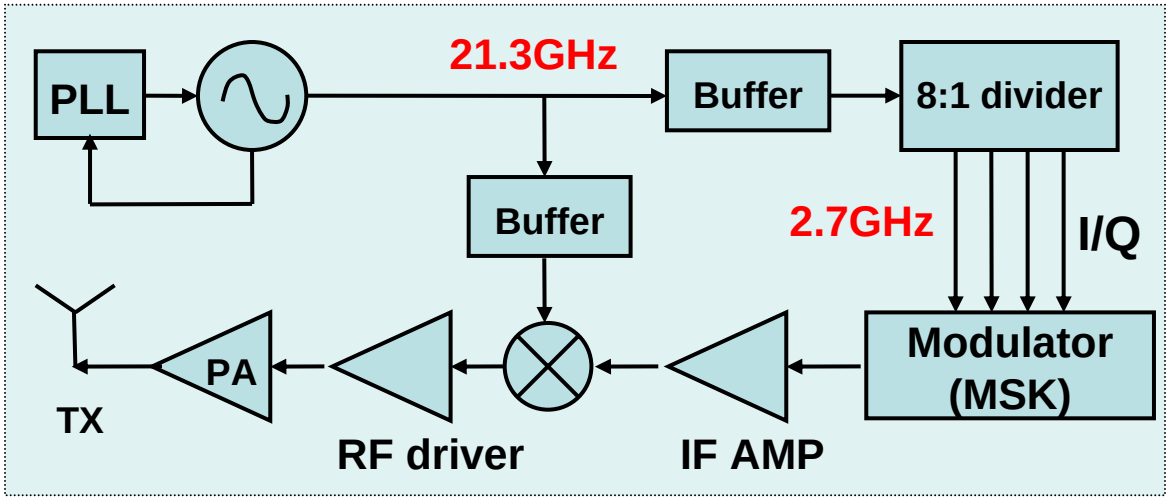
Single Chip RF Transmitter with On-Chip Antenna



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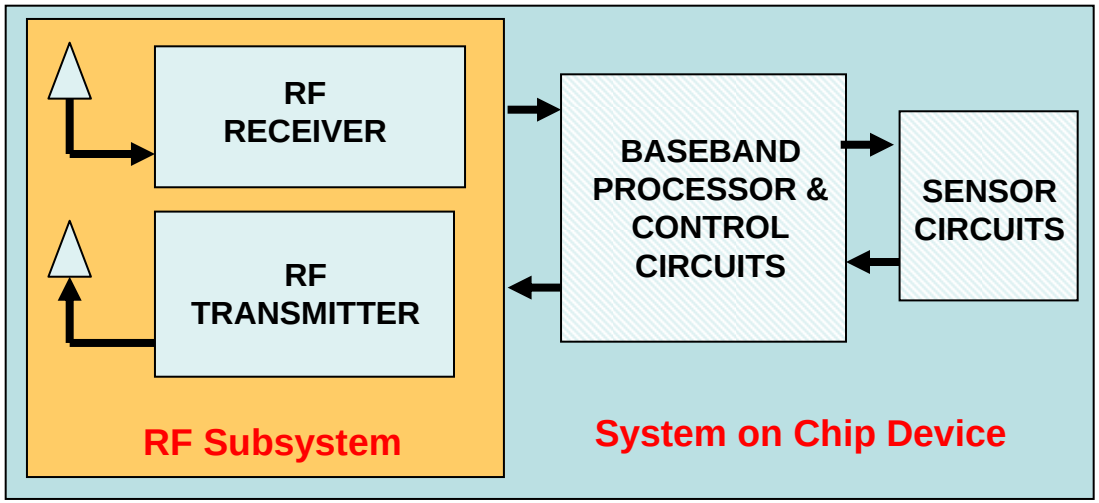
Single-chip radio

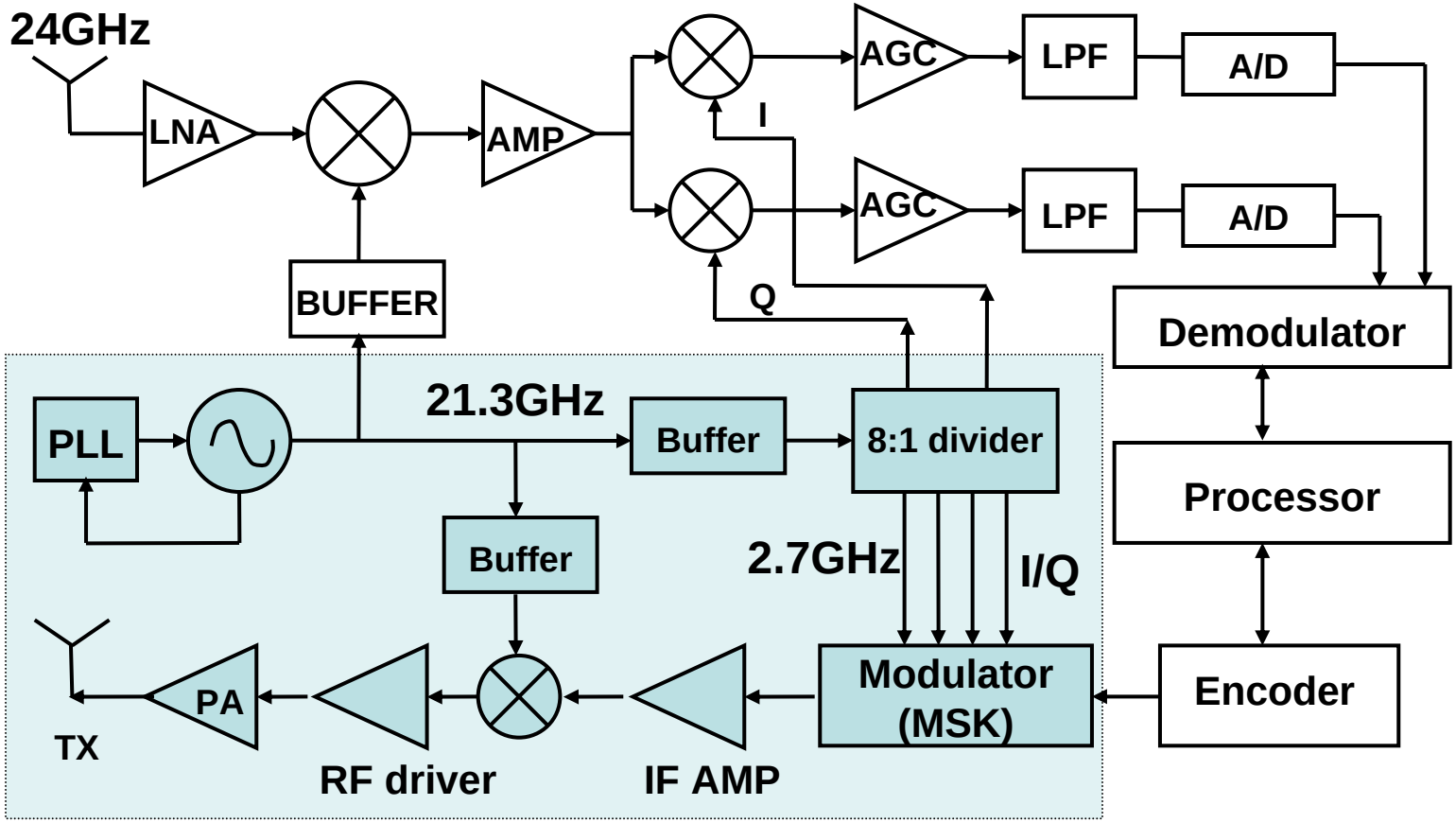


- **24-GHz true single chip radio including on-chip antennas, RF transceiver circuits, baseband processor, microcontroller, and frequency reference.**
- **Single chip radio will be**
  - **Reliable and easy to use**
  - **Low cost**
  - **Compact (~3 mm x 3 mm x 5 mm, difficult to detect)**

Single Chip Radio

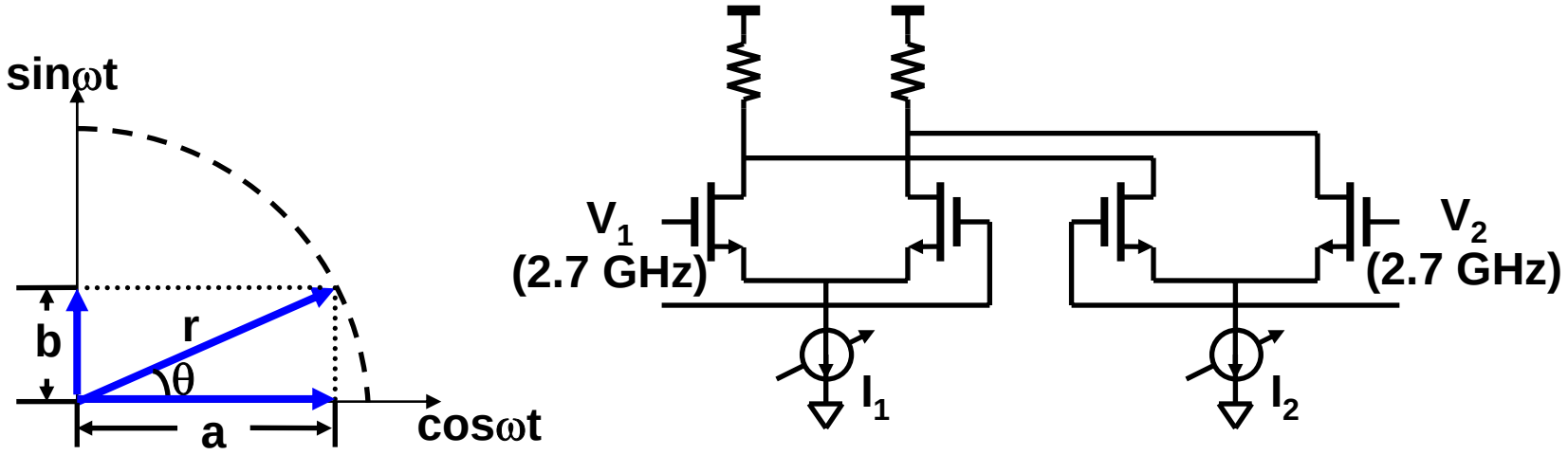
- **Current goal is to make the single chip radio + a power source to have the size of an m&m. Lifetime of 30 days with duty cycle of 0.1%.**
- **100-kbps node to node communication over 1-5 m.**
- **Communication between a node to a base station located up to 100 m away.**

Radio Architecture



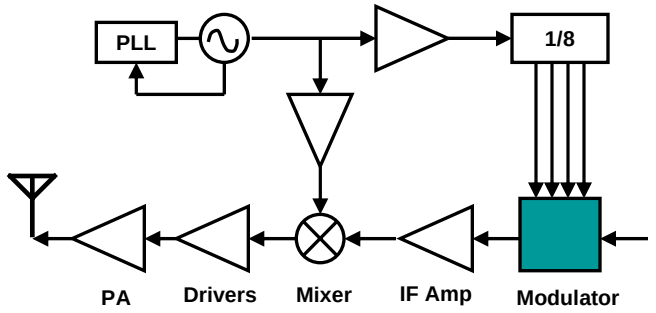
- Dual conversion requiring 1 synthesizer. RF=24 GHz, IF=2.7 GHz. This should effectively eliminate the unwanted coupling between the transmitted signal and VCO.
- 8-dB N.F. and 80-dB gain for the receiver. 10-dBm PA output.

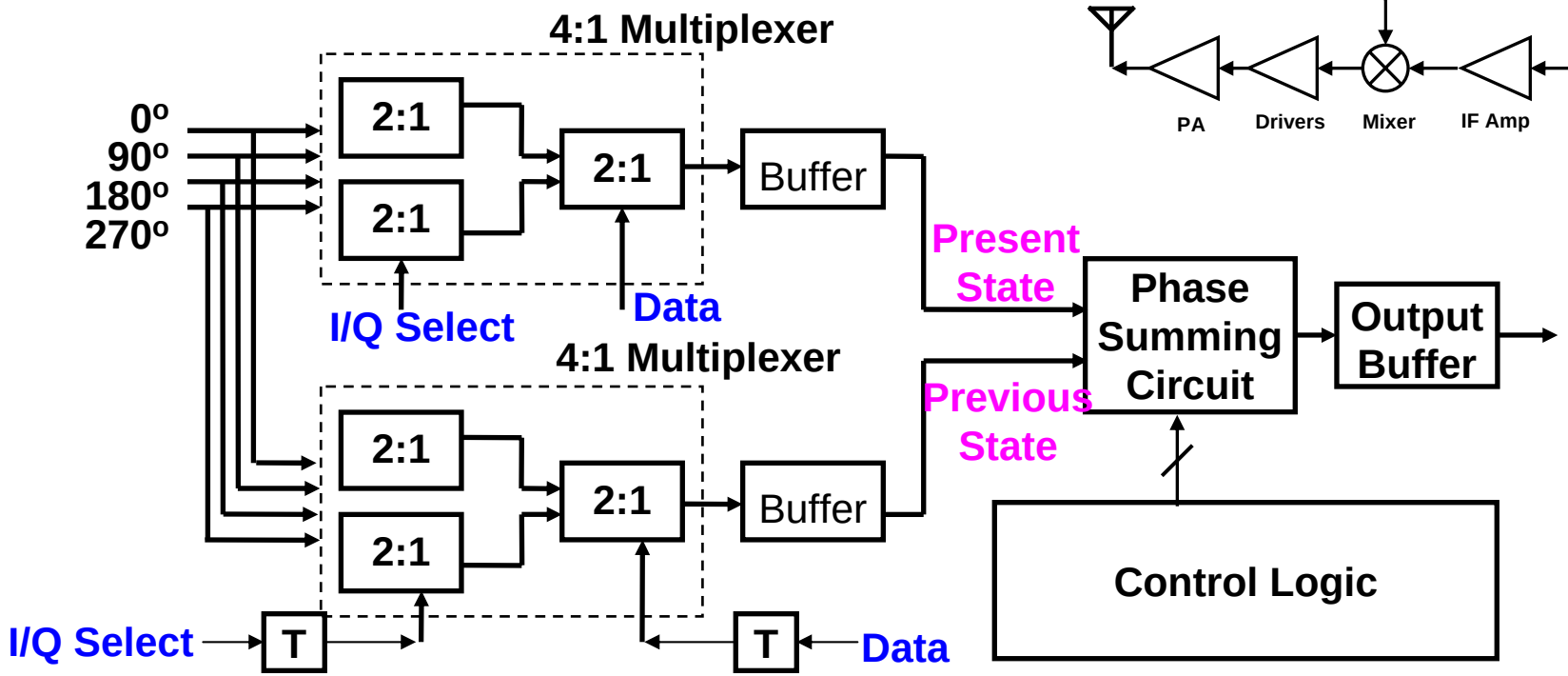
Arbitrary Phase Generation/Summing



- Phase combining using current summing
- Constant current → constant envelope
- Current consumption: 320 μA

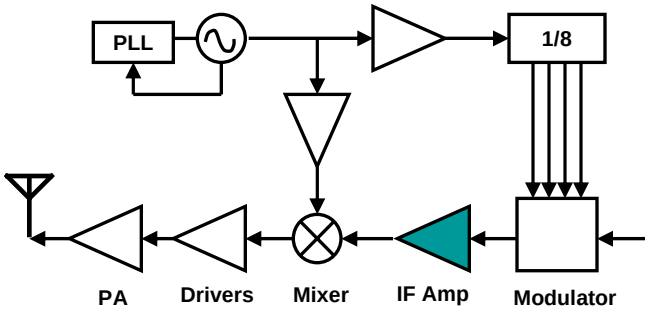
MSK Modulator

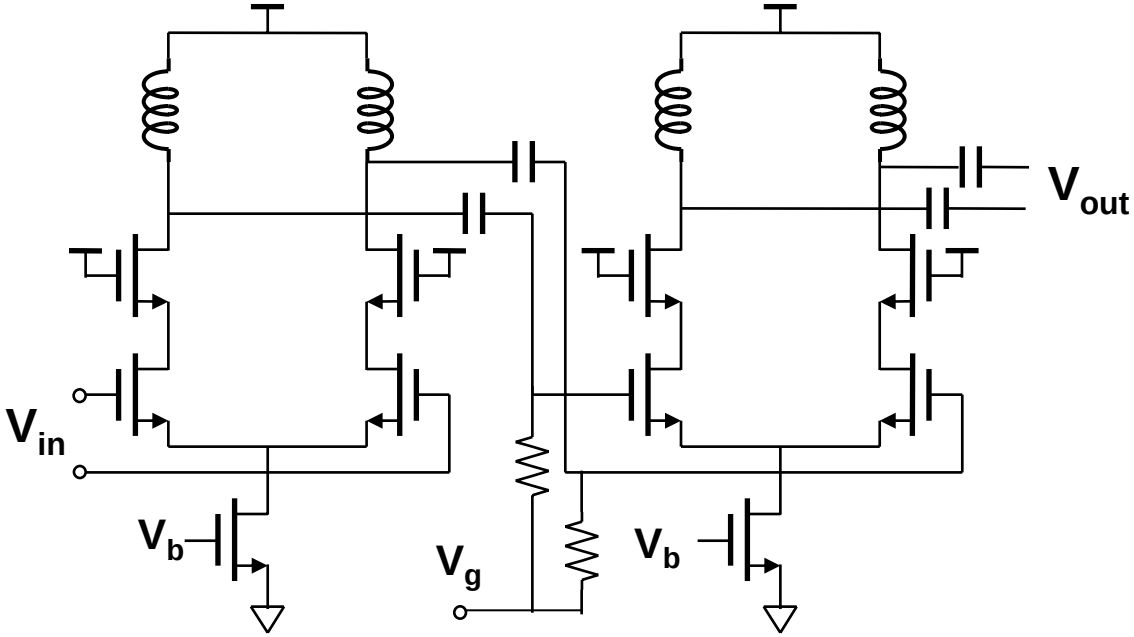




- No I/Q mixers and DAC, No IF filters
- Power dissipation: 2 mA x 1.5 V
- Data rate: greater than100 Mbps (Mcps)

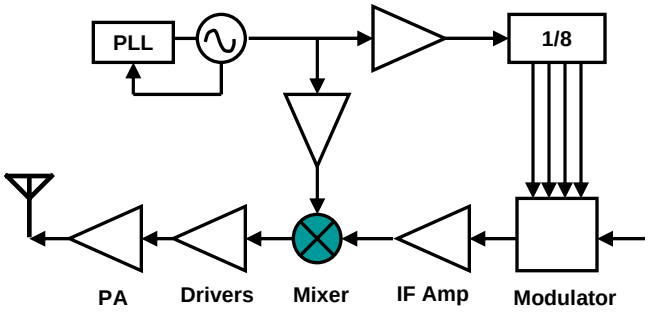
IF Amplifiers

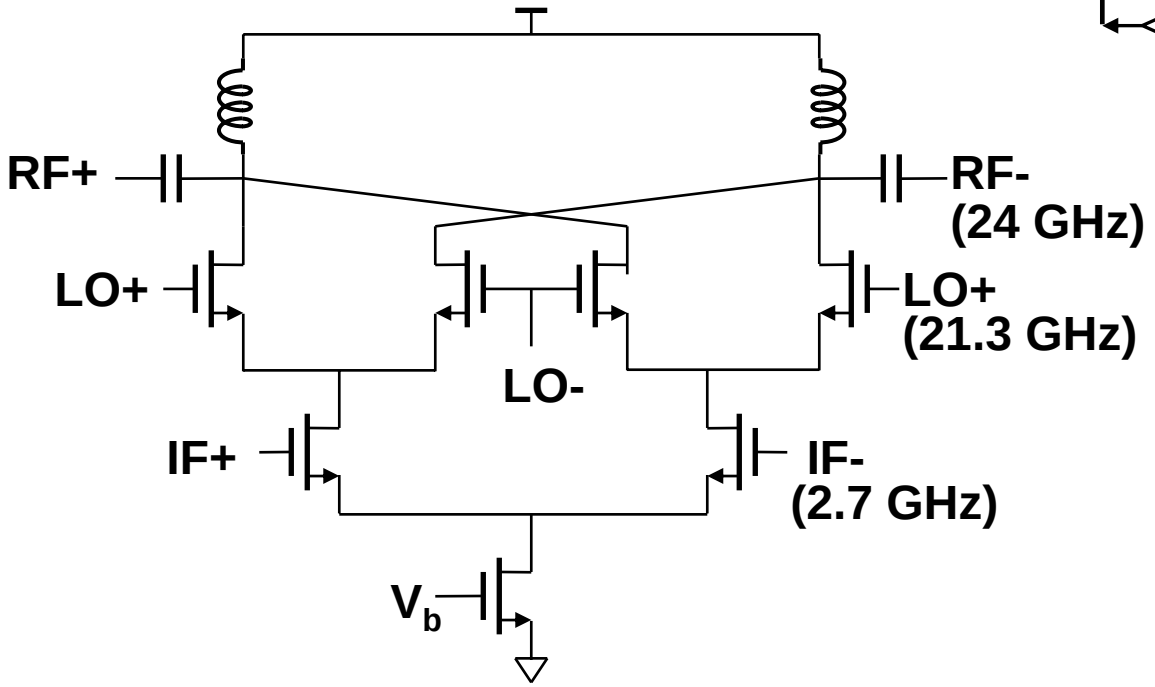




- Two stage cascode amplifiers
- Power dissipation: 5 mA x 1.5 V
- 18 dB power gain, -15 dBm IIP3 @ 2.7 GHz

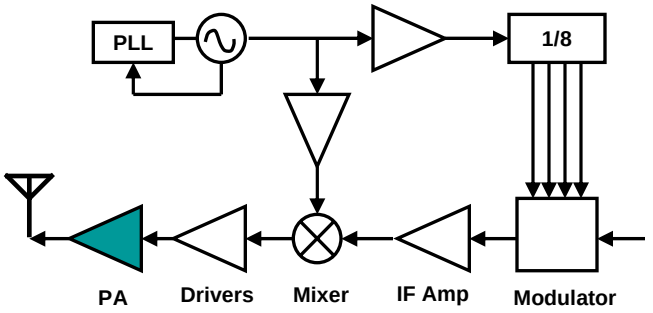
Mixer

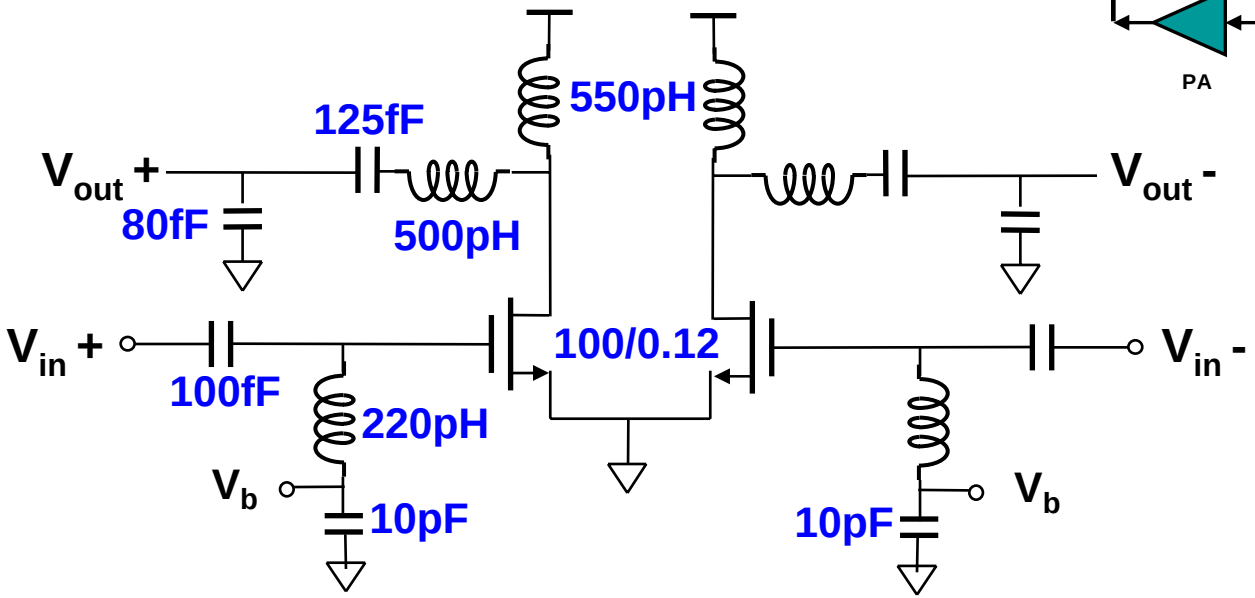




- Doubled balanced Gilbert cell
- Power dissipation: 4.5 mA x 1.5 V
- 1 dB power gain, -10 dBm P_{1dB}

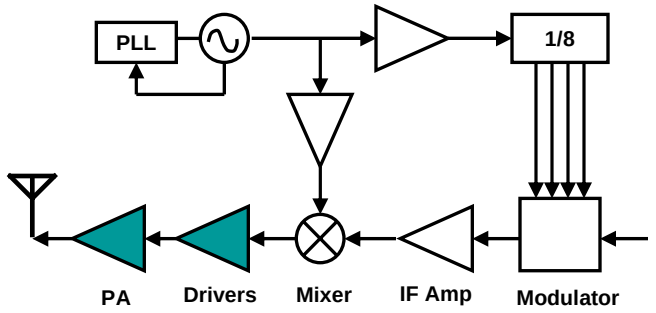
Power Amplifier

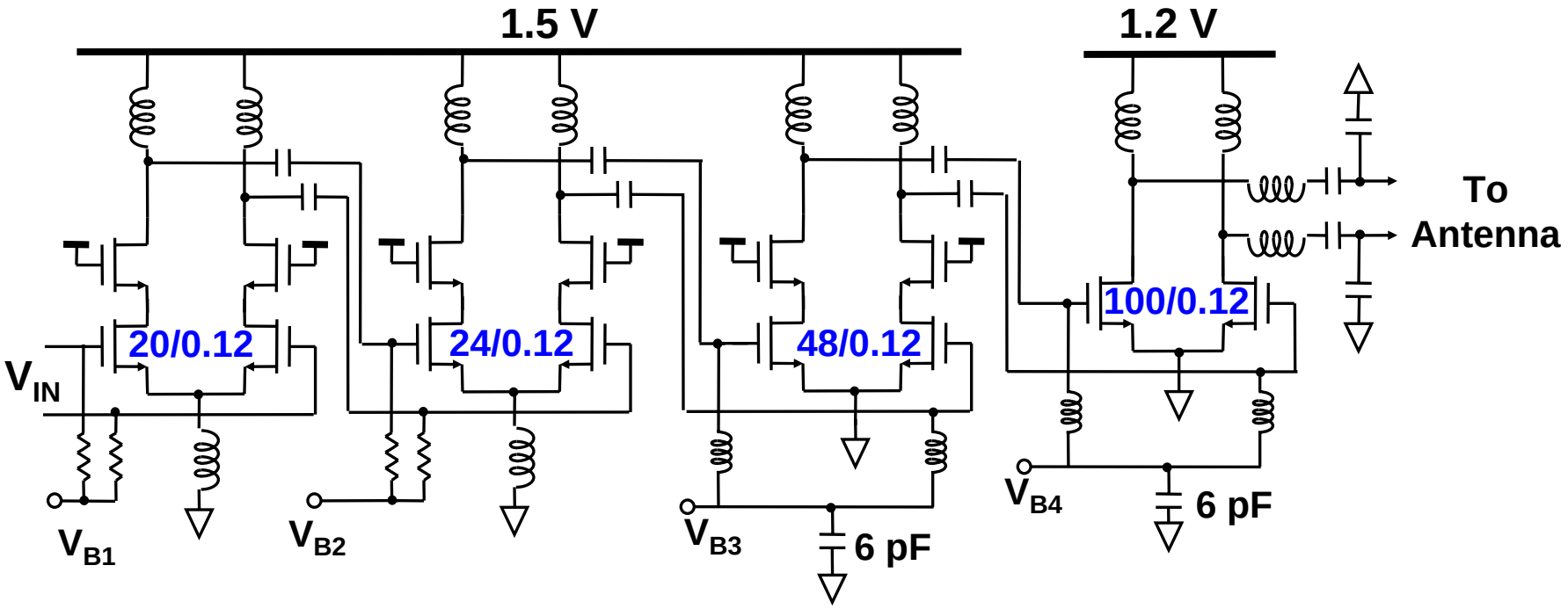




- Class-E configuration
- 10-dBm saturated output power at 1.2 V (Efficiency is ~ 20 %).
- 8-dBm saturated output power at 1.0 V

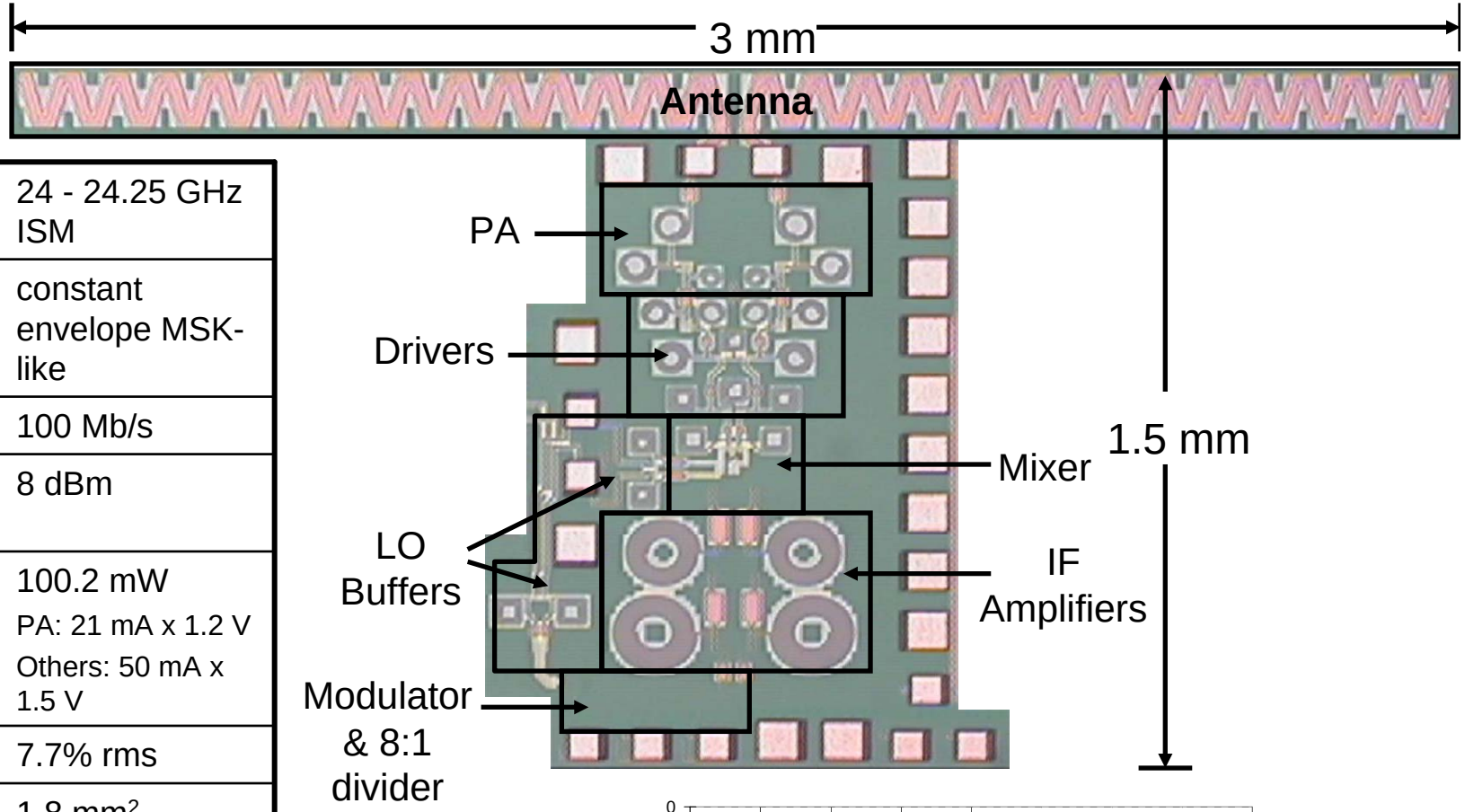
Drivers and PA





- Drivers: 4 stages tapered cascode amplifiers. First stage with 12-μm width (not shown).
- Fully-differential.

24GHz transmitter

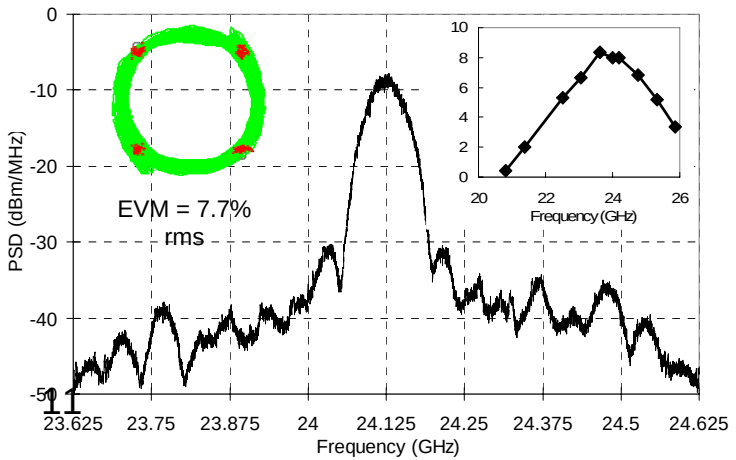


Frequency band	24 - 24.25 GHz ISM
Modulation	constant envelope MSK-like
Data rate	100 Mb/s
Output power	8 dBm
Power consumption	100.2 mW PA: 21 mA x 1.2 V Others: 50 mA x 1.5 V
EVM	7.7% rms
Chip Area	1.8 mm^2

UMC 130-nm 1P8M CMOS

Peak output power is 8 dBm.

Measured output spectrum for 100 Mb/s data rate is reasonable.



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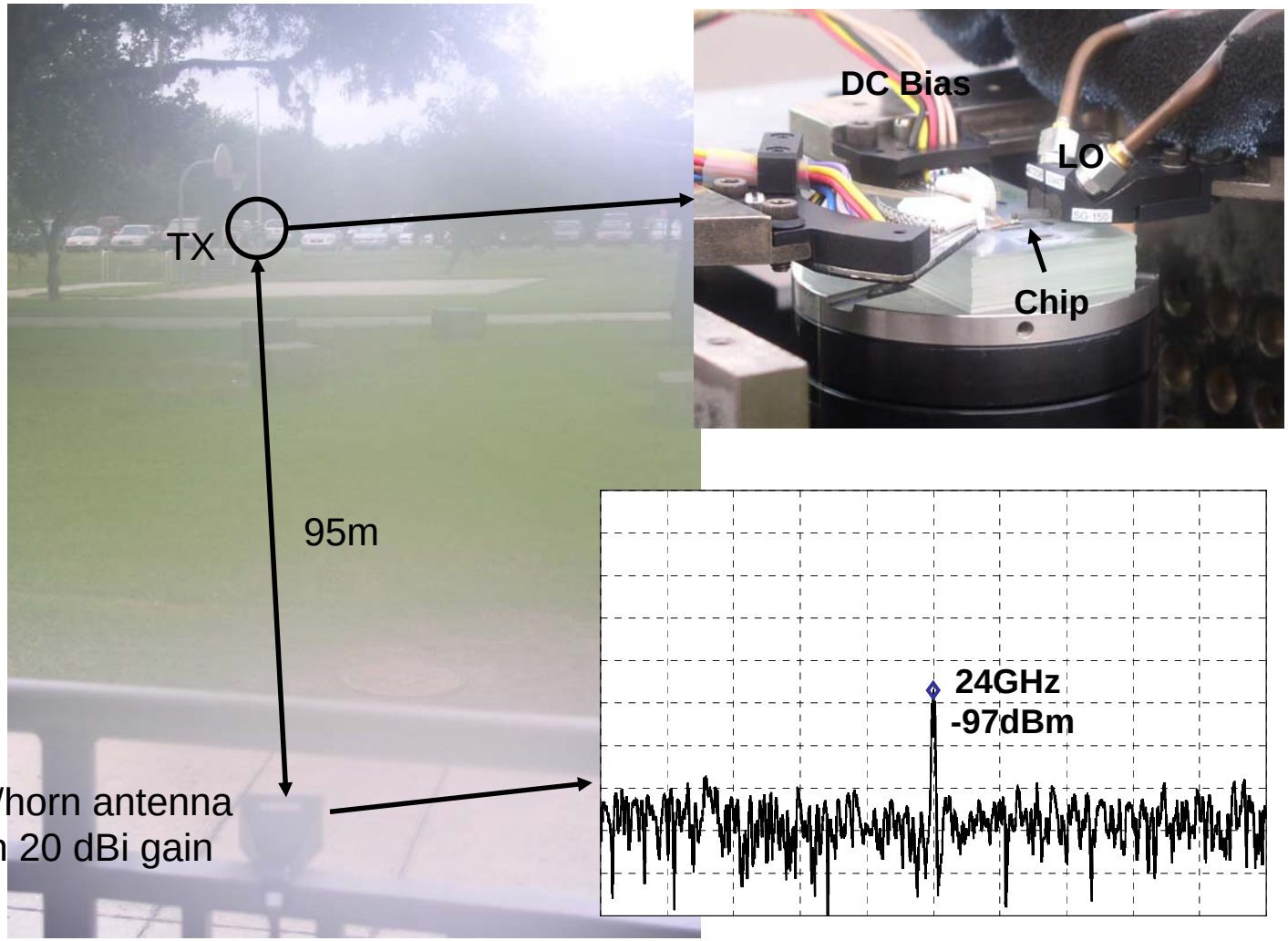
24-GHz Transmitter



- Reception of the signal from a transmitter IC with an on-chip antenna using a 20-dBi gain horn antenna 95 meters away. Communication over 90m using a CMOS radio with on-chip antennas is possible.

Transmitter Measurements (GSSG bond pads)

	W/O Notch Filters	With Notch Filters
Frequency band	24 - 24.25 GHz ISM	
Modulation	constant envelope MSK-like	
Data rate	100 Mb/s	
Output power	8 dBm	7.5 dBm
Power dissipation	100 mW (W/O Synthesizer) PA: 21 mA x 1.2 V Others: 50 mA x 1.5 V	154 mW PA: 23 mA x 1.2 V Others: 60 mA x 1.5 V Synthesizer: 36 mW

- To supply 150 mA peak current, use an ac13 Zn-O oxide battery (280 mAh) + 10 100μF chip capacitors which occupy ~530 mm^3.
- A sphere with ~1 cm diameter.
- Sufficient for 2 month operation at 0.1% duty cycle.

Conclusions

- A ~8-dBm 24-GHz transmitter with an on-chip antenna has been demonstrated in 130-nm CMOS technology.
- With an on-chip phase locked loop and antenna, it can provide ~6 dBm power to the antenna while consuming ~ 150 mW.
- Use of dual conversion architecture eliminates the VCO pulling problem even when the antenna and PA are integrated with a VCO at ~ 4dBm output power.
- LO and other stray emission problems can be controlled by employing on-chip notch filters.
- Communication over 90m using a CMOS radio with on-chip antennas is possible.
- There appears to be no fundamental limitations for Integration of antenna in a transmitter.